I²C-bus specification and user manual (UM10204). The I²C bus I/O is implemented with GPIO in open-drain modes.

UART Mode: This is a full-feature UART operating at up to 1 Mbps. It supports automotive single-wire interface (LIN), infrared interface (IrDA), and SmartCard (ISO7816) protocols, all of which are minor variants of the basic UART protocol. In addition, it supports the 9-bit multiprocessor mode that allows addressing of peripherals connected over common RX and TX lines. Common UART functions such as parity error, break detect, and frame error are supported. An 8-deep FIFO allows much greater CPU service latencies to be tolerated.

SPI Mode: The SPI mode supports full Motorola SPI, TI SSP (essentially adds a start pulse used to synchronize SPI Codecs), and National Microwire (half-duplex form of SPI). The SPI block can use the FIFO and also supports an EzSPI mode in which data interchange is reduced to reading and writing an array in memory.

GPIO

The PSoC 4100M has 55 GPIOs in the 68-pin QFN package. The GPIO block implements the following:

- Eight drive strength modes including strong push-pull, resistive pull-up and pull-down, weak (resistive) pull-up and pull-down, open drain and open source, input only, and disabled
- Input threshold select (CMOS or LVTTL)
- Individual control of input and output disables
- Hold mode for latching previous state (used for retaining I/O state in Deep Sleep mode and Hibernate modes)
- Selectable slew rates for dV/dt related noise control to improve EMI

The pins are organized in logical entities called ports, which are 8-bit in width. During power-on and reset, the blocks are forced to the disable state so as not to crowbar any inputs and/or cause excess turn-on current. A multiplexing network known as a high-speed I/O matrix is used to multiplex between various signals that may connect to an I/O pin. Pin locations for fixed-function peripherals are also fixed to reduce internal multiplexing complexity.

Data output and pin state registers store, respectively, the values to be driven on the pins and the states of the pins themselves.

Every I/O pin can generate an interrupt if so enabled and each I/O port has an interrupt request (IRQ) and interrupt service routine (ISR) vector associated with it (8 for PSoC 4100M).

The Pins of Port 6 (up to 6 depending on the package) are overvoltage tolerant (V_{IN} can exceed V_{DD}). The overvoltage cells will not sink more than 10 µA when their inputs exceed V_{DDIO} in compliance with I²C specifications.

Special Function Peripherals

LCD Segment Drive

The PSoC 4100M has an LCD controller, which can drive up to four commons and up to 51 segments. Any pin can be either a common or a segment pin. It uses full digital methods to drive the LCD segments requiring no generation of internal LCD voltages. The two methods used are referred to as digital correlation and PWM.

Digital correlation pertains to modulating the frequency and levels of the common and segment signals to generate the highest RMS voltage across a segment to light it up or to keep the RMS signal zero. This method is good for STN displays but may result in reduced contrast with TN (cheaper) displays.

PWM pertains to driving the panel with PWM signals to effectively use the capacitance of the panel to provide the integration of the modulated pulse-width to generate the desired LCD voltage. This method results in higher power consumption but can result in better results when driving TN displays. LCD operation is supported during Deep Sleep refreshing a small display buffer (4 bits; 1 32-bit register per port).

CapSense

CapSense is supported on all pins in the PSoC 4100M through a CapSense Sigma-Delta (CSD) block that can be connected to any pin through an analog mux bus that any GPIO pin can be connected to via an Analog switch. CapSense functionality can thus be provided on any pin or group of pins in a system under software control. A component is provided for the CapSense block, which provides automatic hardware tuning (Cypress SmartSense™), to make it easy for the user.

Shield voltage can be driven on another Mux Bus to provide water tolerance capability. Water tolerance is provided by driving the shield electrode in phase with the sense electrode to keep the shield capacitance from attenuating the sensed input.

Each CSD block has two IDACs which can be used for general purposes if CapSense is not being used.(both IDACs are available in that case) or if CapSense is used without water tolerance (one IDAC is available). The PSoC 4100M has two CSD blocks which can be used independently; one for CapSense and the other for IDACs.

The two CapSense blocks are referred to as CSD0 and CSD1. Capacitance sensing inputs on Ports 0, 1, 2, 3, 4, 6, and 7 are sensed by CSD0. Capacitance sensing inputs on Port 5 are sensed by CSD1.

Ordering Information

The PSoC 4100M family part numbers and features are listed in the following table.

Category	MPN	Features												Package			
		Max CPU Speed (MHz)	Flash (KB)	SRAM (KB)	Opamp (CTBm)	CSD	IDAC (1X7-BIT, 1-8-BIT)	Direct LCD Drive	12-bit SAR ADC	LP Comparators	TCPWM Blocks	SCB Blocks	GPIO	48-Pin TQFP	64-Pin TQFP (0.5mm pitch)	64-Pin TQFP (0.8mm pitch)	68-Pin QFN
4125	CY8C4125AZI-M433	24	32	4	2	–	–	–	806 Ksps	2	8	4	38	✔	–	–	–
	CY8C4125AZI-M443	24	32	4	2	✔	–	✔	806 Ksps	2	8	4	38	✔	–	–	–
	CY8C4125AZI-M445	24	32	4	2	✔	–	✔	806 Ksps	2	8	4	51	–	✔	–	–
	CY8C4125LTI-M445	24	32	4	2	✔	–	✔	806 Ksps	2	8	4	55	–	–	–	✔
	CY8C4125AXI-M445	24	32	4	2	✔	–	✔	806 Ksps	2	8	4	51	–	–	✔	–
4126	CY8C4126AZI-M443	24	64	8	2	✔	–	✔	806 Ksps	2	8	4	38	✔	–	–	–
	CY8C4126AZI-M445	24	64	8	2	✔	–	✔	806 Ksps	2	8	4	51	–	✔	–	–
	CY8C4126AZI-M475	24	64	8	4	–	✔	–	806 Ksps	2	8	4	51	–	✔	–	–
	CY8C4126LTI-M445	24	64	8	2	✔	–	✔	806 Ksps	2	8	4	55	–	–	–	✔
	CY8C4126LTI-M475	24	64	8	4	–	✔	–	806 Ksps	2	8	4	55	–	–	–	✔
	CY8C4126AXI-M445	24	64	8	2	✔	–	✔	806 Ksps	2	8	4	51	–	–	✔	–
4127	CY8C4127LTI-M475	24	128	16	4	✔	✔	–	806 Ksps	2	8	4	55	–	–	–	✔
	CY8C4127AZI-M475	24	128	16	4	–	✔	–	806 Ksps	2	8	4	51	–	✔	–	–
	CY8C4127AZI-M485	24	128	16	4	✔	✔	✔	806 Ksps	2	8	4	51	–	✔	–	–
	CY8C4127AXI-M485	24	128	16	4	✔	✔	✔	806 Ksps	2	8	4	51	–	–	✔	–

The nomenclature used in the preceding table is based on the following part numbering convention:

Field	Description	Values	Meaning
CY8C	Cypress Prefix		
4	Architecture	4	PSoC 4
A	Family	2	4200 Family
B	CPU Speed	4	48 MHz
C	Flash Capacity	4	16 KB
		5	32 KB
		6	64 KB
		7	128 KB
DE	Package Code	AX, AZ	TQFP
		LQ	QFN
		BU	BGA
		FD	CSP
F	Temperature Range	I	Industrial