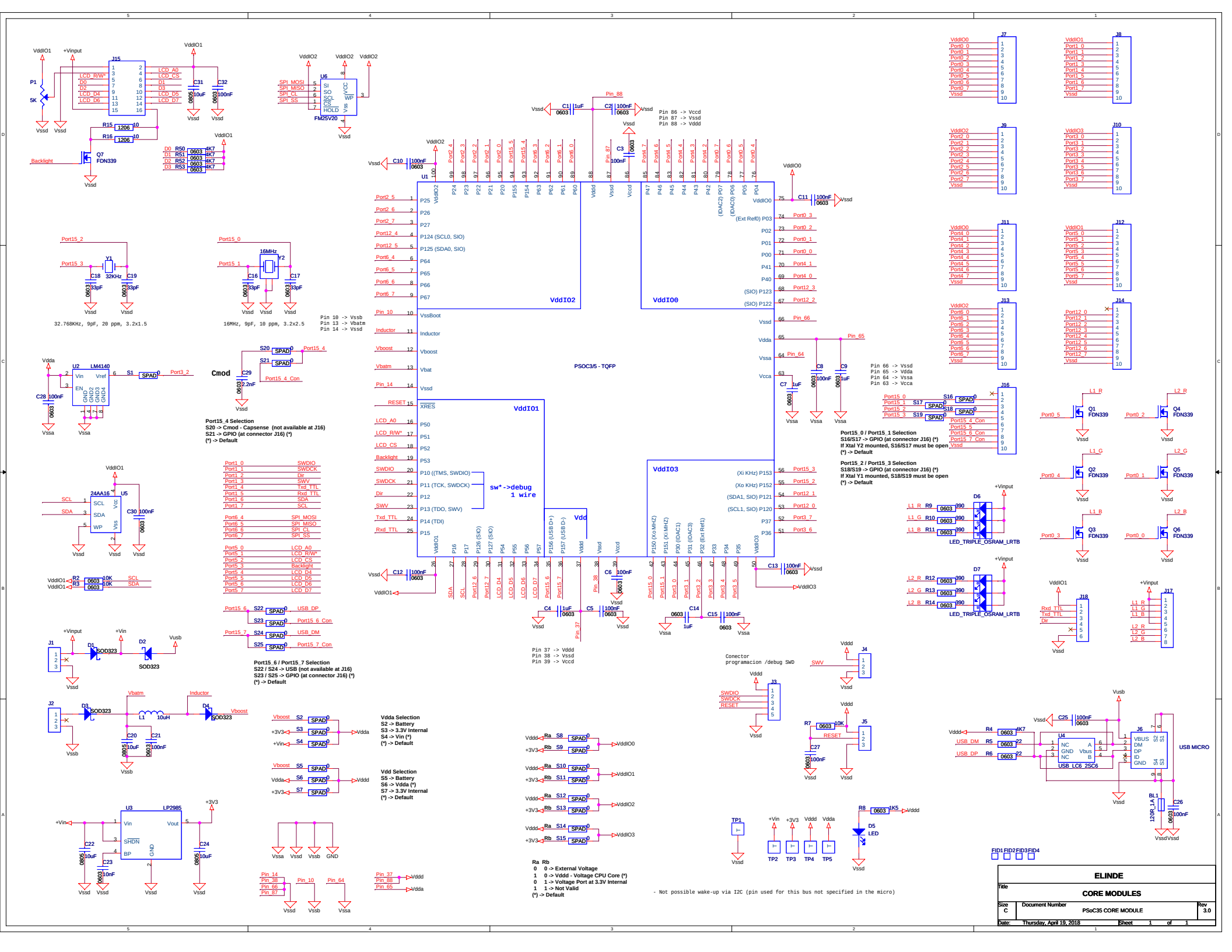
PSOC3/5 - TQFP
VddIO2
VddIO0
VddIO1
VddIO3
Vdd
sw*->debug
1 wire
Pin 86 -> Vccd
Pin 87 -> Vssd
Pin 88 -> Vddd
Pin 10 -> Vssb
Pin 13 -> Vbatm
Pin 14 -> Vssd
Pin 66 -> Vssd
Pin 65 -> Vdda
Pin 64 -> Vssa
Pin 63 -> Vcca
Pin 37 -> Vddd
Pin 38 -> Vssd
Pin 39 -> Vccd
32.768KHz, 9pF, 20 ppm, 3.2x1.5
16MHz, 9pF, 10 ppm, 3.2x2.5
Port15_4 Selection
S20 -> Cmod - Capsense (not available at J16)
S21 -> GPIO (at connector J16) (*)
(*) -> Default
Port15_6 / Port15_7 Selection
S22 / S24 -> USB (not available at J16)
S23 / S25 -> GPIO (at connector J16) (*)
(*) -> Default
Vdda Selection
S2 -> Battery
S3 -> 3.3V Internal
S4 -> Vin (*)
(*) -> Default
Vdd Selection
S5 -> Battery
S6 -> Vdda (*)
S7 -> 3.3V Internal
(*) -> Default
Port15_0 / Port15_1 Selection
S16/S17 -> GPIO (at connector J16) (*)
If Xtal Y2 mounted, S16/S17 must be open
(*) -> Default
Port15_2 / Port15_3 Selection
S18/S19 -> GPIO (at connector J16) (*)
If Xtal Y1 mounted, S18/S19 must be open
(*) -> Default
Ra Rb
0 0 -> External Voltage
1 0 -> Vddd - Voltage CPU Core (*)
0 1 -> Voltage Port at 3.3V Internal
1 1 -> Not Valid
(*) -> Default
- Not possible wake-up via I2C (pin used for this bus not specified in the micro)
Conector programacion /debug SWD
USB MICRO
LED_TRIPLE_OSRAM_LRTB
ELINDE
CORE MODULES
PSoC35 CORE MODULE
Thursday, April 19, 2018