OTP Lock Command for SLC NAND Flash Memory

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AN209699 documents the command set sequence that is used to permanently protect the OTP area from program operations.

1 Introduction

Cypress SLC NAND products include a One Time Programmable (OTP) area, which is an additional block outside the main flash memory array where sensitive data or code can be stored permanently. A dedicated command set is used to access and permanently protect the OTP area from program operations. The OTP protection status can be read in a bit of the Status Register.

2 OTP Area Protection

2.1 OTP Lock Command Sequence

Table 1. OTP Area Protection Command Sequence

Command	1st Cycle	2nd Cycle	3rd Cycle	4th Cycle	5th Cycle	6th Cycle	7th Cycle
OTP Entry	29h	17h	04h	19h	-	-	-
OTP Protection Setup	4Ch	03h	1Dh	41h	-	-	-
Page Program	80h	00h	00h	00h	00h	00h	10h

Following the OTP protection setup sequence, a page program sequence with an address of zero and without data input is issued by the host system to program the protection control bit for the OTP area. The status register read command is then used to poll the status register to determine when the programming operation is completed and verify that the OTP area is protected. To exit OTP area access mode, a Reset command (FFh) is issued by the host system.
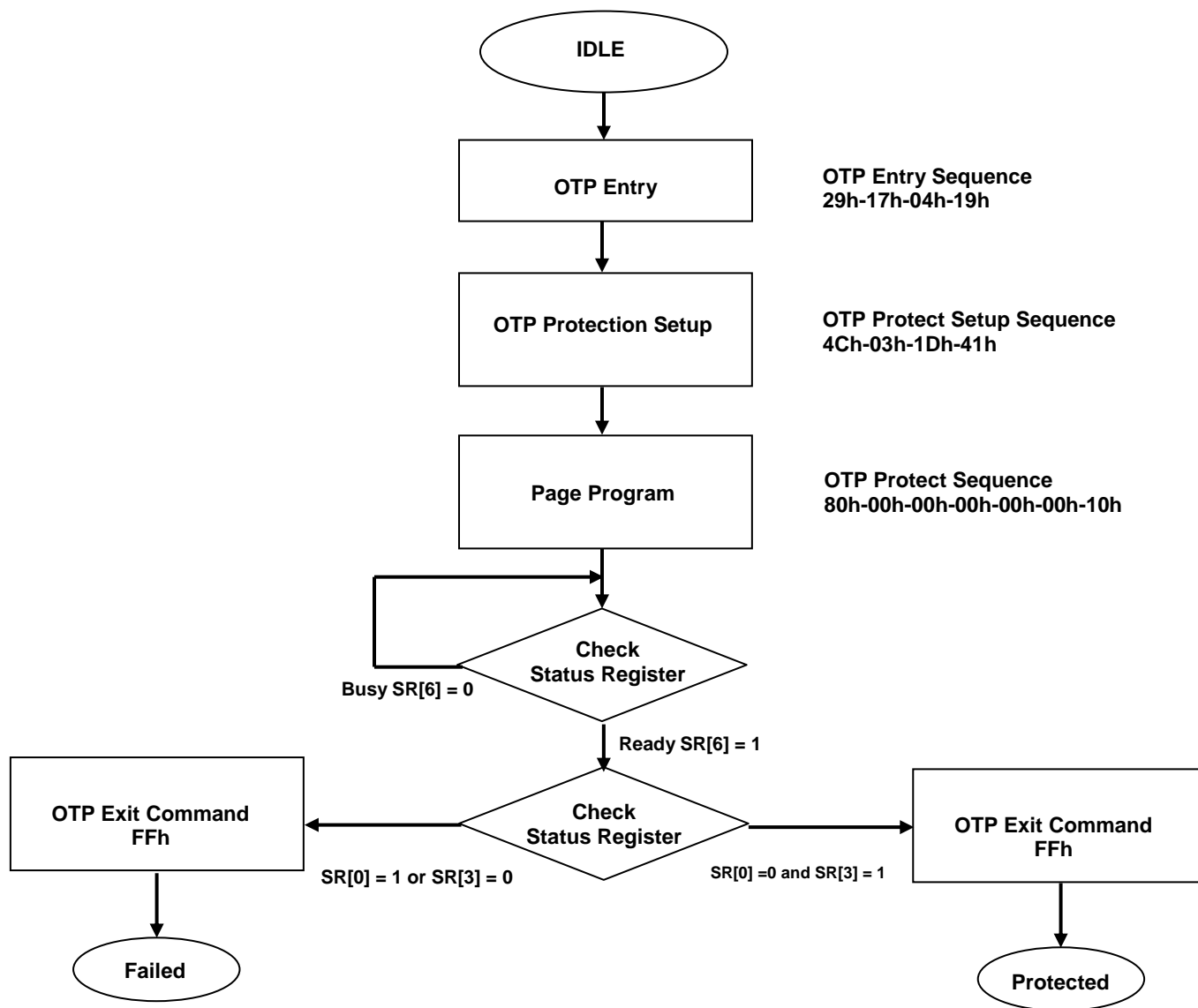
2.2 Status Register

After the OTP area protect command sequence is issued by the host system, the host system can read the Status Register bit 0 (SR[0]) to check whether the operation has been completed successfully (SR[0]=0) or not (SR[0]=1). The user can read the Status Register bit 3 (SR[3]) to check whether the OPT area is protected (SR[3]=1) or not (SR[3]=0).
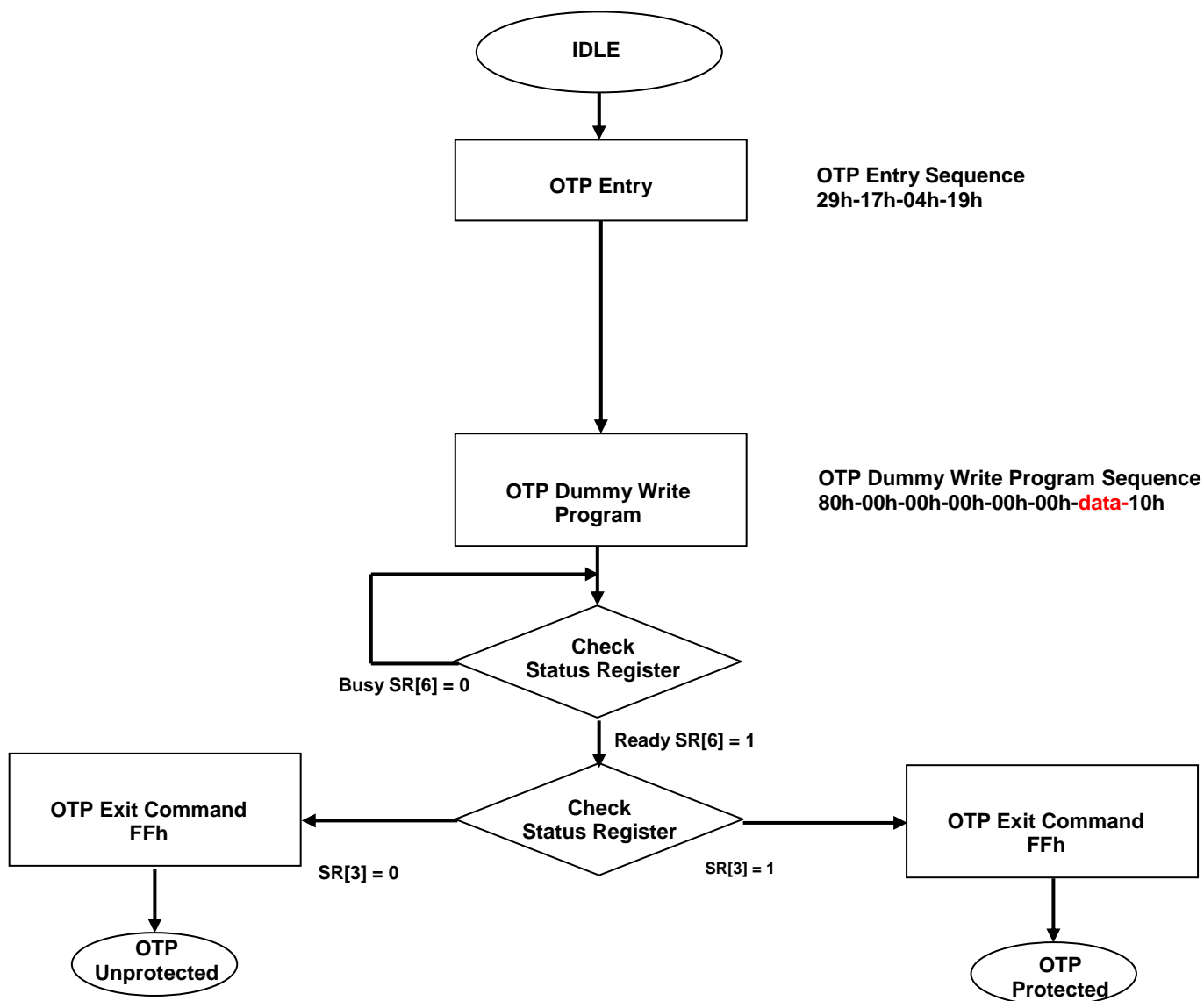
Table 2. Status Register Coding

SR bit	Program/Erase	CODING
0	Pass / Fail	Pass: '0' Fail: '1'
3	Protection Status	Unprotected: '0' Protected: '1'
6	Ready / Busy	Busy: '0' Ready: '1'

2.3   OTP Lock Command Sequence Flow Chart

```
                        ┌─────────────┐
                        │    IDLE     │
                        └─────────────┘
                               │
                               ▼
                    ┌────────────────────┐        OTP Entry Sequence
                    │     OTP Entry      │        29h-17h-04h-19h
                    └────────────────────┘
                               │
                               ▼
                    ┌────────────────────┐        OTP Protect Setup Sequence
                    │ OTP Protection Setup│       4Ch-03h-1Dh-41h
                    └────────────────────┘
                               │
                               ▼
                    ┌────────────────────┐        OTP Protect Sequence
                    │    Page Program    │        80h-00h-00h-00h-00h-00h-10h
                    └────────────────────┘
```

Check Status Register

Busy SR[6] = 0

Ready SR[6] = 1

Check Status Register

OTP Exit Command FFh

SR[0] = 1 or SR[3] = 0

SR[0] =0 and SR[3] = 1

OTP Exit Command FFh

Failed

Protected

2.4   OTP Read Status Sequence Flow Chart

At any given time, the host controller may want to check the OTP lock status. The sequence below highlights the different steps necessary. A dummy program operation (data=FFh or no data) must be performed prior to reading the status SR[3] register setting. Indeed such operation is used to determine whether the OTP is locked.

```
                          ┌──────────┐
                          │   IDLE   │
                          └────┬─────┘
                               │
                               ▼
                        ┌─────────────┐      OTP Entry Sequence
                        │  OTP Entry  │      29h-17h-04h-19h
                        └──────┬──────┘
                               │
                               ▼
                   ┌────────────────────┐    OTP Dummy Write Program Sequence
                   │  OTP Dummy Write   │    80h-00h-00h-00h-00h-00h-data-10h
                   │     Program        │
                   └─────────┬──────────┘
                             │
                  ┌──────────▼──────────┐
          Busy    │       Check         │
          SR[6]=0 │   Status Register   │
                  └──────────┬──────────┘
                             │ Ready SR[6] = 1
                             ▼
  ┌─────────────┐  ┌──────────────────┐  ┌─────────────┐
  │ OTP Exit    │◄─│      Check        │─►│ OTP Exit    │
  │ Command FFh │  │  Status Register  │  │ Command FFh │
  └──────┬──────┘  └──────────────────┘  └──────┬──────┘
         │    SR[3]=0            SR[3]=1         │
         ▼                                       ▼
  ┌─────────────┐                         ┌─────────────┐
  │     OTP     │                         │     OTP     │
  │ Unprotected │                         │  Protected  │
  └─────────────┘                         └─────────────┘
```

3   Related Datasheets

- 1Gb – 8Gb 3.0V (ML-1) High Reliability, SLC NAND Flash Memory
  http://www.cypress.com/products/1gb-8gb-30v-ml-1-high-reliability-slc-nand-flash-memory

- 1Gb – 16Gb 3.0V (ML-2) High Reliability, SLC NAND Flash Memory
  http://www.cypress.com/products/1gb-16gb-30v-ml-2-high-reliability-slc-nand-flash-memory

- 1Gb – 4Gb 1.8V (MS-1) High Reliability, SLC NAND Flash Memory
  http://www.cypress.com/products/1gb-4gb-18v-ms-1-high-reliability-slc-nand-flash-memory

- 1Gb – 16 Gb 1.8V (MS-2) High Reliability, SLC NAND Flash Memory
  http://www.cypress.com/products/1gb-16-gb-18v-ms-2-high-reliability-slc-nand-flash-memory

- 1Gb – 4Gb 3.0V (SL) High Security, SLC NAND Flash Memory
  http://www.cypress.com/products/1gb-4gb-30v-sl-high-security-slc-nand-flash-memory

- e.MMC Managed NAND Flash Memory
  http://www.cypress.com/products/emmc-managed-nand-flash-memory

Document History

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**	5046620	XILA	12/21/2015	New Spec.
*A	5216255	MOH	04/14/2016	2.4: Added Section describing how to read the OTP status at any time.

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