Power Supply

If you are in a critical loop, whether it be controlling machinery, or writing internal EEPROM, power supply and UP have to handle detection and orderly termination of processing threads upon loss of power. Some points –

1) Use LVD to alert UP there is an imminent loss of power about to occur. Process that interrupt to create an orderly shutdown. Point of pickoff for LVD is also of consideration, closer to the energy source generally better control and maximization over power loss. If external LVD is desired then use A/D converter as LVD device. But also potentially presents circuit design problems associated with pin injection current limitations, eg. when power is absent on PSOC, but coming up on LVD sense node. A simple resistor in series with input may resolve that issue.

2) LVD alone is not enough, some processes need time during a loss of power to complete. That's where short term energy storage is critical, eg. electrolytics, bulk caps, battery…..

3) Circuit design, make sure energy cap does not supply energy back to line or regulator by diode
isolation. Schottky preferred (switched power MOSFET best) where possible due to lower Vf,
less wasted Pdiss, and allows greater V compliance range in design.

4) To compute cap size needed ( this is an approximation, assuming load looks like a constant current source, in reality load typically resistive so one would use exponentials to calculate. UP looks like a constant I load due to CV**2 x f Pdiss, whereas loads, like LEDs with I limiting resistors, look more resistive ) -

Q = C x V, I = C x dV / dT, C = ( I x dT ) / dV, dT = ( C x dV ) / I

I is max current needed

dT is time needed to complete processor thread completion, like EEPROM write as an example

dV is allowed voltage drop to insure UP stays within operation specs, basically ( Vloss_of_power_detect – Vupmin )

All computations have to take worst case values to insure C min is computed, over V and T. Stated another way as C and dV go up, I down, we maximize time UP allowed to continue running on loss of power. So we can use LVD to shut down processes using power, like LED display driving as an example, shut off high speed clks to modules like PWM, counters, etc. to lower I needed. Then finish orderly shutdown. Obviously you shutdown critical processes, like ones controlling safety for humans, ticks, bugs,etc.. first……☺

5) A typical calculation (29466, nominal values, you would need to worst case the example values) –

a. Assume 12 Mhz clock, this allows PSOC to operate over 3.0 V to 5.25 V, assume Vdd nominal
   Is 5V, +/- 5%. You could use LVD to switch clock down from 24 Mhz to 12 Mhz to take advantage
   of wider operating Vdd range while optimizing speed when normal power in effect.

Choose LVDlow_trip = 4.64 V, this is a warning power is about to fail, so dV = 4.64 – 3.00 = 1.64V.

Sum total current required, note PSOC specs show UP core current separate from modules current, so you need to sum all the currents. Also PSOC currents speced as tytpicals, so you will need to use a "fudge" factor scale them up. Or characterize design at temp extremes to get a value with confidence.

So I = ( Iup + Imodules ) xFfudge, lets choose 50 mA as an example, fudge factor 2 x, so I = 100 mA,. Again you will have to worst case this as best as you can.

Lastly assume our main problem is writing EEPROM, we want to write one block with confidence just as power is failing. 200 mS is max needed. Also we need to add some code execution time for rest of orderly shutdown, say 50 mS. Then dT = .25 secs

Equation is Amps, Volts, Farads

So we have (nominals) C = ( .1 x .25 ) / 1.64 = ~ .015 Farads, or 15,000 uF. Electrolytic tolerances quite poor, very temp dependant, so factor this in to value needed.

[url]http://www.cde.com/catalogs/AEappGUIDE.pdf[/url]

Lastly this capacitor has to be charged on power recovery, so use defining equations and estimates of available current to restore capacitance charge, in consideration of startup power supply slew rates. Also protect
regulator outputs from discharging this capacitance with a diode or switched MOSFET in series with regulator
output. Note its voltage drop factors into calculations. Spice useful to get a handle on overall supply design.
The capacitor can be on the input or output side of your regulator, certain advantages and considerations for either topology.

Additionally more energy may be available stored in transformer fields. Spice good for estimating this behavior.

Reminder you have to worst case all values over T and V for a successful/reliable design. And don't forget component aging effects.

Regards, Dana.