PSoC 4100/4200 Family

PSoC® 4 Registers TRM
(Technical Reference Manual)

Spec. # 001-85847 Rev. ** April 18, 2013

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Section H: Register Mapping

The Register Mapping section discusses the registers of the PSoC4 device. It lists all the registers in mapping tables, in address order.

Register General Conventions

The register conventions specific to this section and the Register Reference chapter are listed in this table.

Convention	Example	Description
'x' in a register name	ACBxxCR1	Multiple instances/address ranges of the same register
R	R : 00	Read register or bit(s)
W	W : 00	Write register or bit(s)
WOC	WOC:0	Write one to clear
WZC	WZC:0	Write zero to clear
RC	RC:0	Read to clear
WC	WC:0	Write to clear
NA	NA:000	Reserved
U	R:U	Undefined
00	RW : 00	Reset value is 0x00
XX	RW : XX	Register is not reset
Empty, grayed out table cell		Reserved bit or group of bits, unless otherwise stated. Write reserved bits to zero. Software cannot make any assumptions about return values.

1 CM0 Registers

This section discusses the CMO registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

1.1 CM0 Register Mapping Overview

Register Name	Address
CM0_DWT_CTRL	0xE0001000
CM0_DWT_PCSR	0xE000101C
CM0_DWT_COMP0	0xE0001020
CM0_DWT_MASK0	0xE0001024
CM0_DWT_FUNCTION0	0xE0001028
CM0_DWT_COMP1	0xE0001030
CM0_DWT_MASK1	0xE0001034
CM0_DWT_FUNCTION1	0xE0001038
CM0_DWT_PID4	0xE0001FD0
CM0_DWT_PID0	0xE0001FE0
CM0_DWT_PID1	0xE0001FE4
CM0_DWT_PID2	0xE0001FE8
CM0_DWT_PID3	0xE0001FEC
CM0_DWT_CID0	0xE0001FF0
CM0_DWT_CID1	0xE0001FF4
CM0_DWT_CID2	0xE0001FF8
CM0_DWT_CID3	0xE0001FFC
CM0_BP_CTRL	0xE0002000
CM0_BP_COMP0	0xE0002008
CM0_BP_COMP1	0xE000200C
CM0_BP_COMP2	0xE0002010
CM0_BP_COMP3	0xE0002014
CM0_BP_PID4	0xE0002FD0
CM0_BP_PID0	0xE0002FE0
CM0_BP_PID1	0xE0002FE4
CM0_BP_PID2	0xE0002FE8

Register Name	Address
CM0_BP_PID3	0xE0002FEC
CM0_BP_CID0	0xE0002FF0
CM0_BP_CID1	0xE0002FF4
CM0_BP_CID2	0xE0002FF8
CM0_BP_CID3	0xE0002FFC
CM0_ACTLR	0xE000E008
CM0_SYST_CSR	0xE000E010
CM0_SYST_RVR	0xE000E014
CM0_SYST_CVR	0xE000E018
CM0_SYST_CALIB	0xE000E01C
CM0_ISER	0xE000E100
CM0_ICER	0xE000E180
CM0_ISPR	0xE000E200
CM0_ICPR	0xE000E280
CM0_IPR	0xE000E400
CM0_CPUID	0xE000ED00
CM0_ICSR	0xE000ED04
CM0_AIRCR	0xE000ED0C
CM0_SCR	0xE000ED10
CM0_CCR	0xE000ED14
CM0_SHPR2	0xE000ED1C
CM0_SHPR3	0xE000ED20
CM0_SHCSR	0xE000ED24
CM0_DFSR	0xE000ED30
CM0_DHCSR	0xE000EDF0
CM0_DCRSR	0xE000EDF4
CM0_DCRDR	0xE000EDF8
CM0_DEMCR	0xE000EDFC
CM0_SCS_PID4	0xE000EFD0
CM0_SCS_PID0	0xE000EFE0
CM0_SCS_PID1	0xE000EFE4
CM0_SCS_PID2	0xE000EFE8
CM0_SCS_PID3	0xE000EFEC
CM0_SCS_CID0	0xE000EFF0
CM0_SCS_CID1	0xE000EFF4
CM0_SCS_CID2	0xE000EFF8
CM0_SCS_CID3	0xE000EFFC
CM0_ROM_SCS	0xE00FF000
CM0_ROM_DWT	0xE00FF004
CM0_ROM_BPU	0xE00FF008

Register Name	Address
CM0_ROM_END	0xE00FF00C
CM0_ROM_CSMT	0xE00FFFCC
CM0_ROM_PID4	0xE00FFFD0
CM0_ROM_PID0	0xE00FFFE0
CM0_ROM_PID1	0xE00FFFE4
CM0_ROM_PID2	0xE00FFFE8
CM0_ROM_PID3	0xE00FFFEC
CM0_ROM_CID0	0xE00FFFF0
CM0_ROM_CID1	0xE00FFFF4
CM0_ROM_CID2	0xE00FFFF8
CM0_ROM_CID3	0xE00FFFFC

1.1.1 CM0_DWT_CTRL

Address: 0xE0001000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x2				None			
HW Access	None				None			
SW Access	R				None			
Bit Name	CM0_NUMCOMP [31:28]				Reserved[27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

Watchpoint Comparator Configuration

Bits	Name	Description
31 : 28	CM0_NUMCOMP	Number of comparators available Default: 0x2

1.1.2 CM0_DWT_PCSR

Address: 0xE000101C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	W							
SW Access	R							
Bit Name	CM0_EIASAMPLE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	W							
SW Access	R							
Bit Name	CM0_EIASAMPLE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	W							
SW Access	R							
Bit Name	CM0_EIASAMPLE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	W							
SW Access	R							
Bit Name	CM0_EIASAMPLE [31: 0]							

Watchpoint Comparator PC Sample

Bits	Name	Description
31 : 0	CM0_EIASAMPLE	Executed Instruction Address sample value Default: 0x00000000

1.1.3 CM0_DWT_COMP0

Address: 0xE0001020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Watchpoint Comparator Compare Value

Bits	Name	Description
31 : 0	CM0_COMP	Reference value for comparison. See The DWT comparators on page C1-341. Default: 0x00000000

1.1.4 CM0_DWT_MASK0

Address: 0xE0001024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Watchpoint Comparator Mask

Bits	Name	Description
31 : 0	CM0_MASK	The size of the ignore mask applied to address range matching. See The DWT comparators on page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. Default: 0x00000000

1.1.5 CM0_DWT_FUNCTION0

Address: 0xE0001028

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							0x0
HW Access	None							RW
SW Access	None							R
Bit Name	Reserved[31:25]							CM0_MATCHED

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				CM0_FUNCTION [3:0]			

Watchpoint Comparator Function

Bits	Name	Description
24	CM0_MATCHED	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0. Default: 0x0
3 : 0	CM0_FUNCTION	Select action on comparator match. Default: 0x0 **0x0: DISABLE** Disabled

1.1.5 CM0_DWT_FUNCTION0 (continued)

0x4: IADDR
PC watchpoint event

0x5: DADDR_RO
Watchpoint event

0x6: DADDR_WO
Watchpoint event

0x7: DADDR_RW
Watchpoint event

1.1.6 CM0_DWT_COMP1

Address: 0xE0001030

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP [31: 0]							

Watchpoint Comparator Compare Value

Bits	Name	Description
31 : 0	CM0_COMP	Reference value for comparison. See The DWT comparators on page C1-341. Default: 0x00000000

1.1.7 CM0_DWT_MASK1

Address: 0xE0001034

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_MASK [31: 0]							

Watchpoint Comparator Mask

Bits	Name	Description
31 : 0	CM0_MASK	The size of the ignore mask applied to address range matching. See The DWT comparators on page C1-341 for the usage model. The mask range is IMPLEMENTATION DEFINED. Writing all ones to this field and reading it back can be used to determine the maximum mask size supported. Default: 0x00000000

1.1.8 CM0_DWT_FUNCTION1

Address: 0xE0001038

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							0x0
HW Access	None							RW
SW Access	None							R
Bit Name	Reserved[31:25]							CM0_MATCHED

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				CM0_FUNCTION [3:0]			

Watchpoint Comparator Function

Bits	Name	Description
24	CM0_MATCHED	Comparator match. It indicates that the operation defined by FUNCTION has occurred since the bit was last read: 0 the associated comparator has matched. 1 the associated comparator has not matched. Reading the register clears this bit to 0. Default: 0x0
3 : 0	CM0_FUNCTION	Select action on comparator match. Default: 0x0 **0x0: DISABLE** Disabled

1.1.8 CM0_DWT_FUNCTION1 (continued)

0x4: IADDR
PC watchpoint event

0x5: DADDR_RO
Watchpoint event

0x6: DADDR_WO
Watchpoint event

0x7: DADDR_RW
Watchpoint event

1.1.9 CM0_DWT_PID4

Address: 0xE0001FD0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Peripheral ID #4

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default: 0x00000004

1.1.10 CM0_DWT_PID0

Address: 0xE0001FE0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Peripheral ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default: 0x0000000A

1.1.11 CM0_DWT_PID1

Address: 0xE0001FE4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Peripheral ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default: 0x000000B0

1.1.12 CM0_DWT_PID2

Address: 0xE0001FE8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Peripheral ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default: 0x0000000B

1.1.13 CM0_DWT_PID3

Address: 0xE0001FEC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Peripheral ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default: 0x00000000

1.1.14 CM0_DWT_CID0

Address: 0xE0001FF0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Component ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default: 0x0000000D

1.1.15 CM0_DWT_CID1

Address: 0xE0001FF4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Component ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default: 0x000000E0

1.1.16 CM0_DWT_CID2

Address: 0xE0001FF8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Component ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default: 0x00000005

1.1.17 CM0_DWT_CID3

Address: 0xE0001FFC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Watchpoint Unit CoreSight ROM Table Component ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default: 0x000000B1

1.1.18 CM0_BP_CTRL

Address: 0xE0002000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x4				None		0x0	0x0
HW Access	None				None		R	R
SW Access	R				None		RW	RW
Bit Name	CM0_NUM_CODE [7:4]				Reserved[3:2]		CM0_KEY	CM0_ENABLE

Breakpoint Unit Control

Bits	Name	Description
7 : 4	CM0_NUM_CODE	The number of breakpoint comparators. If NUM_CODE is zero, the implementation does not support any comparators. Default: 0x4
1	CM0_KEY	RAZ on reads, SBO for writes. If written as zero, the write to the register is ignored. Default: 0x0
0	CM0_ENABLE	Enables the BPU: 0 BPU is disabled. 1 BPU is enabled. Default: 0x0

1.1.19 CM0_BP_COMP0

Address: 0xE0002008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None	0x0000000				
HW Access	R		None	R				
SW Access	RW		None	RW				
Bit Name	CM0_MATCH [31:30]		Reserved	CM0_COMP_ADDR [28:2]				

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000000						None	0x0
HW Access	R						None	R
SW Access	RW						None	RW
Bit Name	CM0_COMP_ADDR [28: 2]						Reserved	CM0_ENABLE

Breakpoint Compare Register

Bits	Name	Description
31 : 30	CM0_MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default: 0x0 **0x0: NONE** No breakpoint matching **0x1: LOWER** Breakpoint on lower halfword, upper is unaffected. **0x2: UPPER** Breakpoint on upper halfword, lower is unaffected.

1.1.19 CM0_BP_COMP0 (continued)

		0x3: BOTH Breakpoint on both lower and upper halfwords.
28 : 2	CM0_COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default: 0x0000000
0	CM0_ENABLE	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default: 0x0

1.1.20 CM0_BP_COMP1

Address: 0xE000200C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None	0x0000000				
HW Access	R		None	R				
SW Access	RW		None	RW				
Bit Name	CM0_MATCH [31:30]		Reserved	CM0_COMP_ADDR [28:2]				

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000000						None	0x0
HW Access	R						None	R
SW Access	RW						None	RW
Bit Name	CM0_COMP_ADDR [28: 2]						Reserved	CM0_ENABLE

Breakpoint Compare Register

Bits	Name	Description
31 : 30	CM0_MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default: 0x0 **0x0: NONE** No breakpoint matching **0x1: LOWER** Breakpoint on lower halfword, upper is unaffected. **0x2: UPPER** Breakpoint on upper halfword, lower is unaffected.

1.1.20 CM0_BP_COMP1 (continued)

		0x3: BOTH Breakpoint on both lower and upper halfwords.
28 : 2	CM0_COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default: 0x0000000
0	CM0_ENABLE	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default: 0x0

1.1.21 CM0_BP_COMP2

Address: 0xE0002010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None	0x0000000				
HW Access	R		None	R				
SW Access	RW		None	RW				
Bit Name	CM0_MATCH [31:30]		Reserved	CM0_COMP_ADDR [28:2]				

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000000						None	0x0
HW Access	R						None	R
SW Access	RW						None	RW
Bit Name	CM0_COMP_ADDR [28: 2]						Reserved	CM0_ENABLE

Breakpoint Compare Register

Bits	Name	Description
31 : 30	CM0_MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default: 0x0 **0x0: NONE** No breakpoint matching **0x1: LOWER** Breakpoint on lower halfword, upper is unaffected. **0x2: UPPER** Breakpoint on upper halfword, lower is unaffected.

1.1.21 CM0_BP_COMP2 (continued)

		0x3: BOTH Breakpoint on both lower and upper halfwords.
28 : 2	CM0_COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default: 0x0000000
0	CM0_ENABLE	Enables the comparator: Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default: 0x0

1.1.22 CM0_BP_COMP3

Address: 0xE0002014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None	0x0000000				
HW Access	R		None	R				
SW Access	RW		None	RW				
Bit Name	CM0_MATCH [31:30]		Reserved	CM0_COMP_ADDR [28:2]				

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_COMP_ADDR [28: 2]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000000						None	0x0
HW Access	R						None	R
SW Access	RW						None	RW
Bit Name	CM0_COMP_ADDR [28: 2]						Reserved	CM0_ENABLE

Breakpoint Compare Register

Bits	Name	Description
31 : 30	CM0_MATCH	BP_MATCH defines the behavior when the COMP address is matched. Default: 0x0 **0x0: NONE** No breakpoint matching **0x1: LOWER** Breakpoint on lower halfword, upper is unaffected. **0x2: UPPER** Breakpoint on upper halfword, lower is unaffected.

1.1.22 CM0_BP_COMP3 (continued)

		0x3: BOTH Breakpoint on both lower and upper halfwords.
28 : 2	CM0_COMP_ADDR	Stores bits [28:2] of the comparison address. The comparison address is compared with the address from the Code memory region. Bits [31:29] and [1:0] of the comparison address are zero. Default: 0x0000000
0	CM0_ENABLE	Enables the comparator. Note BP_CTRL.ENABLE must also be set to 1 to enable a comparator. Default: 0x0

1.1.23 CM0_BP_PID4

Address: 0xE0002FD0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Peripheral ID #4

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default: 0x00000004

1.1.24 CM0_BP_PID0

Address: 0xE0002FE0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Peripheral ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default: 0x0000000B

1.1.25 CM0_BP_PID1

Address: 0xE0002FE4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Peripheral ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default: 0x000000B0

1.1.26 CM0_BP_PID2

Address: 0xE0002FE8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Peripheral ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default: 0x0000000B

1.1.27 CM0_BP_PID3

Address: 0xE0002FEC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Peripheral ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default: 0x00000000

1.1.28 CM0_BP_CID0

Address: 0xE0002FF0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Component ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default: 0x0000000D

1.1.29 CM0_BP_CID1

Address: 0xE0002FF4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Component ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default: 0x000000E0

1.1.30 CM0_BP_CID2

Address: 0xE0002FF8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Component ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default: 0x00000005

1.1.31 CM0_BP_CID3

Address: 0xE0002FFC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Breakpoint Unit CoreSight ROM Table Component ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default: 0x000000B1

1.1.32 CM0_ACTLR

Address: 0xE000E008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_ACTRL [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_ACTRL [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_ACTRL [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_ACTRL [31: 0]							

Auxiliary Control Register

Bits	Name	Description
31 : 0	CM0_ACTRL	Always 0 for CM0r0p0 Default: 0x00000000

1.1.33 CM0_SYST_CSR

Address: 0xE000E010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							RW
SW Access	None							R
Bit Name	Reserved[23:17]							CM0_COUNTFLAG

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[7:3]					CM0_CLKSOURCE	CM0_TICKINT	CM0_ENABLE

Systick Control Status

Bits	Name	Description
16	CM0_COUNTFLAG	Indicates whether the counter has counted to 0 since the last read of this register: 0 timer has not counted to 0. 1 timer has counted to 0. COUNTFLAG is set to 1 by a count transition from 1 to 0. COUNTFLAG is cleared to 0 by a read of this register, and by any write to the Current Value register. Default: 0x0

1.1.33 CM0_SYST_CSR (continued)

2	CM0_CLKSOURCE	Indicates the SysTick clock source: 0 SysTick uses the optional external reference clock. 1 SysTick uses the processor clock. If no external clock is provided, this bit reads as one and ignores writes. Default: 0x0
1	CM0_TICKINT	Indicates whether counting to 0 causes the status of the SysTick exception to change to pending: 0 count to 0 does not affect the SysTick exception status. 1 count to 0 changes the SysTick exception status to pending. Changing the value of the counter to 0 by writing zero to the SysTick Current Value register to 0 never changes the status of the SysTick exception. Default: 0x0
0	CM0_ENABLE	Indicates the enabled status of the SysTick counter: 0 counter is disabled. 1 counter is operating. Default: 0x0

1.1.34 CM0_SYST_RVR

Address: 0xE000E014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_RELOAD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_RELOAD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_RELOAD [23: 0]							

Systick Reload Value

Bits	Name	Description
23 : 0	CM0_RELOAD	The value to load into the SYST_CVR register when the counter reaches 0. Default: 0x000000

1.1.35 CM0_SYST_CVR

Address: 0xE000E018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_CURRENT [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_CURRENT [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_CURRENT [23: 0]							

SysTick Current Value

Bits	Name	Description
23 : 0	CM0_CURRENT	Current counter value. This is the value of the counter at the time it is sampled. Default: 0x000000

1.1.36 CM0_SYST_CALIB

Address: 0xE000E01C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	None	RW	None					
SW Access	R	R	None					
Bit Name	CM0_NOREF	CM0_SKEW	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	RW							
SW Access	R							
Bit Name	CM0_TENMS [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	RW							
SW Access	R							
Bit Name	CM0_TENMS [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	RW							
SW Access	R							
Bit Name	CM0_TENMS [23: 0]							

SysTick Calibration Value

Bits	Name	Description
31	CM0_NOREF	Indicates whether the IMPLEMENTATION DEFINED reference clock is provided: 0 the reference clock is implemented. 1 the reference clock is not implemented. When this bit is 1, the CLKSOURCE bit of the SYST_CSR register is forced to 1 and cannot be cleared to 0. Default: 0x0
30	CM0_SKEW	Indicates whether the 10ms calibration value is exact: 0 10ms calibration value is exact. 1 10ms calibration value is inexact, because of the clock frequency. Default: 0x0

1.1.36 CM0_SYST_CALIB (continued)

23 : 0	CM0_TENMS	Optionally, holds a reload value to be used for 10ms (100Hz) timing, subject to system clock skew errors. If this field is zero, the calibration value is not known. Default: 0x000000

1.1.37 CM0_ISER

Address: 0xE000E100

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETENA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETENA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETENA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETENA [31: 0]							

Interrupt Set-Enable Register

Bits	Name	Description
31 : 0	CM0_SETENA	Enables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default: 0x00000000

1.1.38 CM0_ICER

Address: 0xE000E180

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRENA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRENA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRENA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRENA [31: 0]							

Interrupt Clear Enable Register

Bits	Name	Description
31 : 0	CM0_CLRENA	Disables, or reads the enabled state of one or more interrupts. Each bit corresponds to the same numbered interrupt. Default: 0x00000000

1.1.39 CM0_ISPR

Address: 0xE000E200

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETPEND [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETPEND [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETPEND [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1S							
Bit Name	CM0_SETPEND [31: 0]							

Interrupt Set-Pending Register

Bits	Name	Description
31 : 0	CM0_SETPEND	Changes the state of one or more interrupts to pending. Each bit corresponds to the same numbered interrupt. Default: 0x00000000

1.1.40 CM0_ICPR

Address: 0xE000E280

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRPEND [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRPEND [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRPEND [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW1C							
Bit Name	CM0_CLRPEND [31: 0]							

Interrupt Clear-Pending Register

Bits	Name	Description
31 : 0	CM0_CLRPEND	Changes the state of one or more interrupts to not pending. Each bit corresponds to the same numbered interrupt. Default: 0x00000000

1.1.41 CM0_IPR

Address: 0xE000E400

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_N3 [31:30]		Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_N2 [23:22]		Reserved[21:16]					

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_N1 [15:14]		Reserved[13:8]					

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_N0 [7:6]		Reserved[5:0]					

Interrupt Priority Registers

Bits	Name	Description
31 : 30	CM0_PRI_N3	Priority of interrupt number N+3. Default: 0x0
23 : 22	CM0_PRI_N2	Priority of interrupt number N+2. Default: 0x0
15 : 14	CM0_PRI_N1	Priority of interrupt number N+1. Default: 0x0
7 : 6	CM0_PRI_N0	Priority of interrupt number N. Default: 0x0

1.1.42 CM0_CPUID

Address: 0xE000ED00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00							
HW Access	None							
SW Access	R							
Bit Name	CM0_IMPLEMENTER [31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	R				R			
Bit Name	CM0_VARIANT [23:20]				CM0_CONSTANT [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000							
HW Access	None							
SW Access	R							
Bit Name	CM0_PARTNO [15:4]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000				0x0			
HW Access	None				None			
SW Access	R				R			
Bit Name	CM0_PARTNO [15: 4]				CM0_REVISION [3:0]			

CPUID Register

Bits	Name	Description
31 : 24	CM0_IMPLEMENTER	Implementer code for ARM. Default: 0x41
23 : 20	CM0_VARIANT	Implementation defined. In ARM implementations this is the major revision number n in the rn part of the rnpn revision status, Product revision status on page xii. Default: 0x0
19 : 16	CM0_CONSTANT	Indicates the architecture, ARMv6-M Default: 0xC
15 : 4	CM0_PARTNO	Indicates part number, Cortex-M0 Default: 0xC20
3 : 0	CM0_REVISION	Indicates revision. In ARM implementations this is the minor revision number n in the pn part of the rnpn revision status, see Product revision status on page xii. For release r0p0. Default: 0x0

1.1.43 CM0_ICSR

Address: 0xE000ED04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None		0x0	0x0	0x0	0x0	None
HW Access	RW	None		RW	R	RW	R	None
SW Access	RW1S	None		RW1S	RW1C	RW1S	RW1C	None
Bit Name	CM0_NMIPENDSET	Reserved[30:29]		CM0_PENDSVSET	CM0_PENDSVCLR	CM0_PENDSTSETb	CM0_PENDSTCLR	Reserved

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	None	0x000				
HW Access	RW	RW	None	RW				
SW Access	R	R	None	R				
Bit Name	CM0_ISRPREEMPT	CM0_ISRPENDING	Reserved	CM0_VECTPENDING [20:12]				

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000				None			0x000
HW Access	RW				None			RW
SW Access	R				None			R
Bit Name	CM0_VECTPENDING [20: 12]				Reserved[11:9]			CM0_VECTACTIVE [8:0]

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	RW							
SW Access	R							
Bit Name	CM0_VECTACTIVE [8 : 0]							

Interrupt Control State Register

Bits	Name	Description
31	CM0_NMIPENDSET	Activates an NMI exception or reads back the current state. Because NMI is the highest priority exception, it activates as soon as it is registered. Default: 0x0
28	CM0_PENDSVSET	Sets a pending PendSV interrupt or reads back the current state. Use this normally to request a context switch. Writing PENDSVSET and PENDSVCLR to 1 concurrently is UNPREDICT-ABLE. Default: 0x0

1.1.43 CM0_ICSR (continued)

27	CM0_PENDSVCLR	Clears a pending PendSV interrupt. Default: 0x0
26	CM0_PENDSTSETb	Sets a pending SysTick or reads back the current state. Writing PENDSTSET and PENDSTCLR to 1 concurrently is UNPREDICTABLE. Default: 0x0
25	CM0_PENDSTCLR	Clears a pending SysTick, whether set here or by the timer hardware. Default: 0x0
23	CM0_ISRPREEMPT	Indicates whether a pending exception will be serviced on exit from debug halt state. Default: 0x0
22	CM0_ISRPENDING	Indicates if an external configurable, NVIC generated, interrupt is pending. Default: 0x0
20 : 12	CM0_VECTPENDING	The exception number for the highest priority pending exception. 0= No pending exceptions. The pending state includes the effect of memory-mapped enable and mask registers. It does not include the PRIMASK special-purpose register qualifier. Default: 0x000
8 : 0	CM0_VECTACTIVE	The exception number for the current executing exception. 0= Thread mode. This is the same value as IPSR[8:0] Default: 0x000

1.1.44 CM0_AIRCR

Address: 0xE000ED0C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_VECTKEY [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CM0_VECTKEY [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	None						
HW Access	None	None						
SW Access	R	None						
Bit Name	CM0_ENDIANNESS	Reserved[14:8]						

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	None
HW Access	None					R	R	None
SW Access	None					RW1S	RW1C	None
Bit Name	Reserved[7:3]					CM0_SYSRESETREQ	CM0_VECTCL-RACTIVE	Reserved

Application Interrupt and Reset Control Register

Bits	Name	Description
31 : 16	CM0_VECTKEY	Vector Key. The value 0x05FA must be written to this register, otherwise the register write is UNPREDICTABLE. Readback value is UNKNOWN. Default: 0x0000
15	CM0_ENDIANNESS	Indicates the memory system data endianness: 0 little endian 1 big endian. See Endian support on page A3-44 for more information. Default: 0x0

1.1.44 CM0_AIRCR (continued)

2	CM0_SYSRESETREQ	System Reset Request. Writing 1 to this bit asserts a signal to request a reset by the external system. This will cause a full system reset of the CPU and all other components in the device. See Reset management on page B1-240 for more information. Default: 0x0
1	CM0_VECTCLRACTIVE	Clears all active state information for fixed and configurable exceptions. The effect of writing a 1 to this bit if the processor is not halted in Debug state is UNPREDICTABLE. Default: 0x0

1.1.45 CM0_SCR

Address: 0xE000ED10

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None	0x0	0x0	None
HW Access	None			R	None	R	R	None
SW Access	None			RW	None	RW	RW	None
Bit Name	Reserved[7:5]			CM0_SEVONPEND	Reserved	CM0_SLEEPDEEP	CM0_SLEEPONEXIT	Reserved

System Control Register

Bits	Name	Description
4	CM0_SEVONPEND	Determines whether an interrupt transition from inactive state to pending state is a wakeup event: 0: transitions from inactive to pending are not wakeup events. 1: transitions from inactive to pending are wakeup events. See WFE on page A6-197 for more information. Default: 0x0
2	CM0_SLEEPDEEP	An implementation can use this bit to select DeepSleep/Hibernate power modes upon execution of WFI/WFE: 0: Select Sleep mode 1: Select DeepSleep/Hibernate (depends on PWR_CONTROL.HIBERNATE) Default: 0x0

1.1.45 CM0_SCR (continued)

1	CM0_SLEEPONEXIT	Determines whether, on an exit from an ISR that returns to the base level of execution priority, the processor enters a sleep state: 0 do not enter sleep state. 1 enter sleep state. See Power management on page B1-240 for more information. Default: 0x0

1.1.46 CM0_CCR

Address: 0xE000ED14

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x1	None
HW Access	None						None	None
SW Access	None						R	None
Bit Name	Reserved[15:10]						CM0_STKALIGN	Reserved[8:8]

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x1	None		
HW Access	None				None	None		
SW Access	None				R	None		
Bit Name	Reserved[7:4]				CM0_UNALIGN_TRP	Reserved[2:0]		

Configuration and Control Register

Bits	Name	Description
9	CM0_STKALIGN	1: On exception entry, the SP used prior to the exception is adjusted to be 8-byte aligned and the context to restore it is saved. The SP is restored on the associated exception return. Default: 0x1
3	CM0_UNALIGN_TRP	1: unaligned word and halfword accesses generate a HardFault exception. Default: 0x1

1.1.47 CM0_SHPR2

Address: 0xE000ED1C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_11 [31:30]		Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

System Handler Priority Register 2

Bits	Name	Description
31 : 30	CM0_PRI_11	Priority of system handler 11, SVCall Default: 0x0

1.1.48 CM0_SHPR3

Address: 0xE000ED20

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_15 [31:30]		Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	CM0_PRI_14 [23:22]		Reserved[21:16]					

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

System Handler Priority Register 3

Bits	Name	Description
31 : 30	CM0_PRI_15	Priority of system handler 15, SysTick Default: 0x0
23 : 22	CM0_PRI_14	Priority of system handler 14, PendSV Default: 0x0

1.1.49 CM0_SHCSR

Address: 0xE000ED24

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	None						
HW Access	RW	None						
SW Access	RW	None						
Bit Name	CM0_SVCALLPENDED	Reserved[14:8]						

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

System Handler Control and State Register

Bits	Name	Description
15	CM0_SVCALLPENDED	0 SVCall is not pending. 1 SVCall is pending. This bit reflects the pending state on a read, and updates the pending state, to the value written, on a write. (Pending state bits are set to 1 when an exception occurs, and are cleared to 0 when an exception becomes active.) Default: 0x0

1.1.50 CM0_DFSR

Address: 0xE000ED30

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	0x0	0x0	0x0	0x0
HW Access	None			RW1S	RW1S	RW1S	RW1S	RW1S
SW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	Reserved[7:5]			CM0_EXTERNAL	CM0_VCATCH	CM0_DWTTRAP	CM0_BKPT	CM0_HALTED

Debug Fault Status Register

Bits	Name	Description
4	CM0_EXTERNAL	Indicates an asynchronous debug event generated because of EDBGRQ being asserted: 0 no EDBGRQ debug event. 1 EDBGRQ debug event. Default: 0x0
3	CM0_VCATCH	Indicates whether a vector catch debug event was generated: 0 no vector catch debug event generated. 1 vector catch debug event generated. The corresponding FSR shows the primary cause of the exception. Default: 0x0

1.1.50 CM0_DFSR (continued)

2	CM0_DWTTRAP	Indicates a debug event generated by the DWT: 0 no debug events generated by the DWT. 1 at least one debug event generated by the DWT. Default: 0x0
1	CM0_BKPT	Indicates a debug event generated by BKPT instruction execution or a breakpoint match in the BPU: 0 no breakpoint debug event. 1 at least one breakpoint debug event. Default: 0x0
0	CM0_HALTED	Indicates a debug event generated by a C_HALT or C_STEP request, triggered by a write to the DHCSR: 0 no active halt request debug event. 1 halt request debug event active. See Debug Halting Control and Status Register, DHCSR for more information. Default: 0x0

1.1.51 CM0_DHCSR

Address: 0xE000EDF0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00						0x1	0x0
HW Access	R						RW	RW
SW Access	W						R	R
Bit Name	CM0_DBG_KEY_P2 [31:26]						CM0_S_RESET_ST	CM0_S_RETIRE_ST

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0	0x0	0x0	0x0
HW Access	R				RW	RW	RW	RW
SW Access	W				R	R	R	R
Bit Name	CM0_DBG_KEY_P1 [23:20]				CM0_S_LOCKUP	CM0_S_SLEEP	CM0_S_HALT	CM0_S_REGRDY

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				R	R	R	R
SW Access	None				RW	RW	RW	RW
Bit Name	Reserved[7:4]				CM0_C_MASKINTS	CM0_C_STEP	CM0_C_HALT	CM0_C_DEBUGEN

Debug Halting Control and Status Register

Bits	Name	Description
31 : 26	CM0_DBG_KEY_P2	See desciption for Bit 20 Default: 0x00
25	CM0_S_RESET_ST	Indicates whether the processor has been reset since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR Default: 0x1

1.1.51 CM0_DHCSR (continued)

24	CM0_S_RETIRE_ST	When not in Debug state, indicates whether the processor has completed execution of at least one instruction since the last read of DHCSR. This is a sticky bit, that clears to 0 on a read of DHCSR. This bit is UNKNOWN: - after a Local reset, but is set to 1 as soon as the processor completes execution of an instruction - when S_LOCKUP is set to 1 - when S_HALT is set to 1. When the processor is not in Debug state, a debugger can check this bit to determine if the processor is stalled on a load, store or fetch access. Default: 0x0
23 : 20	CM0_DBG_KEY_P1	Debug key: Software must write 0xA05F to [31:16] to enable write accesses to bits [15:0], otherwise the processor ignores the write access. Default: 0x0
19	CM0_S_LOCKUP	Indicates whether the processor is locked up because of an unrecoverable exception. See Unrecoverable exception cases on page B1-238 for more information. This bit can only read as 1 when accessed by a remote debugger using the DAP. The bit clears to 0 when the processor enters Debug state. Default: 0x0
18	CM0_S_SLEEP	Indicates whether the processor is sleeping. The debugger must set the DHCSR.C_HALT bit to 1 to gain control, or wait for an interrupt or other wakeup event to wakeup the system. Default: 0x0
17	CM0_S_HALT	Indicates whether the processor is in Debug state. Default: 0x0
16	CM0_S_REGRDY	A handshake flag for transfers through the DCRDR: - Writing to DCRSR clears the bit to 0. - Completion of the DCRDR transfer then sets the bit to 1. For more information about DCRDR transfers see Debug Core Register Data Register, DCRDR on page C1-337. 0: There has been a write to the DCRDR, but the transfer is not complete. 1: The transfer to or from the DCRDR is complete. This bit is only valid when the processor is in Debug state, otherwise the bit is UNKNOWN. Default: 0x0
3	CM0_C_MASKINTS	When debug is enabled, the debugger can write to this bit to mask PendSV, SysTick and external configurable interrupts. The effect of any attempt to change the value of this bit is UNPREDICTABLE unless both: - before the write to DHCSR, the value of the C_HALT bit is 1 - the write to the DHCSR that changes the C_MASKINTS bit also writes 1 to the C_HALT bit This means that a single write to DHCSR cannot set the C_HALT to 0 and change the value of the C_MASKINTS bit. The bit does not affect NMI. When DHCSR.C_DEBUGEN is set to 0, the value of this bit is UNKNOWN. For more information about the use of this bit see Table C1-7 on page C1-326. Default: 0x0
2	CM0_C_STEP	Processor step bit. The effects of writes to this bit are: 0 Single-stepping disabled. 1 Single-stepping enabled. For more information about the use of this bit see Table C1-7 on page C1-326. Default: 0x0

1.1.51 CM0_DHCSR (continued)

1	CM0_C_HALT	Processor halt bit. The effects of writes to this bit are: 0 Request a halted processor to run. 1 Request a running processor to halt. Table C1-7 on page C1-326 shows the effect of writes to this bit when the processor is in Debug state. Default: 0x0
0	CM0_C_DEBUGEN	Halting debug enable bit. If a debugger writes to DHCSR to change the value of this bit from 0 to 1, it must also write 0 to the C_MASKINTS bit, otherwise behavior is UNPREDICTABLE. This bit can only be written from the DAP. Access to the DHCSR from software running on the processor is IMPLEMENTATION DEFINED. However, writes to this bit from software running on the processor are ignored. Default: 0x0

1.1.52 CM0_DCRSR

Address: 0xE000EDF4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[23:17]							CM0_REGWNR

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			CM0_REGSEL [4:0]				

Debug Core Register Selector Register

Bits	Name	Description
16	CM0_REGWNR	Specifies the type of access for the transfer. Default: 0x0 **0x0: READ** Read transfer **0x1: WRITE** Write transfer
4 : 0	CM0_REGSEL	Specifies the ARM core register or special-purpose register to transfer. Default: 0x00

1.1.52 CM0_DCRSR (continued)

0x00: R0
CPU R0

0x01: R1
CPU R1

0x02: R2
CPU R2

0x03: R3
CPU R3

0x04: R4
CPU R4

0x05: R5
CPU R5

0x06: R6
CPU R6

0x07: R7
CPU R7

0x08: R8
CPU R8

0x09: R9
CPU R9

0x0A: R10
CPU R10

0x0B: R11
CPU R11

0x0C: R12
CPU R12

0x0D: SP
Current Stack Pointer

0x0E: LR
CPU LR

0x0F: DBG_RA
DebugReturnAddress: the address of the first instruction to be executed on exit from Debug state.

1.1.52 CM0_DCRSR (continued)

0x10: XPSR
xPSR

0x11: MSP
Main stack pointer, MSP.

0x12: PSP
Process stack pointer, PSP

0x14: C_P
[31:24]: CONTROL
[7:0]: PRIMASK.

1.1.53 CM0_DCRDR

Address: 0xE000EDF8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	RW							
SW Access	RW							
Bit Name	CM0_DBGTMP [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	RW							
SW Access	RW							
Bit Name	CM0_DBGTMP [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	RW							
SW Access	RW							
Bit Name	CM0_DBGTMP [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	RW							
SW Access	RW							
Bit Name	CM0_DBGTMP [31: 0]							

Debug Core Register Data Register

Bits	Name	Description
31 : 0	CM0_DBGTMP	Data temporary cache, for reading and writing CPU registers. This register is UNKNOWN: - on reset - when DHCSR.S_HALT = 0. - when DHCSR.S_REGRDY = 0 during execution of a DCRSR based transaction that updates the register Default: 0x00000000

1.1.54 CM0_DEMCR

Address: 0xE000EDFC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[31:25]							CM0_DWTENA

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	None	
HW Access	None					R	None	
SW Access	None					RW	None	
Bit Name	Reserved[15:11]					CM0_VC_HARDERR	Reserved[9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[7:1]							CM0_VC_CORERESET

Debug Exception and Monitor Control Register

Bits	Name	Description
24	CM0_DWTENA	Global enable for all features configured and controlled by the DWT unit. When DWTENA is set to 0 DWT registers return UNKNOWN values on reads. In addition, it is IMPLEMENTATION DEFINED whether the processor ignores writes to the DWT while DWTENA is 0. Default: 0x0
10	CM0_VC_HARDERR	Enable halting debug trap on a HardFault exception. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. Default: 0x0

1.1.54 CM0_DEMCR (continued)

0	CM0_VC_CORERESET	Enable Reset Vector Catch. This causes a Local reset to halt a running system. If DHCSR.C_DEBUGEN is set to 0, the processor ignores the value of this bit. Default: 0x0

1.1.55 CM0_SCS_PID4

Address: 0xE000EFD0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Peripheral ID #4

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default: 0x00000004

1.1.56 CM0_SCS_PID0

Address: 0xE000EFE0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Peripheral ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default: 0x00000008

1.1.57 CM0_SCS_PID1

Address: 0xE000EFE4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Peripheral ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default: 0x000000B0

1.1.58 CM0_SCS_PID2

Address: 0xE000EFE8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Peripheral ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default: 0x0000000B

1.1.59 CM0_SCS_PID3

Address: 0xE000EFEC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Peripheral ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default: 0x00000000

1.1.60 CM0_SCS_CID0

Address: 0xE000EFF0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Component ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default: 0x0000000D

1.1.61 CM0_SCS_CID1

Address: 0xE000EFF4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Component ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default: 0x000000E0

1.1.62 CM0_SCS_CID2

Address: 0xE000EFF8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Component ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default: 0x00000005

1.1.63 CM0_SCS_CID3

Address: 0xE000EFFC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

System Control Space ROM Table Component ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default: 0x000000B1

1.1.64 CM0_ROM_SCS

Address: 0xE00FF000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral #0

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to SCS ROM Table Default: 0xFFF0F003

1.1.65 CM0_ROM_DWT

Address: 0xE00FF004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral #1

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to DWT ROM Table Default: 0xFFF02003

1.1.66 CM0_ROM_BPU

Address: 0xE00FF008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral #2

Bits	Name	Description
31 : 0	CM0_VALUE	Offset to BPU ROM Table Default: 0xFFF03003

1.1.67 CM0_ROM_END

Address: 0xE00FF00C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table End Marker

Bits	Name	Description
31 : 0	CM0_VALUE	End marker in peripheral list Default: 0x00000000

1.1.68 CM0_ROM_CSMT

Address: 0xE00FFFCC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000001							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000001							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000001							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000001							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Memory Type

Bits	Name	Description
31 : 0	CM0_VALUE	Memory Type Default: 0x00000001

1.1.69 CM0_ROM_PID4

Address: 0xE00FFFD0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral ID #4

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #4 Default: 0x00000004

1.1.70 CM0_ROM_PID0

Address: 0xE00FFFE0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #0 Default: 0x00000071

1.1.71 CM0_ROM_PID1

Address: 0xE00FFFE4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #1 Default: 0x000000B4

1.1.72 CM0_ROM_PID2

Address: 0xE00FFFE8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #2 Default: 0x0000000B

1.1.73 CM0_ROM_PID3

Address: 0xE00FFFEC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Peripheral ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Peripheral ID #3 Default: 0x00000000

1.1.74 CM0_ROM_CID0

Address: 0xE00FFFF0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Component ID #0

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #0 Default: 0x0000000D

1.1.75 CM0_ROM_CID1

Address: 0xE00FFFF4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Component ID #1

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #1 Default: 0x00000010

1.1.76 CM0_ROM_CID2

Address: 0xE00FFFF8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Component ID #2

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #2 Default: 0x00000005

1.1.77 CM0_ROM_CID3

Address: 0xE00FFFFC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	R							
Bit Name	CM0_VALUE [31: 0]							

CM0 CoreSight ROM Table Component ID #3

Bits	Name	Description
31 : 0	CM0_VALUE	Component ID #3 Default: 0x000000B1

2 CPUSS Registers

This section discusses the CPUSS registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

2.1 CPUSS Register Mapping Overview

Register Name	Address
CPUSS_CONFIG	0x40000000
CPUSS_SYSREQ	0x40000004
CPUSS_SYSARG	0x40000008
CPUSS_PROTECTION	0x4000000C
CPUSS_PRIV_ROM	0x40000010
CPUSS_PRIV_RAM	0x40000014
CPUSS_PRIV_FLASH	0x40000018
CPUSS_WOUNDING	0x4000001C
CPUSS_INTR_SELECT	0x40000020
CPUSS_BIST_CONTROL	0x40000024
CPUSS_BIST_DATA	0x40000028
CPUSS_DFT	0x4000002C

2.1.1 CPUSS_CONFIG

Address: 0x40000000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[7:2]						CPUSS_FLSH_ACC_BYPASS	CPUSS_VECS_IN_RAM

CPU Subsystem Configuration

Bits	Name	Description
1	CPUSS_FLSH_ACC_BYPASS	0: Normal operation 1: Flash Accellerator in bypass mode, functions as single 64b line buffer. Default: 0x0
0	CPUSS_VECS_IN_RAM	0: Vector Table is located at 0000_0000 in Flash 1: Vector Table is located at 2000_0000 in RAM Note that vectors for RESET and FAULT are always fetched from ROM. Value in Flash/RAM is ignored for these vectores. Default: 0x0

2.1.2 CPUSS_SYSREQ

Address: 0x40000004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x1	0x1	0x0	None		
HW Access	R	RW	RW	R	R	None		
SW Access	RW	R	R	RW	RW	None		
Bit Name	CPUSS_SYSREQ	CPUSS_HMASTER	CPUSS_ROM_ACCESS_EN	CPUSS_PRIVILEGED	CPUSS_NO_RST_OVR	Reserved[26:24]		

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_COMMAND [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_COMMAND [15: 0]							

System Request Register

Bits	Name	Description
31	CPUSS_SYSREQ	Firmware/ATE writes 1 to request a system call. This will lead to an immediate NMI (non maskable interrupt). System call implementation will write 0 after servicing the request. Default: 0x0
30	CPUSS_HMASTER	0: Request was made by Cortex-M0 CPU firmware 1: Request was made by external debugger/ATE probe Note that any writes to this register while SYSREQ=1 will not change the value of HMASTER (such that the origin of a request can continue to be observed). Default: 0x0
29	CPUSS_ROM_ACCESS_EN	Indicates that access to ROM is currently enabled. This bit is used for debug purposes only. Default: 0x1

2.1.2 CPUSS_SYSREQ (continued)

28	CPUSS_PRIVILEGED	Indicates whether the system is in privileged or user mode. This bit can only be set from ROM code. Any write to this register that is not originating from ROM will result in clearing this bit. Default: 0x1
27	CPUSS_NO_RST_OVR	Disable Reset Vector fetch relocation: 0: CPU requests to locations 0000_0000 - 0000_0007 are redirected to SROM 1: CPU requests to locations 0000_0000 - 0000_0007 are made to flash. Note that this bit defaults to 0 on reset, ensuring actual reset vector fetches are always made to ROM Flash DFT routines may set this bit to 1 to enable uninhibited read-back of programmed data in the first flash page. Default: 0x0
15 : 0	CPUSS_COMMAND	Opcode of the system call being requested. Default: 0x0000

2.1.3 CPUSS_SYSARG

Address: 0x40000008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_ARG32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_ARG32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_ARG32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_ARG32 [31: 0]							

System Request Argument Register

Bits	Name	Description
31 : 0	CPUSS_ARG32	Argument to System Call specified in SYSREQ. Semantics of argument depends on system call made. Typically a pointer to a parameter block. Default: 0x00000000

2.1.4 CPUSS_PROTECTION

Address: 0x4000000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW1S	None						
Bit Name	CPUSS_PROT_LOCK	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				CPUSS_PROT [3:0]			

Protection Register

Bits	Name	Description
31	CPUSS_PROT_LOCK	Setting this field will block (ignore) any further writes to the PROT field in this register. Once set, this field cannot be cleared. Default: 0x0
3 : 0	CPUSS_PROT	Current protection mode - this field is available as a global signal everywhere in the system. Writes to this field are ignored when PROT_LOCK=1. Default: 0xF **0x0: VIRGIN** 0000: VIRGIN **0x1: OPEN** 0001: OPEN

2.1.4 CPUSS_PROTECTION (continued)

0x2: PROTECTED
001X: PROTECTED

0x4: KILL
01XX: KILL

0x8: BOOT
1XXX: BOOT

2.1.5 CPUSS_PRIV_ROM

Address: 0x40000010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_ROM_LIMIT [7:0]							

Privileged Limit Register

Bits	Name	Description
7 : 0	CPUSS_ROM_LIMIT	Indicates the limit where the privileged area of ROM starts in increments of 256B. 0: Entire ROM is Privileged 1: First 256B are UserMode accessiable ... Any number larger than the size of the ROM indicates that the entire ROM is user mode accessible. Default: 0x00

2.1.6 CPUSS_PRIV_RAM

Address: 0x40000014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x000
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[15:9]							CPUSS_RAM_LIMIT [8:0]

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_LIMIT [8 : 0]							

Privileged Limit Register

Bits	Name	Description
8 : 0	CPUSS_RAM_LIMIT	Indicates the limit where the privileged area of SRAM starts in increments of 256B. 0: Entire SRAM is Privileged 1: First 256B are UserMode accessiable ... Any number larger than the size of the RAM indicates that the entire ROM is user mode accessible. Default: 0x000

2.1.7 CPUSS_PRIV_FLASH

Address: 0x40000018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x000		
HW Access	None					R		
SW Access	None					RW		
Bit Name	Reserved[15:11]					CPUSS_FLASH_LIMIT [10:0]		

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_FLASH_LIMIT [10 : 0]							

Privileged Limit Register

Bits	Name	Description
10 : 0	CPUSS_FLASH_LIMIT	Indicates the limit where the privileged area of FLASH starts in increments of 256B. 0: Entire FLASH is Privileged 1: First 256B are UserMode accessiable ... Any number larger than the size of the FLASH indicates that the entire Flash is user mode accessible. Note that SuperVisory rows are always Privileged. If FLASH_LIMIT defines a non-empty privileged area, the boot ROM will assume that a system call table exists at the beginning of the Flash privileged area and use it for all SystemCalls made using CPUSS_SYSREQ. Note that marking the entire flash as Privileged will generally not work, since all system calls return to User mode before returning (and they would not be able to return to anything in Flash if it was entirely Privileged). Default: 0x000

2.1.8 CPUSS_WOUNDING

Address: 0x4000001C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None	0x0			None	0x0		
HW Access	None	R			None	R		
SW Access	None	RW1S			None	RW1S		
Bit Name	Reserved	CPUSS_FLASH_WOUND [22:20]			Reserved	CPUSS_RAM_WOUND [18:16]		

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x000
HW Access	None							RW
SW Access	None							R
Bit Name	Reserved[15:9]							CPUSS_RAM_SIZE [8:0]

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	RW							
SW Access	R							
Bit Name	CPUSS_RAM_SIZE [8 : 0]							

Wounding Control Register

Bits	Name	Description
22 : 20	CPUSS_FLASH_WOUND	Indicates the amount of accessible Flash in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of RAM is not accessible and will return bus error when accessed (HRESP=1). Default: 0x0 **0x0: FULL** Entire Flash accessible **0x1: DIV_BY_2** 1/2 of Flash accessible

2.1.8 CPUSS_WOUNDING (continued)

		0x2: DIV_BY_4 1/4th of Flash accessible **0x3: DIV_BY_8** 1/8th of Flash accessible **0x4: DIV_BY_16** 1/16th of Flash accessible **0x5: DIV_BY_32** 1/32th of Flash accessible **0x6: DIV_BY_64** 1/64th of Flash accessible **0x7: DIV_BY_128** 1/128th of Flash accessible
18 : 16	CPUSS_RAM_WOUND	Indicates the amount of accessible RAM in this part. The value in this field is effectively write-once (it is only possible to set bits, not clear them). The remainder portion of RAM is not accessible and will return bus error when accessed (HRESP=1). Default: 0x0 **0x0: FULL** Entire RAM accessible **0x1: DIV_BY_2** 1/2 of RAM accessible **0x2: DIV_BY_4** 1/4th of RAM accessible **0x3: DIV_BY_8** 1/8th of RAM accessible **0x4: DIV_BY_16** 1/16th of RAM accessible **0x5: DIV_BY_32** 1/32th of RAM accessible **0x6: DIV_BY_64** 1/64th of RAM accessible **0x7: DIV_BY_128** 1/128th of RAM accessible
8 : 0	CPUSS_RAM_SIZE	Indicates size of RAM in this device in units of 256B (0: 0B, 1: 256B, 2: 512B ...) Default: 0x000

2.1.9 CPUSS_INTR_SELECT

Address: 0x40000020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_SELECT32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_SELECT32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_SELECT32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_SELECT32 [31: 0]							

Interrupt Multiplexer Select Register

Bits	Name	Description
31 : 0	CPUSS_SELECT32	When bitlt;Ngt; is set, NVIC IRQlt;Ngt; is connected to DSI. When cleared it is connected to its fixed function role as defined in SAS/PAS. Default: 0x00000000

2.1.10 CPUSS_BIST_CONTROL

Address: 0x40000024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	
HW Access	RW0C	RW	RW0C	RW	R	R	R	
SW Access	RW1S	R	RW1S	R	RW	RW	RW	
Bit Name	CPUSS_ROM_GO	CPUSS_ROM_FAIL	CPUSS_RAM_GO	CPUSS_RAM_FAIL	CPUSS_RAM_WORD	CPUSS_RAM_PREADR	CPUSS_RAM_OPCNT [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0		0x0		0x0		0x0	
HW Access	R		R		R		R	
SW Access	RW		RW		RW		RW	
Bit Name	CPUSS_RAM_OP4 [23:22]		CPUSS_RAM_OP3 [21:20]		CPUSS_RAM_OP2 [19:18]		CPUSS_RAM_OP1 [17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_ADDR [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_ADDR [15: 0]							

BIST Control Register

Bits	Name	Description
31	CPUSS_ROM_GO	Firmare/Probe sets this field to start ROM BIST. When ROM bist is executing in hardware, the ROM does not respond properly to requests from the AHB bus and any accesses to ROM by CPU or Probe are not allowed and will have an unpredictable result. Default: 0x0
30	CPUSS_ROM_FAIL	Indicats pass/fail of the SROM BIST. This value is valid only when ROM_GO=0. 0: ROM BIST succeeded 1: ROM BIST failed Default: 0x0

2.1.10 CPUSS_BIST_CONTROL (continued)

29	CPUSS_RAM_GO	Firmare/Probe sets this field to start a SRAM BIST access sequence to a single RAM location. When RAM bist is executing in hardware, the RAM is disconnected from the AHB bus and any accesses to SRAM by CPU or Probe will find the AHB HREADY signal de-asserted. Default: 0x0
28	CPUSS_RAM_FAIL	Indicates pass/fail of the SRAM operation sequence. If any of the read operations in the BIST sequence fail, this bit will be asserted. This bit is valid only when RAM_GO=0 Default: 0x0
27	CPUSS_RAM_WORD	0: Single byte location access to RAM 1: Word access to RAM (32b) Default: 0x0
26	CPUSS_RAM_PREADR	0: Execute sequence as specified 1: In cycle before RAM_OP1 read data (without comparing) from ~RAM_ADDR Default: 0x0
25 : 24	CPUSS_RAM_OPCNT	Number of RAM operations to execute when fired using RAM_GO. 0: only execute RAM_OP1 (opt plus PREADDR) 1: execute RAM_OP1, RAM_OP2 (opt plus PREADDR) 2: execute RAM_OP1, RAM_OP2, RAM_OP3 (opt plus PREADDR) 3: execute RAM_OP1, RAM_OP2, RAM_OP3, RAM_OP4 (opt plus PREADDR) Default: 0x0
23 : 22	CPUSS_RAM_OP4	Fourth RAM Bist operation 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
21 : 20	CPUSS_RAM_OP3	Third RAM Bist operation 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
19 : 18	CPUSS_RAM_OP2	Second RAM Bist operation 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
17 : 16	CPUSS_RAM_OP1	First RAM Bist operation 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
15 : 0	CPUSS_RAM_ADDR	Byte location address for RAM BIST sequence. When RAM_WORD=1 the 2 lsbs are ignored. Default: 0x0000

2.1.11 CPUSS_BIST_DATA

Address: 0x40000028

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_DATA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_DATA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_DATA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	CPUSS_RAM_DATA [31: 0]							

BIST Data Register

Bits	Name	Description
31 : 0	CPUSS_RAM_DATA	Data pattern for BIST sequence. If RAM_WORD=0, only bits [7:0] are used. Default: 0x00000000

2.1.12 CPUSS_DFT

Address: 0x4000002C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[7:3]					CPUSS_RAM_PD	CPUSS_ROM_PD	CPUSS_FLASH_PD

DFT Select Register

Bits	Name	Description
2	CPUSS_RAM_PD	Forcibly powers down system SRAM macro(s) periphery logic when set and TEST_MODE is active. Memory array is connected to Vcchib and cannot be powered down. Default: 0x0
1	CPUSS_ROM_PD	Forcibly powers down system ROM macro(s) when set and TEST_MODE is active. Default: 0x0
0	CPUSS_FLASH_PD	Forcibly powers down Flash macro(s) when set and TEST_MODE is active. Default: 0x0

3 CSD Registers

This section discusses the CSD registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

3.1 CSD Register Mapping Overview

Register Name	Address
CSD_ID	0x40080000
CSD_CONFIG	0x40080004
CSD_IDAC	0x40080008
CSD_COUNTER	0x4008000C
CSD_STATUS	0x40080010
CSD_INTR	0x40080014
CSD_INTR_SET	0x40080018
CSD_TRIM1	0x4008FF00
CSD_TRIM2	0x4008FF04

3.1.1 CSD_ID

Address: 0x40080000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	CSD_REVISION [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	CSD_REVISION [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	CSD_ID [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	CSD_ID [15: 0]							

ID Revision Number

Bits	Name	Description
31 : 16	CSD_REVISION	the version number is 0x0001 Default: 0x0001
15 : 0	CSD_ID	the ID of CSD peripheral is 0xE0E1 Default: 0xE0E1

3.1.2 CSD_CONFIG

Address: 0x40080004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	0x0			None	0x0
HW Access	R	R	R	R			None	R
SW Access	RW	RW	RW	RW			None	RW
Bit Name	CSD_ENABLE	CSD_DDFTCOMP	CSD_ADFTEN	CSD_DDFTSEL [28:26]			Reserved	CSD_REFBUF_DRV [24:23]

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	0x1	None	0x0	0x0	0x0	0x0
HW Access	R	R	R	None	R	R	R	R
SW Access	RW	RW	RW	None	RW	RW	RW	RW
Bit Name	CSD_REFBUF_DRV [24: 23]	CSD_SENSE_INSEL	CSD_REBUF_OUTSEL	Reserved	CSD_SENSE_COMP_EN	CSD_MUTUAL_CAP	CSD_POLARITY2	CSD_POLARITY

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x1	0x0		0x0
HW Access	R	R	R	R	R	R		R
SW Access	RW	RW	RW	RW	RW	RW		RW
Bit Name	CSD_COMP_PIN	CSD_COMP_MODE	CSD_REFBUF_EN	CSD_SENSE_EN	CSD_SENSE_COMP_BW	CSD_SHIELD_DELAY [10:9]		CSD_DSI_SENSE_EN

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	None			0x1	0x0
HW Access	R	R	RW1C	None			R	R
SW Access	RW	RW	RW1S	None			RW	RW
Bit Name	CSD_PRS_12_8	CSD_PRS_SELECT	CSD_PRS_CLEAR	Reserved[4:2]			CSD_SAMPLE_SYNC	CSD_DSI_SAMPLE_EN

Configuration and Control

Bits	Name	Description
31	CSD_ENABLE	Master enable of the CSD IP. Must be set to 1 for any CSD operation to function. Default: 0x0

3.1.2 CSD_CONFIG (continued)

30	CSD_DDFTCOMP	Changes comp_out signal for DFT purpose only. This signal can be routed to pins or other destinations using DDFTSEL Default: 0x0 **0x0: REFBUFCOMP** Normal function: comp_out is reference buffer comparator output. **0x1: SENSECOMP** DFT override function: comp_out is sensing comparator output (unflopped).
29	CSD_ADFTEN	When selected, convert IDAC1/2 outputs from current to voltage before sending to AMUXBUS-A/B. IDAC1/2 output currents and connectivity are determined by other CSD_CONFIG/ CSD_IDAC settings same as in normal mode. Default: 0x0
28 : 26	CSD_DDFTSEL	Changes the dsi_sample_out signal from its normal function (sample_out) to a selection of other DDFT signals. Default: 0x0 **0x0: NORMAL** Normal functionality. **0x1: CSD_SENSE** dsi_sample_out= csd_sense **0x2: CSD_SHIELD** dsi_sample_out= csd_shield **0x3: CLK_SAMPLE** dsi_sample_out= clk_sample **0x4: COMP_OUT** dsi_sample_out= comp_out
24 : 23	CSD_REFBUF_DRV	Current drive strength for reference buffer. Default: 0x0 **0x0: OFF** Current drive mode OFF **0x1: DRV_1** Lowest current drive mode **0x2: DRV_2** Mid current drive mode **0x3: DRV_3** Highest current drive mode
22	CSD_SENSE_INSEL	Selects how to connect the sensing comparator to the Cmod capacitor. Default: 0x0

3.1.2 CSD_CONFIG (continued)

		0x0: SENSE_CHANNEL1 Use the Channel 1 sense line to conenct to Cmod. **0x1: SENSE_AMUXA** Use the AMUXBUS-A bus to connect to Cmod.
21	CSD_REBUF_OUTSEL	Selects which AMUXBUS the reference buffer connects to. Default: 0x1 **0x0: AMUXA** Connect to AMUXBUS-A (not normally used). **0x1: AMUXB** Connect to AMUXBUS-B (normally used for all CSD operations).
19	CSD_SENSE_COMP_EN	Turns on the sense comparator circuit. Must be done some time before enable SENSE_EN. 0: Sense comparator is powered off. 1: Sense comparator is powered on. Default: 0x0
18	CSD_MUTUAL_CAP	Enables mutual cap sensing mode Default: 0x0 **0x0: SELFCAP** Self-cap mode (configure sense line as CSD_SENSE) **0x1: MUTUALCAP** Mutual-cap mode (configure Tx line as CSD_SENSE, Rx Line as AMUXA)
17	CSD_POLARITY2	For normal CSD operations this field is not used. When using the IDACs for other-than-CSD purposes, this bit controls the IDAC2 polarity only. Default: 0x0 **0x0: VSSIO** Normal: switch between Vssio and Cmod. For non-CSD application, IDAC2 will source current. **0x1: VDDIO** Inverted: switch between Vddio and Cmod. For non-CSD application, IDAC2 will sink current.
16	CSD_POLARITY	Selects the polarity of the sensing operation. When using the IDACs for other-than-CSD purposes, this bit controls the IDAC1 polarity only. Default: 0x0 **0x0: VSSIO** Normal: switch between Vssio and Cmod. For non-CSD application, IDAC1 will source current. **0x1: VDDIO** Inverted: switch between Vddio and Cmod. For non-CSD application, IDAC1 will sink current.
15	CSD_COMP_PIN	Connects either the Cmod or Csh_tank sense return line to the reference buffer comparator. This switch must be set to the same pin that is being charged up by the reference buffer (through the AMUXBUS settings in GPIO). Default: 0x0

3.1.2 CSD_CONFIG (continued)

		0x0: CHANNEL1 Use the sense line designated as Channel 1; this is normally used to conenct Cmod.
		0x1: CHANNEL2 Use the sense line designated as Channel 2; this is normally used to connect Csh_tank.
14	CSD_COMP_MODE	Selects between charging of the Cmod/Csh_tank capacitor using the GPIO digital output buffer or the CSD reference buffer. Note that using the GPIO requires proper configuraiton of the GPIO pin. Default: 0x0
		0x0: CHARGE_BUF Use CSD Reference Buffer to charge capacitor. Capacitor must be connected to AMUXBUS-A/B (see REBUF_OUTSEL) and selected using COMP_PIN.
		0x1: CHARGE_IO Use GPIO Driver to charge capacitor. Capacitor must be selected using COMP_PIN, and GPIO must be in AMUXB mode.
13	CSD_REFBUF_EN	Enables the reference buffer/comparator circuits for charging Cmod/Csh_tank using the mode selected in COMP_MODE. Default: 0x0
12	CSD_SENSE_EN	Enables the sense modulator output. Also turns on the IDAC compensation current as selected by CSD_IDAC. Default: 0x0
11	CSD_SENSE_COMP_BW	Selects bandwidth for sensing comparator Default: 0x1
		0x0: LOW Lower bandwidth
		0x1: HIGH High bandwidth (default)
10 : 9	CSD_SHIELD_DELAY	Indicates the number of clk_hf clock cycles that csd_shield is delayed relative to csd_sense. Valid values are 0,1,2. Default: 0x0
8	CSD_DSI_SENSE_EN	Enables the use of the dsi_sense_in input instead of the internally generated modulation signal to drive csd_sense and csd_shield signals. Default: 0x0
7	CSD_PRS_12_8	Selects between 8 or 12b PRS sequence Default: 0x0
		0x0: 8B 8-bit PRS sequence (G(x)=X^8+X^4+X^3+X^2+1, period= 255)
		0x1: 12B 12-bit PRS sequence (G(x)=X^12+X^9+X^3+X^2+1, period=4095)
6	CSD_PRS_SELECT	Selects between PRS or simple divide by 2 sense modulation. Default: 0x0

3.1.2 CSD_CONFIG (continued)

		0x0: DIV2 Select simple divide-by-2 of clk_csd1 as output. **0x1: PRS** Select PRS sequencer output, and start the sequencer.
5	CSD_PRS_CLEAR	When set, forces the pseudo-random generator to its initial state. Note that it may take some time for this setting to take effect depending on the clock frequency used for clk_csd1. Hardware clears this bit at the same time PRS is cleared. Default: 0x0
1	CSD_SAMPLE_SYNC	Enables double synchronizing of sample input from DSI (only relevant when DSI_SAMPLE_EN=1). Default: 0x1
0	CSD_DSI_SAMPLE_EN	Enables the use of the dsi_sample_in input instead of the comparator output to strobe COUNTER. Default: 0x0

3.1.3 CSD_IDAC

Address: 0x40080008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None	0x0	None			0x0	0x0	
HW Access	None	R	None			R	R	
SW Access	None	RW	None			RW	RW	
Bit Name	Reserved	CSD_FEEDBACK_MODE	Reserved[29:27]			CSD_IDAC2_RANGE	CSD_IDAC2_MODE [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	None	0x00						
HW Access	None	R						
SW Access	None	RW						
Bit Name	Reserved	CSD_IDAC2 [22:16]						

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	
HW Access	None					R	R	
SW Access	None					RW	RW	
Bit Name	Reserved[15:11]					CSD_IDAC1_RANGE	CSD_IDAC1_MODE [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	CSD_IDAC1 [7:0]							

IDAC Configuration

Bits	Name	Description
30	CSD_FEEDBACK_MODE	This bit controls whether, during CSD operation, the IDAC is controlled from the sampling flip-flop or directly from the comparator. Default: 0x0 **0x0: FLOP** Use feedback from sampling flip-flop (used in most modes). **0x1: COMP** Use feedback from comparator directly (used in single Cmod mutual cap sensing only)

3.1.3 CSD_IDAC (continued)

26	CSD_IDAC2_RANGE	Current multiplier setting for IDAC2. Default: 0x0 **0x0: 4X** Use 4X gain setting. **0x1: 8X** Use 8X gain setting.
25 : 24	CSD_IDAC2_MODE	Controls the usage mode of IDAC2 Default: 0x0 **0x0: OFF** IDAC2 is not used. **0x1: FIXED** IDAC2 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE** IDAC2 is switched on and off depending on the result of the comparator. **0x3: DSI** IDAC2 is controlled from dsi input dsi_idac2_en. It is connected to AMUXBUS-A or AMUXBUS-B depending on IDAC_SWAP setting.
22 : 16	CSD_IDAC2	Current setting for IDAC2 (7 bits). Default: 0x00
10	CSD_IDAC1_RANGE	Current multiplier setting for IDAC1. Default: 0x0 **0x0: 4X** Use 4X gain setting. **0x1: 8X** Use 8X gain setting.
9 : 8	CSD_IDAC1_MODE	Controls the usage mode of IDAC1 Default: 0x0 **0x0: OFF** IDAC1 is not used. **0x1: FIXED** IDAC1 is active whenever CSD_CONFIG.SENSE_EN is asserted. **0x2: VARIABLE** IDAC1 is switched on and off depending on the result of the comparator. **0x3: DSI** IDAC1 is controlled from dsi input dsi_idac1_en. It is connected to AMUXBUS-A or AMUXBUS-B depending on IDAC_SWAP setting.

3.1.3 CSD_IDAC (continued)

7 : 0	CSD_IDAC1	Current setting for IDAC1 (8 bits). Default: 0x00

3.1.4 CSD_COUNTER

Address: 0x4008000C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	CSD_PERIOD [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	CSD_PERIOD [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	CSD_COUNTER [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	CSD_COUNTER [15: 0]							

CSD Counter Register

Bits	Name	Description
31 : 16	CSD_PERIOD	The remaining period (in clk_csd1 cycles) during which COUNTER will count the comparator output count. Firmware will write this field to the desired period, after which it will start counting down to 0. Upon completion of the sense operation, this field will be 0. Writing a non-0 value to this register initiates a sensing operation. It is assumed that the modulation is properly configured, all pins are properly selected and configured and that sense currents are flowing before this field is written. Default: 0x0000
15 : 0	CSD_COUNTER	This field increments whenever the comparator is sampled and the sample is 1. Firmware typically writes 0 to this field whenever a new sense operation is initiated by writing a non-0 value to PERIOD. Default: 0x0000

3.1.5 CSD_STATUS

Address: 0x40080010

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW	RW	RW	RW
SW Access	None				R	R	R	R
Bit Name	Reserved[7:4]				CSD_SAMPLE	CSD_COMP_OUT	CSD_CSD_SENSE	CSD_CSD_CHARGE

Status Register

Bits	Name	Description
3	CSD_SAMPLE	Output of main sensing comparator. Default: 0x0
2	CSD_COMP_OUT	Output of reference buffer comparator used to charge up Cmod or Csh_tank. Default: 0x0 **0x0: C_LT_VREF** Ctank lt; Vref **0x1: C_GT_VREF** Ctank gt; Vref

3.1.5 CSD_STATUS (continued)

1	CSD_CSD_SENSE	Signal used to drive the Cs switches. Default: 0x0
0	CSD_CSD_CHARGE	Qualified, and possible inverted value of COMP_OUT that is used to drive GPIOs charging Cmod or Csh_tank. Default: 0x0

3.1.6 CSD_INTR

Address: 0x40080014

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							RW1S
SW Access	None							RW1C
Bit Name	Reserved[7:1]							CSD_CSD

CSD Interrupt Request Register

Bits	Name	Description
0	CSD_CSD	The CSD IRQ bit is set. Firmware must clear this bit as part of the interrupt handler. Default: 0x0

3.1.7 CSD_INTR_SET

Address: 0x40080018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							None
SW Access	None							RW1S
Bit Name	Reserved[7:1]							CSD_CSD

CSD Interrupt set register

Bits	Name	Description
0	CSD_CSD	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

3.1.8 CSD_TRIM1

Address: 0x4008FF00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	CSD_IDAC2_SRC_TRIM [7:4]				CSD_IDAC1_SRC_TRIM [3:0]			

CSD Trim Register

Bits	Name	Description
7 : 4	CSD_IDAC2_SRC_TRIM	IDAC2 trim bits for gain control in current source mode Default: 0x0
3 : 0	CSD_IDAC1_SRC_TRIM	IDAC1 trim bits for gain control in current source mode Default: 0x0

3.1.9 CSD_TRIM2

Address: 0x4008FF04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	CSD_IDAC2_SNK_TRIM [7:4]				CSD_IDAC1_SNK_TRIM [3:0]			

CSD Trim Register

Bits	Name	Description
7 : 4	CSD_IDAC2_SNK_TRIM	IDAC2 trim bits for gain control in current sink mode Default: 0x0
3 : 0	CSD_IDAC1_SNK_TRIM	IDAC1 trim bits for gain control in current sink mode Default: 0x0

4 CTBM Registers

This section discusses the CTBM registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

4.1 CTBM Register Mapping Overview

Register Name	Address
CTBM_CTB_CTRL	0x40100000
CTBM_OA_RES0_CTRL	0x40100004
CTBM_OA_RES1_CTRL	0x40100008
CTBM_COMP_STAT	0x4010000C
CTBM_INTR	0x40100020
CTBM_INTR_SET	0x40100024
CTBM_INTR_MASK	0x40100028
CTBM_INTR_MASKED	0x4010002C
CTBM_DFT_CTRL	0x40100030
CTBM_OA0_SW	0x40100080
CTBM_OA0_SW_CLEAR	0x40100084
CTBM_OA1_SW	0x40100088
CTBM_OA1_SW_CLEAR	0x4010008C
CTBM_CTB_SW_HW_CTRL	0x401000C0
CTBM_CTB_SW_STATUS	0x401000C4
CTBM_OA0_OFFSET_TRIM	0x40100F00
CTBM_OA0_SLOPE_OFFSET_TRIM	0x40100F04
CTBM_OA0_COMP_TRIM	0x40100F08
CTBM_OA1_OFFSET_TRIM	0x40100F0C
CTBM_OA1_SLOPE_OFFSET_TRIM	0x40100F10
CTBM_OA1_COMP_TRIM	0x40100F14

4.1.1 CTBM_CTB_CTRL

Address: 0x40100000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	CTBM_ENABLED	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

global CTB and power control

Bits	Name	Description
31	CTBM_ENABLED	- 0: CTB IP disabled (put analog in power down, open all switches) - 1: CTB IP enabled Default: 0x0

4.1.2 CTBM_OA_RES0_CTRL

Address: 0x40100004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	None	0x0	
HW Access	None				R	None	R	
SW Access	None				RW	None	RW	
Bit Name	Reserved[15:12]				CTBM_OA0_PUMP_EN	Reserved	CTBM_OA0_COMPINT[9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0	0x0	None	0x0	0x0	
HW Access	None	R	R	R	None	R	R	
SW Access	None	RW	RW	RW	None	RW	RW	
Bit Name	Reserved	CTBM_OA0_BYPASS_DSI_SYNC	CTBM_OA0_HYST_EN	CTBM_OA0_COMP_EN	Reserved	CTBM_OA0_DRIVE_STR_SEL	CTBM_OA0_PWR_MODE[1:0]	

Opamp0 and resistor0 control

Bits	Name	Description
11	CTBM_OA0_PUMP_EN	Opamp0 pump enable Default: 0x0
9 : 8	CTBM_OA0_COMPINT	Opamp0 comparator edge detect Default: 0x0
		0x0: DISABLE Disabled

4.1.2 CTBM_OA_RES0_CTRL (continued)

		0x1: RISING Rising edge **0x2: FALLING** Falling edge **0x3: BOTH** Both rising and falling edges
6	CTBM_OA0_BYPASS_DSI_SYNC	Opamp0 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default: 0x0
5	CTBM_OA0_HYST_EN	Opamp0 hysteresis enable (10mV) Default: 0x0
4	CTBM_OA0_COMP_EN	Opamp0 comparator enable Default: 0x0
2	CTBM_OA0_DRIVE_STR_SEL	Opamp0 output strenght select 0=1x, 1=10x Default: 0x0
1 : 0	CTBM_OA0_PWR_MODE	Opamp0 power level: 0=off Default: 0x0

4.1.3 CTBM_OA_RES1_CTRL

Address: 0x40100008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	None	0x0	
HW Access	None				R	None	R	
SW Access	None				RW	None	RW	
Bit Name	Reserved[15:12]				CTBM_OA1_PUMP_EN	Reserved	CTBM_OA1_COMPINT[9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0	0x0	None	0x0	0x0	
HW Access	None	R	R	R	None	R	R	
SW Access	None	RW	RW	RW	None	RW	RW	
Bit Name	Reserved	CTBM_OA1_BYPASS_DSI_SYNC	CTBM_OA1_HYST_EN	CTBM_OA1_COMP_EN	Reserved	CTBM_OA1_DRIVE_STR_SEL	CTBM_OA1_PWR_MODE[1:0]	

Opamp1 and resistor1 control

Bits	Name	Description
11	CTBM_OA1_PUMP_EN	Opamp1 pump enable Default: 0x0
9 : 8	CTBM_OA1_COMPINT	Opamp0 comparator edge detect Default: 0x0
		0x0: DISABLE Disabled

4.1.3 CTBM_OA_RES1_CTRL (continued)

		0x1: RISING Rising edge **0x2: FALLING** Falling edge **0x3: BOTH** Both rising and falling edges
6	CTBM_OA1_BYPASS_DSI_SYNC	Opamp1 bypass comparator output synchronization for DSI output: 0=synchronize, 1=bypass Default: 0x0
5	CTBM_OA1_HYST_EN	Opamp1 hysteresis enable (10mV) Default: 0x0
4	CTBM_OA1_COMP_EN	Opamp1 comparator enable Default: 0x0
2	CTBM_OA1_DRIVE_STR_SEL	Opamp1 output strenght select 0=1x, 1=10x Default: 0x0
1 : 0	CTBM_OA1_PWR_MODE	Opamp1 power level: 0=off Default: 0x0

4.1.4 CTBM_COMP_STAT

Address: 0x4010000C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							W
SW Access	None							R
Bit Name	Reserved[23:17]							CTBM_OA1_COMP

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							W
SW Access	None							R
Bit Name	Reserved[7:1]							CTBM_OA0_COMP

Comparator status

Bits	Name	Description
16	CTBM_OA1_COMP	Opamp1 current comparator status Default: 0x0
0	CTBM_OA0_COMP	Opamp0 current comparator status Default: 0x0

4.1.5 CTBM_INTR

Address: 0x40100020

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						RW1S	RW1S
SW Access	None						RW1C	RW1C
Bit Name	Reserved[7:2]						CTBM_COMP1	CTBM_COMP0

Interrupt request register

Bits	Name	Description
1	CTBM_COMP1	Comparator 1 Interrupt: hardware sets this interrupt when comparator 1 triggers. Write with 1 to clear bit. Default: 0x0
0	CTBM_COMP0	Comparator 0 Interrupt: hardware sets this interrupt when comparator 0 triggers. Write with 1 to clear bit. Default: 0x0

4.1.6 CTBM_INTR_SET

Address: 0x40100024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						None	None
SW Access	None						RW1S	RW1S
Bit Name	Reserved[7:2]						CTBM_COMP1_SET	CTBM_COMP0_SET

Interrupt request set register

Bits	Name	Description
1	CTBM_COMP1_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
0	CTBM_COMP0_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

4.1.7 CTBM_INTR_MASK

Address: 0x40100028

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[7:2]						CTBM_COMP1_MASK	CTBM_COMP0_MASK

Interrupt request mask

Bits	Name	Description
1	CTBM_COMP1_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	CTBM_COMP0_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0

4.1.8 CTBM_INTR_MASKED

Address: 0x4010002C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						W	W
SW Access	None						R	R
Bit Name	Reserved[7:2]						CTBM_COMP1_MASKED	CTBM_COMP0_MASKED

Interrupt request masked

Bits	Name	Description
1	CTBM_COMP1_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
0	CTBM_COMP0_MASKED	Logical and of corresponding request and mask bits. Default: 0x0

4.1.9 CTBM_DFT_CTRL

Address: 0x40100030

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	CTBM_DFT_EN	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0		
HW Access	None					R		
SW Access	None					RW		
Bit Name	Reserved[7:3]					CTBM_DFT_MODE [2:0]		

Analog DfT controls

Bits	Name	Description
31	CTBM_DFT_EN	Analog DfT enable Default: 0x0
2 : 0	CTBM_DFT_MODE	Analog DfT mode Default: 0x0

4.1.10 CTBM_OA0_SW

Address: 0x40100080

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None		0x0	None		0x0	None	
HW Access	None		RW1C	None		RW1C	None	
SW Access	None		RW1S	None		RW1S	None	
Bit Name	Reserved[23:22]		CTBM_OA0O_D81	Reserved[20:19]		CTBM_OA0O_D51	Reserved[17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	None	0x0	None					0x0
HW Access	None	RW1C	None					RW1C
SW Access	None	RW1S	None					RW1S
Bit Name	Reserved	CTBM_OA0M_A81	Reserved[13:9]					CTBM_OA0M_A11

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	None	0x0
HW Access	None				RW1C	RW1C	None	RW1C
SW Access	None				RW1S	RW1S	None	RW1S
Bit Name	Reserved[7:4]				CTBM_OA0P_A30	CTBM_OA0P_A20	Reserved	CTBM_OA0P_A00

Opamp0 switch control

Bits	Name	Description
21	CTBM_OA0O_D81	Opamp0 output switch to short 1x with 10x drive Default: 0x0
18	CTBM_OA0O_D51	Opamp0 output sarbus0 (ctbbus2 in CTB) Default: 0x0
14	CTBM_OA0M_A81	Opamp0 negative terminal Opamp0 bottom Default: 0x0
8	CTBM_OA0M_A11	Opamp0 negative terminal P1 Default: 0x0

4.1.10 CTBM_OA0_SW (continued)

3	CTBM_OA0P_A30	Opamp0 positive terminal ctbbus0 Default: 0x0
2	CTBM_OA0P_A20	Opamp0 positive terminal P0 Default: 0x0
0	CTBM_OA0P_A00	Opamp0 positive terminal amuxbusa Default: 0x0

4.1.11 CTBM_OA0_SW_CLEAR

Address: 0x40100084

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None		0x0	None		0x0	None	
HW Access	None		None	None		None	None	
SW Access	None		RW1C	None		RW1C	None	
Bit Name	Reserved[23:22]		CTBM_OA0O_D81	Reserved[20:19]		CTBM_OA0O_D51	Reserved[17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	None	0x0	None					0x0
HW Access	None	None	None					None
SW Access	None	RW1C	None					RW1C
Bit Name	Reserved	CTBM_OA0M_A81	Reserved[13:9]					CTBM_OA0M_A11

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	None	0x0
HW Access	None				None	None	None	None
SW Access	None				RW1C	RW1C	None	RW1C
Bit Name	Reserved[7:4]				CTBM_OA0P_A30	CTBM_OA0P_A20	Reserved	CTBM_OA0P_A00

Opamp0 switch control clear

Bits	Name	Description
21	CTBM_OA0O_D81	see corresponding bit in OA0_SW Default: 0x0
18	CTBM_OA0O_D51	see corresponding bit in OA0_SW Default: 0x0
14	CTBM_OA0M_A81	see corresponding bit in OA0_SW Default: 0x0
8	CTBM_OA0M_A11	see corresponding bit in OA0_SW Default: 0x0

4.1.11 CTBM_OA0_SW_CLEAR (continued)

3	CTBM_OA0P_A30	see corresponding bit in OA0_SW Default: 0x0
2	CTBM_OA0P_A20	see corresponding bit in OA0_SW Default: 0x0
0	CTBM_OA0P_A00	see corresponding bit in OA0_SW Default: 0x0

4.1.12 CTBM_OA1_SW

Address: 0x40100088

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None		0x0	None	0x0	0x0	None	
HW Access	None		RW1C	None	RW1C	RW1C	None	
SW Access	None		RW1S	None	RW1S	RW1S	None	
Bit Name	Reserved[23:22]		CTBM_OA1O_D82	Reserved	CTBM_OA1O_D62	CTBM_OA1O_D52	Reserved[17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	None	0x0	None					0x0
HW Access	None	RW1C	None					RW1C
SW Access	None	RW1S	None					RW1S
Bit Name	Reserved	CTBM_OA1M_A82	Reserved[13:9]					CTBM_OA1M_A22

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None		0x0	0x0
HW Access	None			RW1C	None		RW1C	RW1C
SW Access	None			RW1S	None		RW1S	RW1S
Bit Name	Reserved[7:5]			CTBM_OA1P_A43	Reserved[3:2]		CTBM_OA1P_A13	CTBM_OA1P_A03

Opamp1 switch control

Bits	Name	Description
21	CTBM_OA1O_D82	Opamp1 output switch to short 1x with 10x drive Default: 0x0
19	CTBM_OA1O_D62	Opamp1 output sarbus1 (ctbbus3 in CTB) Default: 0x0
18	CTBM_OA1O_D52	Opamp1 output sarbus0 (ctbbus2 in CTB) Default: 0x0
14	CTBM_OA1M_A82	Opamp1 negative terminal Opamp1 bottom Default: 0x0

4.1.12 CTBM_OA1_SW (continued)

8	CTBM_OA1M_A22	Opamp1 negative terminal P4 Default: 0x0
4	CTBM_OA1P_A43	Opamp1 positive terminal ctbbus1 Default: 0x0
1	CTBM_OA1P_A13	Opamp1 positive terminal P5 Default: 0x0
0	CTBM_OA1P_A03	Opamp1 positive terminal amuxbusb Default: 0x0

4.1.13 CTBM_OA1_SW_CLEAR

Address: 0x4010008C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None		0x0	None	0x0	0x0	None	
HW Access	None		None	None	None	None	None	
SW Access	None		RW1C	None	RW1C	RW1C	None	
Bit Name	Reserved[23:22]		CTBM_OA1O_D82	Reserved	CTBM_OA1O_D62	CTBM_OA1O_D52	Reserved[17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	None	0x0	None					0x0
HW Access	None	None	None					None
SW Access	None	RW1C	None					RW1C
Bit Name	Reserved	CTBM_OA1M_A82	Reserved[13:9]					CTBM_OA1M_A22

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None		0x0	0x0
HW Access	None			None	None		None	None
SW Access	None			RW1C	None		RW1C	RW1C
Bit Name	Reserved[7:5]			CTBM_OA1P_A43	Reserved[3:2]		CTBM_OA1P_A13	CTBM_OA1P_A03

Opamp1 switch control clear

Bits	Name	Description
21	CTBM_OA1O_D82	see corresponding bit in OA1_SW Default: 0x0
19	CTBM_OA1O_D62	see corresponding bit in OA1_SW Default: 0x0
18	CTBM_OA1O_D52	see corresponding bit in OA1_SW Default: 0x0
14	CTBM_OA1M_A82	see corresponding bit in OA1_SW Default: 0x0

4.1.13 CTBM_OA1_SW_CLEAR (continued)

8	CTBM_OA1M_A22	see corresponding bit in OA1_SW Default: 0x0
4	CTBM_OA1P_A43	see corresponding bit in OA1_SW Default: 0x0
1	CTBM_OA1P_A13	see corresponding bit in OA1_SW Default: 0x0
0	CTBM_OA1P_A03	see corresponding bit in OA1_SW Default: 0x0

4.1.14 CTBM_CTB_SW_HW_CTRL

Address: 0x401000C0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	None	
HW Access	None				R	R	None	
SW Access	None				RW	RW	None	
Bit Name	Reserved[7:4]				CTBM_P3_HW_CTRL	CTBM_P2_HW_CTRL	Reserved[1:0]	

CTB bus switch control status

Bits	Name	Description
3	CTBM_P3_HW_CTRL	Pin P3 switches Default: 0x0
2	CTBM_P2_HW_CTRL	Pin P2 switches Default: 0x0

4.1.15 CTBM_CTB_SW_STATUS

Address: 0x401000C4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None	0x0	0x0	0x0	None			
HW Access	None	W	W	W	None			
SW Access	None	R	R	R	None			
Bit Name	Reserved	CTBM_OA1O_D62_STAT	CTBM_OA1O_D52_STAT	CTBM_OA0O_D51_STAT	Reserved[27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

CTB bus switch control status

Bits	Name	Description
30	CTBM_OA1O_D62_STAT	see OA1O_D62 bit in OA1_SW Default: 0x0
29	CTBM_OA1O_D52_STAT	see OA1O_D52 bit in OA1_SW Default: 0x0
28	CTBM_OA0O_D51_STAT	see OA0O_D51 bit in OA0_SW Default: 0x0

4.1.16 CTBM_OA0_OFFSET_TRIM

Address: 0x40100F00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		CTBM_OA0_OFFSET_TRIM [5:0]					

Opamp0 trim control

Bits	Name	Description
5 : 0	CTBM_OA0_OFFSET_TRIM	Opamp0 offset trim Default: 0x00

4.1.17 CTBM_OA0_SLOPE_OFFSET_TRIM

Address: 0x40100F04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		CTBM_OA0_SLOPE_OFFSET_TRIM [5:0]					

Opamp0 trim control

Bits	Name	Description
5 : 0	CTBM_OA0_SLOPE_OFFSET_TRIM	Opamp0 slope offset drift trim Default: 0x00

4.1.18 CTBM_OA0_COMP_TRIM

Address: 0x40100F08

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[7:2]						CTBM_OA0_COMP_TRIM [1:0]	

Opamp0 trim control

Bits	Name	Description
1 : 0	CTBM_OA0_COMP_TRIM	Opamp0 Compenation Capacitor Trim Default: 0x0

4.1.19 CTBM_OA1_OFFSET_TRIM

Address: 0x40100F0C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		CTBM_OA1_OFFSET_TRIM [5:0]					

Opamp1 trim control

Bits	Name	Description
5 : 0	CTBM_OA1_OFFSET_TRIM	Opamp1 offset trim Default: 0x00

4.1.20 CTBM_OA1_SLOPE_OFFSET_TRIM

Address: 0x40100F10

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		CTBM_OA1_SLOPE_OFFSET_TRIM [5:0]					

Opamp1 trim control

Bits	Name	Description
5 : 0	CTBM_OA1_SLOPE_OFFSET_TRIM	Opamp1 slope offset drift trim Default: 0x00

4.1.21 CTBM_OA1_COMP_TRIM

Address: 0x40100F14

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[7:2]						CTBM_OA1_COMP_TRIM[1:0]	

Opamp1 trim control

Bits	Name	Description
1 : 0	CTBM_OA1_COMP_TRIM	Opamp1 Compenation Capacitor Trim Default: 0x0

5 HSIOM4A Registers

This section discusses the HSIOM4A registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

5.1 HSIOM4A Register Mapping Overview

Register Name	Address
HSIOM_PORT_SEL0	0x40010000
HSIOM_PORT_SEL1	0x40010004
HSIOM_PORT_SEL2	0x40010008
HSIOM_PORT_SEL3	0x4001000C
HSIOM_PORT_SEL4	0x40010010

5.1.1 HSIOM_PORT_SEL0

Address: 0x40010000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Port 0 control register.

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects pin 7 source. Default: 0x0 **0xE: WAKEUP** Pin is used as WAKEUP input to wakeup from STOP power mode. Note that this pin is always available for this function. Selecting this pin role only ensures that no other function is overloaded on this pin (ie. that the output is not driven by some other function prohibiting wakeup behavior). **0xF: SCB1_SPI_SSEL0** Pin is connected to SPI SSSEL (Slave Select) output #0 of SCB #1. This mode remains active and usable in DeepSleep mode.
27 : 24	HSIOM_SEL6	Selects pin 6 source. Default: 0x0

5.1.1 HSIOM_PORT_SEL0 (continued)

		0x8: EXT_CLK Pin is connected to EXT_CLK input of system clock system. To use it, it must also be selected in CLK_SELECT register. **0xF: SCB1_SPI_CLK** Pin is connected to CLK pin of SPI #1. This mode remains active and usable in DeepSleep mode.
23 : 20	HSIOM_SEL5	Selects pin 5 source. Default: 0x0 **0x9: SCB1_UART_TX** Pin is connected to TX (transmit) output of UART #1. **0xE: SCB1_I2C_SDA** Pin is connected to SDA data pin of I2C #1. This mode remains active and usable in DeepSleep mode. **0xF: SCB1_SPI_MISO** Pin is connected to MISO pin of SPI #1. This mode remains active and usable in DeepSleep mode.
19 : 16	HSIOM_SEL4	Selects pin 4 source. Default: 0x0 **0x9: SCB1_UART_RX** Pin is connected to RX (receive) input of UART #1. **0xE: SCB1_I2C_SCL** Pin is connected to SCL (clock) pin of I2C #1. This mode remains active and usable in Deep-Sleep mode. **0xF: SCB1_SPI_MOSI** Pin is connected to MOSI pin of SPI #1. This mode remains active and usable in DeepSleep mode.
15 : 12	HSIOM_SEL3	Selects pin 3 source. Default: 0x0 **0x0: COMP2_INN** Pin is used as N input for low-power comparator #2 (must also set GPIO_PRT0.DM3= OFF).
11 : 8	HSIOM_SEL2	Selects pin 2 source. Default: 0x0 **0x0: COMP2_INP** Pin is used as P input for low-power comparator #2 (must also set GPIO_PRT0.DM2= OFF). **0xF: SCB0_SPI_SSEL3** Pin is connected to SPI SSSEL (Slave Select) output #3 of SCB #0. This mode remains active and usable in DeepSleep mode.

5.1.1 HSIOM_PORT_SEL0 (continued)

7 : 4	HSIOM_SEL1	Selects pin 1 source. Default: 0x0 **0x0: COMP1_INN** Pin is used as N input for low-power comparator #1 (must also set GPIO_PRT0.DM1= OFF). **0xF: SCB0_SPI_SSEL2** Pin is connected to SPI SSSEL (Slave Select) output #2 of SCB #0. This mode remains active and usable in DeepSleep mode.
3 : 0	HSIOM_SEL0	Selects pin 0 source. All of the values given for this field are usable for any pin. Only SARMUX_0 is specific to P0.0. Default: 0x0 **0x0: GPIO** Pin is regular firmware controlled GPIO. **0x1: GPIO_DSI** Output is firmware controlled, but OE is controlled from DSI. **0x2: DSI_DSI** Both Output and OE are controlled from DSI. **0x3: DSI_GPIO** Output is controlled from DSI, but OE is firmware controlled. **0x4: CSD_SENSE** Pin is a CSD sense pin (analog mode) **0x5: CSD_SHIELD** Pin is a CSD shield pin (analog mode) **0x6: AMUXA** Pin is connected to AMUXBUS A. **0x7: AMUXB** Pin is connected to AMUXBUS B. This mode is also used for CSD GPIO charging. When CSD GPIO charging is enabled in CSD_CONTROL, digital IO driver is connected to csd_charge signal (and pin is also still connected to AMUXBUS B). **0x8: ACT_0** Pin specific Active source #0. **0x9: ACT_1** Pin specific Active source #1. **0xA: ACT_2** Pin specific Active source #2.

5.1.1 HSIOM_PORT_SEL0 (continued)

0xB: ACT_3
Pin specific Active source #3.

0xC: LCD_COM
Pin is an LCD common pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured).

0xD: LCD_SEG
Pin is an LCD segment pin. This mode remains active and usable in DeepSleep mode (provided that the LCD block is enabled and properly configured).

0xE: DPSLP_0
Pin specific DeepSleep souurce #0.

0xF: DPSLP_1
Pin specific DeepSleep souurce #1.

0x0: COMP1_INP
Pin is used as P input for low-power comparator #1 (must also set GPIO_PRT0.DM0= OFF).

0xF: SCB0_SPI_SSEL1
Pin is connected to SPI SSSEL (Slave Select) output #1 of SCB #0. This mode remains active and usable in DeepSleep mode.

5.1.2 HSIOM_PORT_SEL1

Address: 0x40010004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Port 1 control register.

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects pin 7 source. Default: 0x0 **0x0: EXT_VREF** Pin is used as external reference input for the SAR (must also set GPIO_PRT1.DM7= OFF).
27 : 24	HSIOM_SEL6	Selects pin 6 source. Default: 0x0
23 : 20	HSIOM_SEL5	Selects pin 5 source. Default: 0x0 **0x0: CTB_OA2_INP** Pin is used as P input for OpAmp #2 of the CTB (must also set GPIO_PRT1.DM5= OFF).

5.1.2 HSIOM_PORT_SEL1 (continued)

19 : 16	HSIOM_SEL4	Selects pin 4 source. Default: 0x0 **0x0: CTB_OA2_INN** Pin is used as N input for OpAmp #2 of the CTB (must also set GPIO_PRT1.DM4= OFF).
15 : 12	HSIOM_SEL3	Selects pin 3 source. Default: 0x0 **0x0: CTB_OA2_OUT** Pin is used as output for OpAmp #2 of the CTB (must also set GPIO_PRT1.DM3= OFF). **0x8: TCPWM3_N** Pin is connected to TCPWM counter #3, complementary output.
11 : 8	HSIOM_SEL2	Selects pin 2 source. Default: 0x0 **0x0: CTB_OA1_OUT** Pin is used as output for OpAmp #1 of the CTB (must also set GPIO_PRT1.DM2= OFF). **0x8: TCPWM3_P** Pin is connected to TCPWM counter #3, regular output.
7 : 4	HSIOM_SEL1	Selects pin 1 source. Default: 0x0 **0x0: CTB_OA1_INN** Pin is used as N input for OpAmp #1 of the CTB (must also set GPIO_PRT1.DM1= OFF). **0x8: TCPWM2_N** Pin is connected to TCPWM counter #2, complementary output.
3 : 0	HSIOM_SEL0	Selects pin 0 source. Default: 0x0 **0x0: CTB_OA1_INP** Pin is used as P input for OpAmp #1 of the CTB (must also set GPIO_PRT1.DM0= OFF). **0x8: TCPWM2_P** Pin is connected to TCPWM counter #2, regular output.

5.1.3 HSIOM_PORT_SEL2

Address: 0x40010008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Port 2 control register.

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects pin 7 source. Default: 0x0 **0x0: SARMUX_7** Pin is used as input #7 to the SAR ADC (must also set GPIO_PRT2.DM7= OFF). **0x8: TCPWM1_N** Pin is connected to TCPWM counter #1, complementary output.
27 : 24	HSIOM_SEL6	Selects pin 6 source. Default: 0x0 **0x0: SARMUX_6** Pin is used as input #6 to the SAR ADC (must also set GPIO_PRT2.DM6= OFF).

5.1.3 HSIOM_PORT_SEL2 (continued)

		0x8: TCPWM1_P Pin is connected to TCPWM counter #1, regular output.
23 : 20	HSIOM_SEL5	Selects pin 5 source. Default: 0x0 **0x0: SARMUX_5** Pin is used as input #5 to the SAR ADC (must also set GPIO_PRT2.DM5= OFF). **0x8: TCPWM0_N** Pin is connected to TCPWM counter #0, complementary output.
19 : 16	HSIOM_SEL4	Selects pin 4 source. Default: 0x0 **0x0: SARMUX_4** Pin is used as input #4 to the SAR ADC (must also set GPIO_PRT2.DM4= OFF). **0x8: TCPWM0_P** Pin is connected to TCPWM counter #0, regular output.
15 : 12	HSIOM_SEL3	Selects pin 3 source. Default: 0x0 **0x0: SARMUX_3** Pin is used as input #3 to the SAR ADC (must also set GPIO_PRT2.DM3= OFF).
11 : 8	HSIOM_SEL2	Selects pin 2 source. Default: 0x0 **0x0: SARMUX_2** Pin is used as input #2 to the SAR ADC (must also set GPIO_PRT2.DM2= OFF).
7 : 4	HSIOM_SEL1	Selects pin 1 source. Default: 0x0 **0x0: SARMUX_1** Pin is used as input #1 to the SAR ADC (must also set GPIO_PRT2.DM1= OFF).
3 : 0	HSIOM_SEL0	Selects pin 0 source. Default: 0x0 **0x0: SARMUX_0** Pin is used as input #0 to the SAR ADC (must also set GPIO_PRT2.DM0= OFF).

5.1.4 HSIOM_PORT_SEL3

Address: 0x4001000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL7 [31:28]				HSIOM_SEL6 [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL5 [23:20]				HSIOM_SEL4 [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Port 3 control register.

Bits	Name	Description
31 : 28	HSIOM_SEL7	Selects pin 7 source. Default: 0x0 **0x8: TCPWM3_N** Pin is connected to TCPWM counter #3, complementary output. **0xE: SWD_CLK** Pin is connected to SWD CLK signal
27 : 24	HSIOM_SEL6	Selects pin 6 source. Default: 0x0 **0x8: TCPWM3_P** Pin is connected to TCPWM counter #3, regular output.

5.1.4 HSIOM_PORT_SEL3 (continued)

		0xE: SWD_IO Pin is connected to SWD IO signal. **0xF: SCB1_SPI_SSEL3** Pin is connected to SPI SSSEL (Slave Select) output #3 of SCB #1. This mode remains active and usable in DeepSleep mode.
23 : 20	HSIOM_SEL5	Selects pin 5 source. Default: 0x0 **0x8: TCPWM2_N** Pin is connected to TCPWM counter #2, complementary output. **0xF: SCB1_SPI_SSEL2** Pin is connected to SPI SSSEL (Slave Select) output #2 of SCB #1. This mode remains active and usable in DeepSleep mode.
19 : 16	HSIOM_SEL4	Selects pin 4 source. Default: 0x0 **0x8: TCPWM2_P** Pin is connected to TCPWM counter #2, regular output. **0xF: SCB1_SPI_SSEL1** Pin is connected to SPI SSSEL (Slave Select) output #1 of SCB #1. This mode remains active and usable in DeepSleep mode.
15 : 12	HSIOM_SEL3	Selects pin 3 source. Default: 0x0 **0x8: TCPWM1_N** Pin is connected to TCPWM counter #1, complementary output. **0xE: SWD_CLK** Pin is connected to SWD CLK signal **0xF: SCB1_SPI_SSEL0** Pin is connected to SPI SSSEL (Slave Select) output #0 of SCB #1. This mode remains active and usable in DeepSleep mode.
11 : 8	HSIOM_SEL2	Selects pin 2 source. Default: 0x0 **0x8: TCPWM1_P** Pin is connected to TCPWM counter #1, regular output. **0xE: SWD_IO** Pin is connected to SWD IO signal. **0xF: SCB1_SPI_CLK** Pin is connected to CLK pin of SPI #1. This mode remains active and usable in DeepSleep mode.

5.1.4 HSIOM_PORT_SEL3 (continued)

7 : 4	HSIOM_SEL1	Selects pin 1 source. Default: 0x0 **0x8: TCPWM0_N** Pin is connected to TCPWM counter #0, complementary output. **0x9: SCB1_UART_TX** Pin is connected to TX (transmit) input of UART #1. **0xE: SCB1_I2C_SDA** Pin is connected to SDA data pin of I2C #1. This mode remains active and usable in DeepSleep mode. **0xF: SCB1_SPI_MISO** Pin is connected to MISO pin of SPI #1. This mode remains active and usable in DeepSleep mode.
3 : 0	HSIOM_SEL0	Selects pin 0 source. Default: 0x0 **0x8: TCPWM0_P** Pin is connected to TCPWM counter #0, regular output. **0x9: SCB1_UART_RX** Pin is connected to RX (receive) input of UART #1. **0xE: SCB1_I2C_SCL** Pin is connected to SCL (clock) pin of I2C #1. This mode remains active and usable in Deep-Sleep mode. **0xF: SCB1_SPI_MOSI** Pin is connected to MOSI pin of SPI #1. This mode remains active and usable in DeepSleep mode.

5.1.5 HSIOM_PORT_SEL4

Address: 0x40010010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL3 [15:12]				HSIOM_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	RW				RW			
SW Access	RW				RW			
Bit Name	HSIOM_SEL1 [7:4]				HSIOM_SEL0 [3:0]			

Port 4 control register.

Bits	Name	Description
15 : 12	HSIOM_SEL3	Selects pin 3 source. Default: 0x0 **0x7: CSD_CSHTANK** Pin is connected to external CSD Csh_tank capacitor used in capactitive sensing or REFBUF precharge mode. **0x7: CSD_CSHTANK_CHRG** Pin is connected to external CSD Csh_tank capacitor in GPIO pre-charge mode (must also set GPIO_PRT4.DM3= 0_Z/Z_1). **0xF: SCB0_SPI_SSEL0** Pin is connected to SPI SSSEL (Slave Select) output #0 of SCB #1. This mode remains active and usable in DeepSleep mode.

5.1.5 HSIOM_PORT_SEL4 (continued)

11 : 8	HSIOM_SEL2	Selects pin 2 source. Default: 0x0 **0x6: CSD_CMOD** Pin is connected to external CSD Cmod capacitor used in sensing or REFBUF precharge mode. **0x7: CSD_CMOD_CHRG** Pin is connected to external CSD Cmod capacitor in GPIO pre-charge mode (must also set GPIO_PRT4.DM2= 0_Z/Z_1). **0xF: SCB0_SPI_CLK** Pin is connected to CLK pin of SPI #0. This mode remains active and usable in DeepSleep mode.
7 : 4	HSIOM_SEL1	Selects pin 1 source. Default: 0x0 **0x9: SCB0_UART_TX** Pin is connected to TX (transmit) input of UART #0. **0xE: SCB0_I2C_SDA** Pin is connected to SDA data pin of I2C #0. This mode remains active and usable in DeepSleep mode. **0xF: SCB0_SPI_MISO** Pin is connected to MISO pin of SPI #0. This mode remains active and usable in DeepSleep mode.
3 : 0	HSIOM_SEL0	Selects pin 0 source. Default: 0x0 **0x9: SCB0_UART_RX** Pin is connected to RX (receive) input of UART #0 **0xE: SCB0_I2C_SCL** Pin is connected to SCL (clock) pin of I2C #0. This mode remains active and usable in Deep-Sleep mode. **0xF: SCB0_SPI_MOSI** Pin is connected to MOSI pin of SPI #0. This mode remains active and usable in DeepSleep mode.

6 LCD Registers

This section discusses the LCD registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

6.1 LCD Register Mapping Overview

Register Name	Address
LCD_ID	0x40090000
LCD_DIVIDER	0x40090004
LCD_CONTROL	0x40090008
LCD_DATA0	0x40090100
LCD_DATA1	0x40090200
LCD_DATA2	0x40090300
LCD_DATA3	0x40090400

6.1.1 LCD_ID

Address: 0x40090000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LCD_REVISION [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LCD_REVISION [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LCD_ID [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LCD_ID [15: 0]							

ID Revision

Bits	Name	Description
31 : 16	LCD_REVISION	the version number is 0x0001 Default: 0x0001
15 : 0	LCD_ID	the ID of LCD controller peripheral is 0xF0F0 Default: 0xF0F0

6.1.2 LCD_DIVIDER

Address: 0x40090004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DEAD_DIV [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DEAD_DIV [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_SUBFR_DIV [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_SUBFR_DIV [15: 0]							

LCD Divider Register

Bits	Name	Description
31 : 16	LCD_DEAD_DIV	Length of the dead time period in cycles. When set to zero, no dead time period exists. Default: 0x0000
15 : 0	LCD_SUBFR_DIV	Input clock frequency divide value, to generate the 1/4 sub-frame period. The sub-frame period is 4*(SUBFR_DIV+1) cycles long. Default: 0x0000

6.1.3 LCD_CONTROL

Address: 0x40090008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	W	None						
SW Access	R	None						
Bit Name	LCD_LS_EN_STAT	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[15:12]				LCD_COM_NUM [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0		0x0	0x0	0x0	0x0	0x0
HW Access	None	R		R	R	R	R	R
SW Access	None	RW		RW	RW	RW	RW	RW
Bit Name	Reserved	LCD_BIAS [6:5]		LCD_OP_MODE	LCD_TYPE	LCD_LCD_MODE	LCD_HS_EN	LCD_LS_EN

LCD Configuration Register

Bits	Name	Description
31	LCD_LS_EN_STAT	LS enable status bit. This bit is a copy of LS_EN that is synchronized to the low speed clock domain and back to the system clock domain. Firmware can use this bit to observe whether LS_EN has taken effect in the low speed clock domain. Firmware should never change the configuration for the LS generator without ensuring this bit is 0. The following procedure should be followed to disable the LS generator: 1. If LS_EN=0 we are done. Exit the procedure. 2. Check that LS_EN_STAT=1. If not, wait until it is. This will catch the case of a recent enable (LS_EN=1) that has not taken effect yet. 3. Set LS_EN=0. 4. Wait until LS_EN_STAT=0. Default: 0x0

6.1.3 LCD_CONTROL (continued)

11 : 8	LCD_COM_NUM	The number of COM connections minus 2. So: 0: 2 COMs 1: 3 COMs ... 13: 15 COMs 14: 16 COMs 15: undefined Default: 0x0
6 : 5	LCD_BIAS	PWM bias selection Default: 0x0 **0x0: HALF** 1/2 Bias **0x1: THIRD** 1/3 Bias **0x2: FOURTH** 1/4 Bias (not supported by LS generator) **0x3: FIFTH** 1/5 Bias (not supported by LS generator)
4	LCD_OP_MODE	Driving mode configuration Default: 0x0 **0x0: PWM** PWM Mode **0x1: CORRELATION** Digital Correlation Mode
3	LCD_TYPE	LCD driving waveform type configuration. Default: 0x0 **0x0: TYPE_A** Type A - Each frame addresses each COM pin only once with a balanced (DC=0) waveform. **0x1: TYPE_B** Type B - Each frame addresses each COM pin twice in sequence with a positive and negative waveform that together are balanced (DC=0).
2	LCD_LCD_MODE	HS/LS Mode selection Default: 0x0 **0x0: LS** Select Low Speed (32kHz) Generator (Works in Active, Sleep and DeepSleep power modes). **0x1: HS** Select High Speed (system clock) Generator (Works in Active and Sleep power modes only).

6.1.3 LCD_CONTROL (continued)

1	LCD_HS_EN	High speed (HS) generator enable 1: enable 0: disable Default: 0x0
0	LCD_LS_EN	Low speed (LS) generator enable 1: enable 0: disable Default: 0x0

6.1.4 LCD_DATA0

Address: 0x40090100

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

LCD Pin Data Registers

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 1-4 (COM1 is lsb). Default: 0x00000000

6.1.5 LCD_DATA1

Address: 0x40090200

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

LCD Pin Data Registers

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 5-8 (COM5 is lsb). Default: 0x00000000

6.1.6 LCD_DATA2

Address: 0x40090300

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

LCD Pin Data Registers

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 9-12 (COM9 is lsb). Default: 0x00000000

6.1.7 LCD_DATA3

Address: 0x40090400

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	LCD_DATA [31: 0]							

LCD Pin Data Registers

Bits	Name	Description
31 : 0	LCD_DATA	Bits [4i+3:4i] represent the pin data for pin [i] for COMS 13-16 (COM13 is lsb). Default: 0x00000000

7 LPCOMP Registers

This section discusses the LPCOMP registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

7.1 LPCOMP Register Mapping Overview

Register Name	Address
LPCOMP_ID	0x400A0000
LPCOMP_CONFIG	0x400A0004
LPCOMP_DFT	0x400A0008
LPCOMP_INTR	0x400A000C
LPCOMP_INTR_SET	0x400A0010
LPCOMP_TRIM1	0x400AFF00
LPCOMP_TRIM2	0x400AFF04
LPCOMP_TRIM3	0x400AFF08
LPCOMP_TRIM4	0x400AFF0C

7.1.1 LPCOMP_ID

Address: 0x400A0000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LPCOMP_REVISION [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LPCOMP_REVISION [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LPCOMP_ID [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	R							
Bit Name	LPCOMP_ID [15: 0]							

ID Revision

Bits	Name	Description
31 : 16	LPCOMP_REVISION	the version number is 0x0001 Default: 0x0001
15 : 0	LPCOMP_ID	the ID of LPCOMP peripheral is 0xE0E0 Default: 0xE0E0

7.1.2 LPCOMP_CONFIG

Address: 0x400A0004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0		0x0	0x0	0x0	
HW Access	R	RW	R		R	R	R	
SW Access	RW	R	RW		RW	RW	RW	
Bit Name	LPCOMP_ENABLE2	LPCOMP_OUT2	LPCOMP_INTTYPE2 [13:12]		LPCOMP_FILTER2	LPCOMP_HYST2	LPCOMP_MODE2 [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0		0x0	0x0	0x0	
HW Access	R	RW	R		R	R	R	
SW Access	RW	R	RW		RW	RW	RW	
Bit Name	LPCOMP_ENABLE1	LPCOMP_OUT1	LPCOMP_INTTYPE1 [5:4]		LPCOMP_FILTER1	LPCOMP_HYST1	LPCOMP_MODE1 [1:0]	

LPCOMP Configuration Register

Bits	Name	Description
15	LPCOMP_ENABLE2	Enable comparator #2 Default: 0x0
14	LPCOMP_OUT2	Current output value of the comparator. Default: 0x0
13 : 12	LPCOMP_INTTYPE2	Sets which edge will trigger an IRQ Default: 0x0 **0x0: DISABLE** Disabled

7.1.2 LPCOMP_CONFIG (continued)

		0x1: RISING Rising edge **0x2: FALLING** Falling edge **0x3: BOTH** Both rising and falling edges
11	LPCOMP_FILTER2	Enable the inline digital filter for the comparator Default: 0x0
10	LPCOMP_HYST2	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default: 0x0
9 : 8	LPCOMP_MODE2	Operating mode for the comparator Default: 0x0 **0x0: SLOW** Slow operating mode (uses less power, lt;50uA) **0x1: FAST** Fast operating mode (uses more power, lt;400uA) **0x2: ULP** Ultra low power operting mode (uses ~2-4uA)
7	LPCOMP_ENABLE1	Enable comparator #1 Default: 0x0
6	LPCOMP_OUT1	Current output value of the comparator. Default: 0x0
5 : 4	LPCOMP_INTTYPE1	Sets which edge will trigger an IRQ Default: 0x0 **0x0: DISABLE** Disabled **0x1: RISING** Rising edge **0x2: FALLING** Falling edge **0x3: BOTH** Both rising and falling edges
3	LPCOMP_FILTER1	Enable the inline digital filter for the comparator Default: 0x0

7.1.2 LPCOMP_CONFIG (continued)

2	LPCOMP_HYST1	Add 10mV hysteresis to the comparator - 0: Enable Hysteresis - 1: Disable Hysteresis Default: 0x0
1 : 0	LPCOMP_MODE1	Operating mode for the comparator Default: 0x0 **0x0: SLOW** Slow operating mode (uses less power, lt;50uA) **0x1: FAST** Fast operating mode (uses more power, lt;400uA) **0x2: ULP** Ultra low power operting mode (uses ~2-4uA)

7.1.3 LPCOMP_DFT

Address: 0x400A0008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[7:2]						LPCOMP_BYPASS	LPCOMP_CAL_EN

LPCOMP DFT register

Bits	Name	Description
1	LPCOMP_BYPASS	Enables bypass of inp input straight to output. This can be used as baseline to measure comparator response time. Default: 0x0
0	LPCOMP_CAL_EN	Calibration enable. Setting this bit will short the inputs of the comparators for offset measurement. Default: 0x0

7.1.4 LPCOMP_INTR

Address: 0x400A000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						RW1S	RW1S
SW Access	None						RW1C	RW1C
Bit Name	Reserved[7:2]						LPCOMP_COMP2	LPCOMP_COMP1

LPCOMP Interrupt request register

Bits	Name	Description
1	LPCOMP_COMP2	Comparator #2 generated an interrupt Default: 0x0
0	LPCOMP_COMP1	Comparator #1 generated an interrupt Default: 0x0

7.1.5 LPCOMP_INTR_SET

Address: 0x400A0010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						None	None
SW Access	None						RW1S	RW1S
Bit Name	Reserved[7:2]						LPCOMP_COMP2	LPCOMP_COMP1

LPCOMP Interrupt set register

Bits	Name	Description
1	LPCOMP_COMP2	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
0	LPCOMP_COMP1	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

7.1.6 LPCOMP_TRIM1

Address: 0x400AFF00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			LPCOMP_COMP1_TRIMA [4:0]				

LPCOMP Trim Register

Bits	Name	Description
4 : 0	LPCOMP_COMP1_TRIMA	Trim A for Comparator #1 Default: 0x00

7.1.7 LPCOMP_TRIM2

Address: 0x400AFF04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			LPCOMP_COMP1_TRIMB [4:0]				

LPCOMP Trim Register

Bits	Name	Description
4 : 0	LPCOMP_COMP1_TRIMB	Trim B for Comparator #1 Default: 0x00

7.1.8 LPCOMP_TRIM3

Address: 0x400AFF08

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			LPCOMP_COMP2_TRIMA [4:0]				

LPCOMP Trim Register

Bits	Name	Description
4 : 0	LPCOMP_COMP2_TRIMA	Trim A for Comparator #2 Default: 0x00

7.1.9 LPCOMP_TRIM4

Address: 0x400AFF0C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			LPCOMP_COMP2_TRIMB [4:0]				

LPCOMP Trim Register

Bits	Name	Description
4 : 0	LPCOMP_COMP2_TRIMB	Trim B for Comparator #2 Default: 0x00

8 PCLK Registers

This section discusses the PCLK registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

8.1 PCLK Register Mapping Overview

Register Name	Address
CLK_DIVIDER_A	0x40020000
CLK_DIVIDER_B	0x40020040
CLK_DIVIDER_C	0x40020080
CLK_DIVIDER_FRAC_A	0x40020100
CLK_DIVIDER_FRAC_B	0x40020140
CLK_DIVIDER_FRAC_C	0x40020180
CLK_SELECT	0x40020200

8.1.1 CLK_DIVIDER_A

Address: 0x40020000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	CLK_ENABLE_A	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_A [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_A [15: 0]							

Clock Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_A	Enable divider A. Default: 0x0
15 : 0	CLK_DIVIDER_A	Divider value for divider A in the row. OUTPUT= INPUT / (DIVIDER_A+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Default: 0x0000

8.1.2 CLK_DIVIDER_B

Address: 0x40020040

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	CLK_ENABLE_B	CLK_CASCADE_A_B	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_B [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_B [15: 0]							

Clock Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_B	Enable divider B. Default: 0x0
30	CLK_CASCADE_A_B	Cascade divider A into divider B Default: 0x0
15 : 0	CLK_DIVIDER_B	Divider value for divider B in the row. OUTPUT= INPUT / (DIVIDER_B+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Also note that dividide by 1 does not work if CASCADE_A_B=1. Default: 0x0000

8.1.3 CLK_DIVIDER_C

Address: 0x40020080

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	CLK_ENABLE_C	CLK_CASCADE_B_C	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_C [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_C [15: 0]							

Clock Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_C	Enable divider C. Default: 0x0
30	CLK_CASCADE_B_C	Cascade divider B into divider C Default: 0x0
15 : 0	CLK_DIVIDER_C	Divider value for divider C in the row. OUTPUT= INPUT / (DIVIDER_C+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Also note that dividide by 1 does not work if CASCADE_A_B=1. Default: 0x0000

8.1.4 CLK_DIVIDER_FRAC_A

Address: 0x40020100

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	CLK_ENABLE_A	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[23:21]			CLK_FRAC_A [20:16]				

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_A [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_A [15: 0]							

Frac Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_A	Enable divider A. Default: 0x0
20 : 16	CLK_FRAC_A	Fractional divider value: 0/32 .. 31/32 Default: 0x00
15 : 0	CLK_DIVIDER_A	Divider value for divider A in the row. OUTPUT= INPUT / (DIVIDER_A+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Default: 0x0000

8.1.5 CLK_DIVIDER_FRAC_B

Address: 0x40020140

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	CLK_ENABLE_B	CLK_CASCADE_A_B	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[23:21]			CLK_FRAC_B [20:16]				

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_B [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_B [15: 0]							

Frac Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_B	Enable divider B. Default: 0x0
30	CLK_CASCADE_A_B	Cascade divider A into divider B Default: 0x0
20 : 16	CLK_FRAC_B	Fractional divider value: 0/32 .. 31/32 Default: 0x00
15 : 0	CLK_DIVIDER_B	Divider value for divider B in the row. OUTPUT= INPUT / (DIVIDER_B+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Also note that dividide by 1 does not work if CASCADE_A_B=1. Default: 0x0000

8.1.6 CLK_DIVIDER_FRAC_C

Address: 0x40020180

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	CLK_ENABLE_C	CLK_CASCADE_B_C	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[23:21]			CLK_FRAC_C [20:16]				

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_C [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	CLK_DIVIDER_C [15: 0]							

Frac Divider Configuration

Bits	Name	Description
31	CLK_ENABLE_C	Enable divider C. Default: 0x0
30	CLK_CASCADE_B_C	Cascade divider B into divider C Default: 0x0
20 : 16	CLK_FRAC_C	Fractional divider value: 0/32 .. 31/32 Default: 0x00
15 : 0	CLK_DIVIDER_C	Divider value for divider C in the row. OUTPUT= INPUT / (DIVIDER_C+1). In other words, a value of 0 means divide by 1. Note that selecting divide by 1 (value 0) does not work for blocks that require full DIVIDED_CLOCK clock reconstruction (See Section 20.6 in SAS). Also note that dividide by 1 does not work if CASCADE_A_B=1. Default: 0x0000

8.1.7 CLK_SELECT

Address: 0x40020200

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0		0x0			
HW Access	None		R		R			
SW Access	None		RW		RW			
Bit Name	Reserved[7:6]		CLK_DIVIDER_ABC [5:4]		CLK_DIVIDER_N [3:0]			

Clock Routing Configuration

Bits	Name	Description
5 : 4	CLK_DIVIDER_ABC	Select which divider from row to use. Default: 0x0 **0x0: OFF** Clock disabled **0x1: A** Divider N-A **0x2: B** Divider N-B

8.1.7 CLK_SELECT (continued)

		0x3: C Divider N-C
3 : 0	CLK_DIVIDER_N	Select divider bank row to source clock from. Addressed as following: 0 to NUMDIV-1: Non-fractional divider NUMDIV to NUMFRACDIV: Fractional divider E.g. PSOC4A NUMDIV=3, NUMFRACDIV=1 0 to 2: non-fractional divider 0 to 2 3: fractional divider 0 Default: 0x0

9 SAR Registers

This section discusses the SAR registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

9.1 SAR Register Mapping Overview

Register Name	Address
SAR_CTRL	0x401A0000
SAR_SAMPLE_CTRL	0x401A0004
SAR_SAMPLE_TIME01	0x401A0010
SAR_SAMPLE_TIME23	0x401A0014
SAR_RANGE_THRES	0x401A0018
SAR_RANGE_COND	0x401A001C
SAR_CHAN_EN	0x401A0020
SAR_START_CTRL	0x401A0024
SAR_DFT_CTRL	0x401A0030
SAR_CHAN_CONFIG	0x401A0080
SAR_CHAN_WORK	0x401A0100
SAR_CHAN_RESULT	0x401A0180
SAR_CHAN_WORK_VALID	0x401A0200
SAR_CHAN_RESULT_VALID	0x401A0204
SAR_STATUS	0x401A0208
SAR_AVG_STAT	0x401A020C
SAR_INTR	0x401A0210
SAR_INTR_SET	0x401A0214
SAR_INTR_MASK	0x401A0218
SAR_INTR_MASKED	0x401A021C
SAR_SATURATE_INTR	0x401A0220
SAR_SATURATE_INTR_SET	0x401A0224
SAR_SATURATE_INTR_MASK	0x401A0228
SAR_SATURATE_INTR_MASKED	0x401A022C
SAR_RANGE_INTR	0x401A0230
SAR_RANGE_INTR_SET	0x401A0234

Register Name	Address
SAR_RANGE_INTR_MASK	0x401A0238
SAR_RANGE_INTR_MASKED	0x401A023C
SAR_INTR_CAUSE	0x401A0240
SAR_INJ_CHAN_CONFIG	0x401A0280
SAR_INJ_RESULT	0x401A0290
SAR_MUX_SWITCH0	0x401A0300
SAR_MUX_SWITCH_CLEAR0	0x401A0304
SAR_MUX_SWITCH1	0x401A0308
SAR_MUX_SWITCH_CLEAR1	0x401A030C
SAR_MUX_SWITCH_HW_CTRL	0x401A0340
SAR_MUX_SWITCH_STATUS	0x401A0348
SAR_PUMP_CTRL	0x401A0380
SAR_ANA_TRIM	0x401A0F00
SAR_WOUNDING	0x401A0F04

9.1.1 SAR_CTRL

Address: 0x401A0000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	0x1	None		0x0	
HW Access	R	R	R	R	None		R	
SW Access	RW	RW	RW	RW	None		RW	
Bit Name	SAR_ENABLED	SAR_SWITCH_DISABLE	SAR_DSI_MODE	SAR_DSI_SYNC_CONFIG	Reserved[27:26]		SAR_ICONT_LV [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[23:20]				SAR_SPARE [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0		0x0	None	0x0			None
HW Access	R		R	None	R			None
SW Access	RW		RW	None	RW			None
Bit Name	SAR_PWR_CTRL_VREF [15:14]		SAR_SAR_HW_CTRL_NEGVREF	Reserved	SAR_NEG_SEL [11:9]			Reserved

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0			None			
HW Access	R	R			None			
SW Access	RW	RW			None			
Bit Name	SAR_VREF_BYP_CAP_EN	SAR_VREF_SEL [6:4]			Reserved[3:0]			

Analog control register.

Bits	Name	Description
31	SAR_ENABLED	- 0: SAR IP disabled (put analog in power down and stop clocks), also can clear FW_TRIGGER and INJ_START_EN (if not tailgaiting) on write. - 1: SAR IP enabled. Default: 0x0

9.1.1 SAR_CTRL (continued)

30	SAR_SWITCH_DISABLE	Disable SAR sequencer from enabling routing switches (note DSI and firmware can always close switches independent of this control) - 0: Normal mode, SAR sequencer changes switches according to pin address in channel configurations - 1: Switches disabled, SAR sequencer does not enable any switches, it is the responsibility of the firmware or UDBs (through DSI) to set the switches to route the signal to be converted through the SARMUX Default: 0x0
29	SAR_DSI_MODE	SAR sequencer takes configuration from DSI signals (note this also has the same effect as SWITCH_DISABLE==1) - 0: Normal mode, SAR sequencer operates according to CHAN_EN enables and CHAN_CONFIG channel configurations - 1: CHAN_EN, INJ_START_EN and channel configurations in CHAN_CONFIG and INJ_CHAN_CONFIG are ignored Default: 0x0
28	SAR_DSI_SYNC_CONFIG	- 0: bypass clock domain synchronisation of the DSI config signals. - 1: synchronize the DSI config signals to peripheral clock domain. Default: 0x1
25 : 24	SAR_ICONT_LV	SARADC low power mode. Default: 0x0 **0x0: NORMAL_PWR** normal power (default), max clk_sar is 18MHz. **0x1: HALF_PWR** 1/2 power mode, max clk_sar is 9MHz. **0x2: MORE_PWR** 1.333 power mode, max clk_sar is 18MHz. **0x3: QUARTER_PWR** 1/4 power mode, max clk_sar is 4.5MHz.
19 : 16	SAR_SPARE	Spare controls, not yet designated, for late changes done with an ECO Default: 0x0
15 : 14	SAR_PWR_CTRL_VREF	VREF buffer low power mode. Default: 0x0 **0x0: NORMAL_PWR** normal power (default), no bypass cap, max clk_sar is 3MHz. **0x1: HALF_PWR** 1/2 power mode, no bypass cap, max clk_sar is 1.5MHz. **0x2: THIRD_PWR** 1/3 power mode, no bypass cap, max clk_sar is 1MHz. **0x3: QUARTER_PWR** 1/4 power mode, with bypass cap, max clk_sar is 18MHz.

9.1.1 SAR_CTRL (continued)

13	SAR_SAR_HW_CTRL_NEGVREF	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for VREF to NEG switch. Default: 0x0
11 : 9	SAR_NEG_SEL	SARADC internal NEG selection for Single ended conversion Default: 0x0 **0x0: VSSA_KELVIN** NEG input of SARADC is connected to vssa_kelvin, gives more precision around zero. Note this opens both SARADC internal switches, therefore use this value to insert a break-before-make cycle on those switches when SWITCH_DISABLE is high. **0x1: ART_VSSA** NEG input of SARADC is connected to VSSA in AROUTE close to the SARADC **0x2: P1** NEG input of SARADC is connected to P1 pin of SARMUX **0x3: P3** NEG input of SARADC is connected to P3 pin of SARMUX **0x4: P5** NEG input of SARADC is connected to P5 pin of SARMUX **0x5: P7** NEG input of SARADC is connected to P7 pin of SARMUX **0x6: ACORE** NEG input of SARADC is connected to an ACORE in AROUTE **0x7: VREF** NEG input of SARADC is shorted with VREF input of SARADC.
7	SAR_VREF_BYP_CAP_EN	VREF bypass cap enable for when VREF buffer is on Default: 0x0
6 : 4	SAR_VREF_SEL	SARADC internal VREF selection. Default: 0x0 **0x0: VREF0** VREF0 from PRB (VREF buffer on) **0x1: VREF1** VREF1 from PRB (VREF buffer on) **0x2: VREF2** VREF2 from PRB (VREF buffer on) **0x3: VREF_AROUTE** VREF from AROUTE (VREF buffer on)

9.1.1 SAR_CTRL (continued)

0x4: VBGR
1.024V from BandGap (VREF buffer on)

0x5: VREF_EXT
External precision Vref direct from a pin (low impedance path).

0x6: VDDA_DIV_2
Vdda/2 (VREF buffer on)

0x7: VDDA
Vdda.

9.1.2 SAR_SAMPLE_CTRL

Address: 0x401A0004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SAR_EOS_DSI_OUT_EN	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0x1	0x0	0x0	0x0
HW Access	None				R	R	R	R
SW Access	None				RW	RW	RW	RW
Bit Name	Reserved[23:20]				SAR_DSI_SYNC_TRIGGER	SAR_DSI_TRIGGER_LEVEL	SAR_DSI_TRIGGER_EN	SAR_CONTINUOUS

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0			0x1	0x0	0x0	0x0
HW Access	R	R			R	R	R	R
SW Access	RW	RW			RW	RW	RW	RW
Bit Name	SAR_AVG_SHIFT	SAR_AVG_CNT [6:4]			SAR_DIFFERENTIAL_SIGNED	SAR_SINGLE_ENDED_SIGNED	SAR_LEFT_ALIGN	SAR_SUB_RESOLU-TION

Sample control register.

Bits	Name	Description
31	SAR_EOS_DSI_OUT_EN	Enable to output EOS_INTR to DSI. When enabled each time EOS_INTR is set by the hardware also a pulse is send on the dsi_eos signal. Default: 0x0

9.1.2 SAR_SAMPLE_CTRL (continued)

19	SAR_DSI_SYNC_TRIGGER	- 0: bypass clock domain synchronisation of the DSI trigger signal. - 1: synchronize the DSI trigger signal to the SAR clock domain, if needed an edge detect is done in the peripheral clock domain. Default: 0x1
18	SAR_DSI_TRIGGER_LEVEL	- 0: DSI trigger signal is a pulse input, a positive edge detected on the DSI trigger signal triggers a new scan. - 1: DSI trigger signal is a level input, as long as the DSI trigger signal remains high the SAR will do continuous scans. Default: 0x0
17	SAR_DSI_TRIGGER_EN	- 0: firmware trigger only: disable hardware (DSI) trigger. - 1: enable hardware (DSI) trigger (e.g. from TCPWM, GPIO or UDB). Default: 0x0
16	SAR_CONTINUOUS	- 0: Wait for next FW_TRIGGER (one shot) or hardware (DSI) trigger (e.g. from TPWM for periodic triggering) before scanning enabled channels. - 1: Continuously scan enabled channels, ignore triggers. Default: 0x0
7	SAR_AVG_SHIFT	Averaging shifting: after averaging the result is shifted right to fit in the sample resolution, i.e. 12 bits. Default: 0x0
6 : 4	SAR_AVG_CNT	Averaging Count for channels that have over sampling enabled (AVG_EN). A channel will be sampled back to back (1lt;lt;(AVG_CNT+1)) = [2..256] times before the result is stored and the next enabled channel is sampled (1st order accumulate and dump filter). If shifting is not enabled (AVG_SHIFT=0) then the result is forced to shift right so that is fits in 16 bits, so right shift is done by max(0,AVG_CNT-3). Default: 0x0
3	SAR_DIFFERENTIAL_SIGNED	Output data from a differential conversion as a signed value Default: 0x1 **0x0: UNSIGNED** result data is unsigned (zero extended if needed) **0x1: SIGNED** Default: result data is signed (sign extended if needed)
2	SAR_SINGLE_ENDED_SIGNED	Output data from a single ended conversion as a signed value Default: 0x0 **0x0: UNSIGNED** Default: result data is unsigned (zero extended if needed) **0x1: SIGNED** result data is signed (sign extended if needed)
1	SAR_LEFT_ALIGN	Left align data in data[15:0], default data is right aligned in data[11:0], with sign extension to 16 bits if the channel is differential. Default: 0x0
0	SAR_SUB_RESOLUTION	Conversion resolution for channels that have sub-resolution enabled (RESOLUTION=1) (otherwise resolution is 12-bit). Default: 0x0 **0x0: 8B** 8-bit.

9.1.2 SAR_SAMPLE_CTRL (continued)

0x1: 10B
10-bit.

9.1.3 SAR_SAMPLE_TIME01

Address: 0x401A0010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None						0x004	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[31:26]						SAR_SAMPLE_TIME1 [25:16]	

Bits	23	22	21	20	19	18	17	16
Reset Value	0x004							
HW Access	R							
SW Access	RW							
Bit Name	SAR_SAMPLE_TIME1 [25 : 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x004	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						SAR_SAMPLE_TIME0 [9:0]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x004							
HW Access	R							
SW Access	RW							
Bit Name	SAR_SAMPLE_TIME0 [9 : 0]							

Sample time specification ST0 and ST1

Bits	Name	Description
25 : 16	SAR_SAMPLE_TIME1	Sample time1 Default: 0x004
9 : 0	SAR_SAMPLE_TIME0	Sample time0 (aperture) in ADC clock cycles. Minimum sample time is 222ns, which is 4 cycles with an 18MHz clock. Minimum legal value in this register is 1. Default: 0x004

9.1.4 SAR_SAMPLE_TIME23

Address: 0x401A0014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None						0x004	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[31:26]						SAR_SAMPLE_TIME3 [25:16]	

Bits	23	22	21	20	19	18	17	16
Reset Value	0x004							
HW Access	R							
SW Access	RW							
Bit Name	SAR_SAMPLE_TIME3 [25 : 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x004	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						SAR_SAMPLE_TIME2 [9:0]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x004							
HW Access	R							
SW Access	RW							
Bit Name	SAR_SAMPLE_TIME2 [9 : 0]							

Sample time specification ST2 and ST3

Bits	Name	Description
25 : 16	SAR_SAMPLE_TIME3	Sample time3 Default: 0x004
9 : 0	SAR_SAMPLE_TIME2	Sample time2 Default: 0x004

9.1.5 SAR_RANGE_THRES

Address: 0x401A0018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SAR_RANGE_HIGH [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SAR_RANGE_HIGH [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SAR_RANGE_LOW [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SAR_RANGE_LOW [15: 0]							

Global range detect threshold register.

Bits	Name	Description
31 : 16	SAR_RANGE_HIGH	high threshold for range detect Default: 0x0000
15 : 0	SAR_RANGE_LOW	low threshold for range detect Default: 0x0000

9.1.6 SAR_RANGE_COND

Address: 0x401A001C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None					
HW Access	R		None					
SW Access	RW		None					
Bit Name	SAR_RANGE_COND [31:30]		Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

Global range detect mode register.

Bits	Name	Description
31 : 30	SAR_RANGE_COND	Range condition select. Default: 0x0 **0x0: BELOW** result lt; RANGE_LOW **0x1: INSIDE** RANGE_LOW lt;= result lt; RANGE_HIGH **0x2: ABOVE** RANGE_HIGH lt;= result

9.1.6 SAR_RANGE_COND (continued)

0x3: OUTSIDE
result lt; RANGE_LOW || RANGE_HIGH lt;= result

9.1.7 SAR_CHAN_EN

Address: 0x401A0020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SAR_CHAN_EN [7:0]							

Enable bits for the channels

Bits	Name	Description
7 : 0	SAR_CHAN_EN	Channel enable. - 0: the corresponding channel is disabled. - 1: the corresponding channel is enabled, it will be included in the next scan. Default: 0x00

9.1.8 SAR_START_CTRL

Address: 0x401A0024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							RW1C
SW Access	None							RW1S
Bit Name	Reserved[7:1]							SAR_FW_TRIGGER

Start control register (firmware trigger).

Bits	Name	Description
0	SAR_FW_TRIGGER	When firmware writes a 1 here it will trigger the next scan of enabled channels, hardware clears this bit when the scan started with this trigger is completed. If scanning continuously the trigger is ignored and hardware clears this bit after the next scan is done. This bit is also cleared when the SAR is disabled. Default: 0x0

9.1.9 SAR_DFT_CTRL

Address: 0x401A0030

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None	0x1	0x0	0x0			
HW Access	R	None	R	R	R			
SW Access	RW	None	RW	RW	RW			
Bit Name	SAR_ADFT_OVERRIDE	Reserved	SAR_DCEN	SAR_EN_CSEL_DFT	SAR_SEL_CSEL_DFT [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None	0x0			0x0			
HW Access	None	R			R			
SW Access	None	RW			RW			
Bit Name	Reserved	SAR_DFT_OUTC [22:20]			SAR_DFT_INC [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x1	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[7:2]						SAR_HIZ	SAR_DLY_INC

DFT control register.

Bits	Name	Description
31	SAR_ADFT_OVERRIDE	During deepsleep/ hibernate mode keep SARMUX active, i.e. do not open all switches (disconnect), to be used for ADFT Default: 0x0
29	SAR_DCEN	Delay Control Enable for latch. - 0: doubles the latch enable time. - 1: normal latch enable time (default). Default: 0x1
28	SAR_EN_CSEL_DFT	Mux select signal for DAC control Default: 0x0

9.1.9 SAR_DFT_CTRL (continued)

27 : 24	SAR_SEL_CSEL_DFT	Usage 1: DFT bits for DAC array Usage 2: For [0]=1 (when dcen=0): Delay timing for latch enable increased by 20% [1]=1: comparator preamp power level increased by 25% Default: 0x0
22 : 20	SAR_DFT_OUTC	DFT control for preamp outputs Default: 0x0
19 : 16	SAR_DFT_INC	DFT control for preamp inputs Default: 0x0
1	SAR_HIZ	DFT control for getting higher input impedance Default: 0x1
0	SAR_DLY_INC	DFT control: Control for delay circuits on sampling phase, =1 doubes the non-overlap delay Default: 0x0

9.1.10 SAR_CHAN_CONFIG

Address: 0x401A0080

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SAR_DSI_OUT_EN	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x0		None	0x0	0x0	0x0
HW Access	None		R		None	R	R	R
SW Access	None		RW		None	RW	RW	RW
Bit Name	Reserved[15:14]		SAR_SAMPLE_TIME_SEL [13:12]		Reserved	SAR_AVG_EN	SAR_RESOLUTION	SAR_DIFFERENTIAL_EN

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0			None	0x0		
HW Access	None	R			None	R		
SW Access	None	RW			None	RW		
Bit Name	Reserved	SAR_PORT_ADDR [6:4]			Reserved	SAR_PIN_ADDR [2:0]		

Channel configuration register.

Bits	Name	Description
31	SAR_DSI_OUT_EN	DSI data output enable for this channel. - 0: the conversion result for this channel is only stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. - 1: the conversion result for this channel is stored in the channel data register and the corresponding CHAN_DATA_VALID bit is set. The same data (same formating), together with the channel number, is sent out on the DSI communication channel for processing in UDBs. Default: 0x0
13 : 12	SAR_SAMPLE_TIME_SEL	Sample time select: select which of the 4 global sample times to use for this channel Default: 0x0

9.1.10 SAR_CHAN_CONFIG (continued)

10	SAR_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default: 0x0
9	SAR_RESOLUTION	Resolution for this channel. When AVG_EN is set this bit is ignored and always a 12-bit resolution is used for this channel. Default: 0x0 **0x0: 12B** 12-bit resolution is used for this channel. **0x1: SUBRES** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	SAR_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (PIN_ADDR[0] is ignored). Default: 0x0
6 : 4	SAR_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default: 0x0 **0x0: SARMUX** SARMUX pins. **0x1: CTB0** CTB0 **0x2: CTB1** CTB1 **0x3: CTB2** CTB2 **0x4: CTB3** CTB3 **0x6: AROUTE_VIRT** AROUTE virtual port **0x7: SARMUX_VIRT** SARMUX virtual port
2 : 0	SAR_PIN_ADDR	Address of the pin to be sampled by this channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default: 0x0

9.1.11 SAR_CHAN_WORK

Address: 0x401A0100

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	W	None						
SW Access	R	None						
Bit Name	SAR_CHAN_WORK_VALID_MIR	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	SAR_WORK [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	SAR_WORK [15: 0]							

Channel working data register

Bits	Name	Description
31	SAR_CHAN_WORK_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_WORK_VALID register Default: 0x0
15 : 0	SAR_WORK	SAR conversion working data of the channel. The data is written here right after sampling this channel. Default: 0x0000

9.1.12 SAR_CHAN_RESULT

Address: 0x401A0180

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	None				
HW Access	W	W	W	None				
SW Access	R	R	R	None				
Bit Name	SAR_CHAN_RESULT_VALID_MIR	SAR_RANGE_INTR_MIR	SAR_SATURATE_INTR_MIR	Reserved[28:24]				

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SAR_RESULT [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SAR_RESULT [15: 0]							

Channel result data register

Bits	Name	Description
31	SAR_CHAN_RESULT_VALID_MIR	mirror bit of corresponding bit in SAR_CHAN_RESULT_VALID register Default: 0x0
30	SAR_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_RANGE_INTR register Default: 0x0
29	SAR_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_SATURATE_INTR register Default: 0x0
15 : 0	SAR_RESULT	SAR conversion result of the channel. The data is copied here from the WORK field after all enabled channels in this scan have been sampled. Default: 0x0000

9.1.13 SAR_CHAN_WORK_VALID

Address: 0x401A0200

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	R							
Bit Name	SAR_CHAN_WORK_VALID [7:0]							

Channel working data register valid bits

Bits	Name	Description
7 : 0	SAR_CHAN_WORK_VALID	If set the corresponding WORK data is valid, i.e. was already sampled during the current scan. Default: 0x00

9.1.14 SAR_CHAN_RESULT_VALID

Address: 0x401A0204

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	R							
Bit Name	SAR_CHAN_RESULT_VALID [7:0]							

Channel result data register valid bits

Bits	Name	Description
7 : 0	SAR_CHAN_RESULT_VALID	If set the corresponding RESULT data is valid, i.e. was sampled during the last scan. Default: 0x00

9.1.15 SAR_STATUS

Address: 0x401A0208

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	W	W	None					
SW Access	R	R	None					
Bit Name	SAR_BUSY	SAR_SW_VREF_NEG	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			W				
SW Access	None			R				
Bit Name	Reserved[7:5]			SAR_CUR_CHAN [4:0]				

Current status of internal SAR registers (mostly for debug)

Bits	Name	Description
31	SAR_BUSY	If high then the SAR is busy with a conversion. This bit is always high when CONTINUOUS is set. Firmware should wait for this bit to be low before putting the SAR in power down. Default: 0x0
30	SAR_SW_VREF_NEG	the current switch status, including DSI and sequencer controls, of the switch in the SARADC that shorts NEG with VREF input (see NEG_SEL). Default: 0x0
4 : 0	SAR_CUR_CHAN	current channel being sampled (channel 16 indicates the injection channel), only valid if BUSY. Default: 0x00

9.1.16 SAR_AVG_STAT

Address: 0x401A020C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00							
HW Access	W							
SW Access	R							
Bit Name	SAR_CUR_AVG_CNT [31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0x00000			
HW Access	None				W			
SW Access	None				R			
Bit Name	Reserved[23:20]				SAR_CUR_AVG_ACCU [19:0]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000							
HW Access	W							
SW Access	R							
Bit Name	SAR_CUR_AVG_ACCU [19 : 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000							
HW Access	W							
SW Access	R							
Bit Name	SAR_CUR_AVG_ACCU [19 : 0]							

Current averaging status (for debug)

Bits	Name	Description
31 : 24	SAR_CUR_AVG_CNT	the current value of the averaging counter. Note that the value shown is updated after the sampling time and therefore runs ahead of the accumulator update. Default: 0x00
19 : 0	SAR_CUR_AVG_ACCU	the current value of the averaging accumulator Default: 0x00000

9.1.17 SAR_INTR

Address: 0x401A0210

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	SAR_INJ_COLLISION_INTR	SAR_INJ_RANGE_INTR	SAR_INJ_SATURATE_INTR	SAR_INJ_EOC_INTR	SAR_DSI_COLLISION_INTR	SAR_FW_COLLISION_INTR	SAR_OVERFLOW_INTR	SAR_EOS_INTR

Interrupt request register.

Bits	Name	Description
7	SAR_INJ_COLLISION_INTR	Injection Collision Interrupt: hardware sets this interrupt when the injection trigger signal is asserted (INJ_START_EN==1 INJ_TAILGATING==0) while the SAR is BUSY. Raising this interrupt is delayed to when the sampling of the injection channel has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the injection channel was sampled later than was intended. Write with 1 to clear bit. Default: 0x0
6	SAR_INJ_RANGE_INTR	Injection Range detect Interrupt: hardware sets this interrupt if the injection conversion result (after averaging) met the condition specified by the SAR_RANGE registers. Write with 1 to clear bit. Default: 0x0

9.1.17 SAR_INTR (continued)

5	SAR_INJ_SATURATE_INTR	Injection Saturation Interrupt: hardware sets this interrupt if an injection conversion result (before averaging) is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with 1 to clear bit. Default: 0x0
4	SAR_INJ_EOC_INTR	Injection End of Conversion Interrupt: hardware sets this interrupt after completing the conversion for the injection channel (irrespective of if tailgating was used). Write with 1 to clear bit. Default: 0x0
3	SAR_DSI_COLLISION_INTR	DSI Collision Interrupt: hardware sets this interrupt when the DSI trigger signal is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the DSI trigger has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with 1 to clear bit. Default: 0x0
2	SAR_FW_COLLISION_INTR	Firmware Collision Interrupt: hardware sets this interrupt when FW_TRIGGER is asserted while the SAR is BUSY. Raising this interrupt is delayed to when the scan caused by the FW_TRIGGER has been completed, i.e. not when the preceeding scan with which this trigger collided is completed. When this interrupt is set it implies that the channels were sampled later than was intended (jitter). Write with 1 to clear bit. Default: 0x0
1	SAR_OVERFLOW_INTR	Overflow Interrupt: hardware sets this interrupt when it sets a new EOS_INTR while that bit was not yet cleared by the firmware. Write with 1 to clear bit. Default: 0x0
0	SAR_EOS_INTR	End Of Scan Interrupt: hardware sets this interrupt after completing a scan of all the enabled channels. Write with 1 to clear bit. Default: 0x0

9.1.18 SAR_INTR_SET

Address: 0x401A0214

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	SAR_INJ_COLLISION_SET	SAR_INJ_RANGE_SET	SAR_INJ_SATURATE_SET	SAR_INJ_EOC_SET	SAR_DSI_COLLISION_SET	SAR_FW_COLLISION_SET	SAR_OVERFLOW_SET	SAR_EOS_SET

Interrupt set request register

Bits	Name	Description
7	SAR_INJ_COLLISION_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
6	SAR_INJ_RANGE_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
5	SAR_INJ_SATURATE_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
4	SAR_INJ_EOC_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
3	SAR_DSI_COLLISION_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

9.1.18 SAR_INTR_SET (continued)

2	SAR_FW_COLLISION_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
1	SAR_OVERFLOW_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
0	SAR_EOS_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

9.1.19 SAR_INTR_MASK

Address: 0x401A0218

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	SAR_INJ_COLLISION_MASK	SAR_INJ_RANGE_MASK	SAR_INJ_SATURATE_MASK	SAR_INJ_EOC_MASK	SAR_DSI_COLLISION_MASK	SAR_FW_COLLISION_MASK	SAR_OVERFLOW_MASK	SAR_EOS_MASK

Interrupt mask register.

Bits	Name	Description
7	SAR_INJ_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
6	SAR_INJ_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
5	SAR_INJ_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
4	SAR_INJ_EOC_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
3	SAR_DSI_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0

9.1.19 SAR_INTR_MASK (continued)

2	SAR_FW_COLLISION_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
1	SAR_OVERFLOW_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SAR_EOS_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x0

9.1.20 SAR_INTR_MASKED

Address: 0x401A021C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SAR_INJ_COLLISION_MASKED	SAR_INJ_RANGE_MASKED	SAR_INJ_SATURATE_MASKED	SAR_INJ_EOC_MASKED	SAR_DSI_COLLISION_MASKED	SAR_FW_COLLISION_MASKED	SAR_OVERFLOW_MASKED	SAR_EOS_MASKED

Interrupt masked request register

Bits	Name	Description
7	SAR_INJ_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
6	SAR_INJ_RANGE_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
5	SAR_INJ_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
4	SAR_INJ_EOC_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
3	SAR_DSI_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default: 0x0

9.1.20 SAR_INTR_MASKED (continued)

2	SAR_FW_COLLISION_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
1	SAR_OVERFLOW_MASKED	Logical and of corresponding request and mask bits. Default: 0x0
0	SAR_EOS_MASKED	Logical and of corresponding request and mask bits. Default: 0x0

9.1.21 SAR_SATURATE_INTR

Address: 0x401A0220

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW1S							
SW Access	RW1C							
Bit Name	SAR_SATURATE_INTR [7:0]							

Saturate interrupt request register.

Bits	Name	Description
7 : 0	SAR_SATURATE_INTR	Saturate Interrupt: hardware sets this interrupt for each channel if a conversion result (before averaging) of that channel is either 0x000 or 0xFFF (for 12-bit resolution), this is an indication that the ADC likely saturated. Write with 1 to clear bit. Default: 0x00

9.1.22 SAR_SATURATE_INTR_SET

Address: 0x401A0224

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW1S							
Bit Name	SAR_SATURATE_SET [7:0]							

Saturate interrupt set request register

Bits	Name	Description
7 : 0	SAR_SATURATE_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x00

9.1.23 SAR_SATURATE_INTR_MASK

Address: 0x401A0228

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SAR_SATURATE_MASK [7:0]							

Saturate interrupt mask register.

Bits	Name	Description
7 : 0	SAR_SATURATE_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x00

9.1.24 SAR_SATURATE_INTR_MASKED

Address: 0x401A022C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	W							
SW Access	R							
Bit Name	SAR_SATURATE_MASKED [7:0]							

Saturate interrupt masked request register

Bits	Name	Description
7 : 0	SAR_SATURATE_MASKED	Logical and of corresponding request and mask bits. Default: 0x00

9.1.25 SAR_RANGE_INTR

Address: 0x401A0230

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW1S							
SW Access	RW1C							
Bit Name	SAR_RANGE_INTR [7:0]							

Range detect interrupt request register.

Bits	Name	Description
7 : 0	SAR_RANGE_INTR	Range detect Interrupt: hardware sets this interrupt for each channel if the conversion result (after averaging) of that channel met the condition specified by the SAR_RANGE registers. Write with 1 to clear bit. Default: 0x00

9.1.26 SAR_RANGE_INTR_SET

Address: 0x401A0234

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW1S							
Bit Name	SAR_RANGE_SET [7:0]							

Range detect interrupt set request register

Bits	Name	Description
7 : 0	SAR_RANGE_SET	Write with 1 to set corresponding bit in interrupt request register. Default: 0x00

9.1.27 SAR_RANGE_INTR_MASK

Address: 0x401A0238

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SAR_RANGE_MASK [7:0]							

Range detect interrupt mask register.

Bits	Name	Description
7 : 0	SAR_RANGE_MASK	Mask bit for corresponding bit in interrupt request register. Default: 0x00

9.1.28 SAR_RANGE_INTR_MASKED

Address: 0x401A023C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	W							
SW Access	R							
Bit Name	SAR_RANGE_MASKED [7:0]							

Range interrupt masked request register

Bits	Name	Description
7 : 0	SAR_RANGE_MASKED	Logical and of corresponding request and mask bits. Default: 0x00

9.1.29 SAR_INTR_CAUSE

Address: 0x401A0240

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	W	W	None					
SW Access	R	R	None					
Bit Name	SAR_RANGE_MASKED_RED	SAR_SATURATE_MASKED_RED	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SAR_INJ_COLLISION_MASKED_MIR	SAR_INJ_RANGE_MASKED_MIR	SAR_INJ_SATURATE_MASKED_MIR	SAR_INJ_EOC_MASKED_MIR	SAR_DSI_COLLISION_MASKED_MIR	SAR_FW_COLLISION_MASKED_MIR	SAR_OVERFLOW_MASKED_MIR	SAR_EOS_MASKED_MIR

Interrupt cause register

Bits	Name	Description
31	SAR_RANGE_MASKED_RED	Reduction OR of all SAR_RANGE_INTR_MASKED bits Default: 0x0
30	SAR_SATURATE_MASKED_RED	Reduction OR of all SAR_SATURATION_INTR_MASKED bits Default: 0x0
7	SAR_INJ_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0

9.1.29 SAR_INTR_CAUSE (continued)

6	SAR_INJ_RANGE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
5	SAR_INJ_SATURATE_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
4	SAR_INJ_EOC_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
3	SAR_DSI_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
2	SAR_FW_COLLISION_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
1	SAR_OVERFLOW_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0
0	SAR_EOS_MASKED_MIR	Mirror copy of corresponding bit in SAR_INTR_MASKED Default: 0x0

9.1.30 SAR_INJ_CHAN_CONFIG

Address: 0x401A0280

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	RW1C	R	None					
SW Access	RW1S	RW	None					
Bit Name	SAR_INJ_START_EN	SAR_INJ_TAILGATING	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x0		None	0x0	0x0	0x0
HW Access	None		R		None	R	R	R
SW Access	None		RW		None	RW	RW	RW
Bit Name	Reserved[15:14]		SAR_INJ_SAMPLE_TIME_SEL [13:12]		Reserved	SAR_INJ_AVG_EN	SAR_INJ_RESOLUTION	SAR_INJ_DIFFERENTIAL_EN

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0			None	0x0		
HW Access	None	R			None	R		
SW Access	None	RW			None	RW		
Bit Name	Reserved	SAR_INJ_PORT_ADDR [6:4]			Reserved	SAR_INJ_PIN_ADDR [2:0]		

Injection channel configuration register.

Bits	Name	Description
31	SAR_INJ_START_EN	Set by firmware to enable the injection channel. If INJ_TAILGATING is not set this bit also functions as trigger for this channel. Cleared by hardware after this channel has been sampled (i.e. this channel is always one shot even if CONTINUOUS is set). Also cleared if the SAR is disabled. Default: 0x0
30	SAR_INJ_TAILGATING	Injection channel tailgating. - 0: no tailgating for this channel, SAR is immediately triggered when the INJ_START_EN bit is set. - 1: injection channel tailgating. The addressed pin is sampled after the next trigger and after all enabled channels have been scanned. Default: 0x0

9.1.30 SAR_INJ_CHAN_CONFIG (continued)

13 : 12	SAR_INJ_SAMPLE_TIME_SEL	Injection sample time select: select which of the 4 global sample times to use for this channel Default: 0x0
10	SAR_INJ_AVG_EN	Averaging enable for this channel. If set the AVG_CNT and AVG_SHIFT settings are used for sampling the addressed pin(s) Default: 0x0
9	SAR_INJ_RESOLUTION	Resolution for this channel. Default: 0x0 **0x0: 12B** 12-bit resolution is used for this channel. **0x1: SUBRES** The resolution specified by SUB_RESOLUTION in the SAR_SAMPLE_CTRL register is used for this channel.
8	SAR_INJ_DIFFERENTIAL_EN	Differential enable for this channel. - 0: The voltage on the addressed pin is measured (Single-ended) and the resulting value is stored in the corresponding data register. - 1: The differential voltage on the addressed pin pair is measured and the resulting value is stored in the corresponding data register. (INJ_PIN_ADDR[0] is ignored). Default: 0x0
6 : 4	SAR_INJ_PORT_ADDR	Address of the port that contains the pin to be sampled by this channel. Default: 0x0 **0x0: SARMUX** SARMUX pins. **0x1: CTB0** CTB0 **0x2: CTB1** CTB1 **0x3: CTB2** CTB2 **0x4: CTB3** CTB3 **0x6: AROUTE_VIRT** AROUTE virtual port **0x7: SARMUX_VIRT** SARMUX virtual port
2 : 0	SAR_INJ_PIN_ADDR	Address of the pin to be sampled by this injection channel. If differential is enabled then PIN_ADDR[0] is ignored and considered to be 0, i.e. PIN_ADDR points to the even pin of a pin pair. Default: 0x0

9.1.31 SAR_INJ_RESULT

Address: 0x401A0290

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	0x0	None			
HW Access	W	W	W	W	None			
SW Access	R	R	R	R	None			
Bit Name	SAR_INJ_EOC_INTR_MIR	SAR_INJ_RANGE_INTR_MIR	SAR_INJ_SATURATE_INTR_MIR	SAR_INJ_COLLISION_INTR_MIR	Reserved[27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SAR_INJ_RESULT [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SAR_INJ_RESULT [15: 0]							

Injection channel result register

Bits	Name	Description
31	SAR_INJ_EOC_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default: 0x0
30	SAR_INJ_RANGE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default: 0x0
29	SAR_INJ_SATURATE_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default: 0x0
28	SAR_INJ_COLLISION_INTR_MIR	mirror bit of corresponding bit in SAR_INTR register Default: 0x0
15 : 0	SAR_INJ_RESULT	SAR conversion result of the channel. Default: 0x0000

9.1.32 SAR_MUX_SWITCH0

Address: 0x401A0300

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None		0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
SW Access	None		RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	Reserved[31:30]		SAR_MUX_FW_P7_COREIO3	SAR_MUX_FW_P6_COREIO2	SAR_MUX_FW_P5_COREIO1	SAR_MUX_FW_P4_COREIO0	SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

SARMUX Firmware switch controls

Bits	Name	Description
29	SAR_MUX_FW_P7_COREIO3	Firmware control: 0=open, 1=close switch between P7 and coreio3 signal. Write with 1 to set bit. Default: 0x0

9.1.32 SAR_MUX_SWITCH0 (continued)

28	SAR_MUX_FW_P6_COREIO2	Firmware control: 0=open, 1=close switch between P6 and coreio2 signal. Write with 1 to set bit. Default: 0x0
27	SAR_MUX_FW_P5_COREIO1	Firmware control: 0=open, 1=close switch between P5 and coreio1 signal. Write with 1 to set bit. Default: 0x0
26	SAR_MUX_FW_P4_COREIO0	Firmware control: 0=open, 1=close switch between P4 and coreio0 signal. Write with 1 to set bit. Default: 0x0
25	SAR_MUX_FW_SARBUS1_VMINUS	Firmware control: 0=open, 1=close switch between sarbus1 and vminus signal. Write with 1 to set bit. Default: 0x0
24	SAR_MUX_FW_SARBUS0_VMINUS	Firmware control: 0=open, 1=close switch between sarbus0 and vminus signal. Write with 1 to set bit. Default: 0x0
23	SAR_MUX_FW_SARBUS1_VPLUS	Firmware control: 0=open, 1=close switch between sarbus1 and vplus signal. Write with 1 to set bit. Default: 0x0
22	SAR_MUX_FW_SARBUS0_VPLUS	Firmware control: 0=open, 1=close switch between sarbus0 and vplus signal. Write with 1 to set bit. Default: 0x0
21	SAR_MUX_FW_AMUXBUSB_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusb and vminus signal. Write with 1 to set bit. Default: 0x0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	Firmware control: 0=open, 1=close switch between amuxbusa and vminus signal. Write with 1 to set bit. Default: 0x0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusb and vplus signal. Write with 1 to set bit. Default: 0x0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	Firmware control: 0=open, 1=close switch between amuxbusa and vplus signal. Write with 1 to set bit. Default: 0x0
17	SAR_MUX_FW_TEMP_VPLUS	Firmware control: 0=open, 1=close switch between temperature sensor and vplus signal, also powers on the temperature sensor. Write with 1 to set bit. Default: 0x0
16	SAR_MUX_FW_VSSA_VMINUS	Firmware control: 0=open, 1=close switch between vssa_kelvin and vminus signal. Write with 1 to set bit. Default: 0x0
15	SAR_MUX_FW_P7_VMINUS	Firmware control: 0=open, 1=close switch between pin P7 and vminus signal. Write with 1 to set bit. Default: 0x0
14	SAR_MUX_FW_P6_VMINUS	Firmware control: 0=open, 1=close switch between pin P6 and vminus signal. Write with 1 to set bit. Default: 0x0
13	SAR_MUX_FW_P5_VMINUS	Firmware control: 0=open, 1=close switch between pin P5 and vminus signal. Write with 1 to set bit. Default: 0x0
12	SAR_MUX_FW_P4_VMINUS	Firmware control: 0=open, 1=close switch between pin P4 and vminus signal. Write with 1 to set bit. Default: 0x0

9.1.32 SAR_MUX_SWITCH0 (continued)

11	SAR_MUX_FW_P3_VMINUS	Firmware control: 0=open, 1=close switch between pin P3 and vminus signal. Write with 1 to set bit. Default: 0x0
10	SAR_MUX_FW_P2_VMINUS	Firmware control: 0=open, 1=close switch between pin P2 and vminus signal. Write with 1 to set bit. Default: 0x0
9	SAR_MUX_FW_P1_VMINUS	Firmware control: 0=open, 1=close switch between pin P1 and vminus signal. Write with 1 to set bit. Default: 0x0
8	SAR_MUX_FW_P0_VMINUS	Firmware control: 0=open, 1=close switch between pin P0 and vminus signal. Write with 1 to set bit. Default: 0x0
7	SAR_MUX_FW_P7_VPLUS	Firmware control: 0=open, 1=close switch between pin P7 and vplus signal. Write with 1 to set bit. Default: 0x0
6	SAR_MUX_FW_P6_VPLUS	Firmware control: 0=open, 1=close switch between pin P6 and vplus signal. Write with 1 to set bit. Default: 0x0
5	SAR_MUX_FW_P5_VPLUS	Firmware control: 0=open, 1=close switch between pin P5 and vplus signal. Write with 1 to set bit. Default: 0x0
4	SAR_MUX_FW_P4_VPLUS	Firmware control: 0=open, 1=close switch between pin P4 and vplus signal. Write with 1 to set bit. Default: 0x0
3	SAR_MUX_FW_P3_VPLUS	Firmware control: 0=open, 1=close switch between pin P3 and vplus signal. Write with 1 to set bit. Default: 0x0
2	SAR_MUX_FW_P2_VPLUS	Firmware control: 0=open, 1=close switch between pin P2 and vplus signal. Write with 1 to set bit. Default: 0x0
1	SAR_MUX_FW_P1_VPLUS	Firmware control: 0=open, 1=close switch between pin P1 and vplus signal. Write with 1 to set bit. Default: 0x0
0	SAR_MUX_FW_P0_VPLUS	Firmware control: 0=open, 1=close switch between pin P0 and vplus signal. Write with 1 to set bit. Default: 0x0

9.1.33 SAR_MUX_SWITCH_CLEAR0

Address: 0x401A0304

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None		0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None		None	None	None	None	None	None
SW Access	None		RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	Reserved[31:30]		SAR_MUX_FW_P7_COREIO3	SAR_MUX_FW_P6_COREIO2	SAR_MUX_FW_P5_COREIO1	SAR_MUX_FW_P4_COREIO0	SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

SARMUX Firmware switch control clear

Bits	Name	Description
29	SAR_MUX_FW_P7_COREIO3	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.33 SAR_MUX_SWITCH_CLEAR0 (continued)

28	SAR_MUX_FW_P6_COREIO2	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
27	SAR_MUX_FW_P5_COREIO1	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
26	SAR_MUX_FW_P4_COREIO0	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
25	SAR_MUX_FW_SARBUS1_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
24	SAR_MUX_FW_SARBUS0_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
23	SAR_MUX_FW_SARBUS1_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
22	SAR_MUX_FW_SARBUS0_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
21	SAR_MUX_FW_AMUXBUSB_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
17	SAR_MUX_FW_TEMP_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
16	SAR_MUX_FW_VSSA_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
15	SAR_MUX_FW_P7_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
14	SAR_MUX_FW_P6_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
13	SAR_MUX_FW_P5_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
12	SAR_MUX_FW_P4_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
11	SAR_MUX_FW_P3_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
10	SAR_MUX_FW_P2_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
9	SAR_MUX_FW_P1_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
8	SAR_MUX_FW_P0_VMINUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
7	SAR_MUX_FW_P7_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.33 SAR_MUX_SWITCH_CLEAR0 (continued)

6	SAR_MUX_FW_P6_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
5	SAR_MUX_FW_P5_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
4	SAR_MUX_FW_P4_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
3	SAR_MUX_FW_P3_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
2	SAR_MUX_FW_P2_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
1	SAR_MUX_FW_P1_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0
0	SAR_MUX_FW_P0_VPLUS	Write 1 to clear corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.34 SAR_MUX_SWITCH1

Address: 0x401A0308

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW1C	RW1C	RW1C	RW1C
SW Access	None				RW1S	RW1S	RW1S	RW1S
Bit Name	Reserved[7:4]				SAR_MUX_FW_ADFT1_SARBUS1	SAR_MUX_FW_ADFT0_SARBUS0	SAR_MUX_FW_P5_DFT_INM	SAR_MUX_FW_P4_DFT_INP

SARMUX Firmware switch controls

Bits	Name	Description
3	SAR_MUX_FW_ADFT1_SARBUS1	Firmware control: 0=open, 1=close switch between adft1 signal and sarbus1 signal. Write with 1 to set bit. Default: 0x0
2	SAR_MUX_FW_ADFT0_SARBUS0	Firmware control: 0=open, 1=close switch between adft0 signal and sarbus0 signal. Write with 1 to set bit. Default: 0x0
1	SAR_MUX_FW_P5_DFT_INM	Firmware control: 0=open, 1=close switch between P5 pin and dft_inm signal. Write with 1 to set bit. Default: 0x0

9.1.34 SAR_MUX_SWITCH1 (continued)

0	SAR_MUX_FW_P4_DFT_INP	Firmware control: 0=open, 1=close switch between P4 pin and dft_inp signal. Write with 1 to set bit. Default: 0x0

9.1.35 SAR_MUX_SWITCH_CLEAR1

Address: 0x401A030C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				None	None	None	None
SW Access	None				RW1C	RW1C	RW1C	RW1C
Bit Name	Reserved[7:4]				SAR_MUX_FW_ADFT1_SARBUS1	SAR_MUX_FW_ADFT0_SARBUS0	SAR_MUX_FW_P5_DFT_INM	SAR_MUX_FW_P4_DFT_INP

SARMUX Firmware switch control clear

Bits	Name	Description
3	SAR_MUX_FW_ADFT1_SARBUS1	Write 1 to clear corresponding bit in MUX_SWITCH1 Default: 0x0
2	SAR_MUX_FW_ADFT0_SARBUS0	Write 1 to clear corresponding bit in MUX_SWITCH1 Default: 0x0
1	SAR_MUX_FW_P5_DFT_INM	Write 1 to clear corresponding bit in MUX_SWITCH1 Default: 0x0
0	SAR_MUX_FW_P4_DFT_INP	Write 1 to clear corresponding bit in MUX_SWITCH1 Default: 0x0

9.1.36 SAR_MUX_SWITCH_HW_CTRL

Address: 0x401A0340

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	None		0x0	0x0	0x0	0x0
HW Access	R	R	None		R	R	R	R
SW Access	RW	RW	None		RW	RW	RW	RW
Bit Name	SAR_MUX_HW_CTRL_SARBUS1	SAR_MUX_HW_CTRL_SARBUS0	Reserved[21:20]		SAR_MUX_HW_CTRL_AMUX-BUSB	SAR_MUX_HW_CTRL_AMUX-BUSA	SAR_MUX_HW_CTRL_TEMP	SAR_MUX_HW_CTRL_VSSA

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	SAR_MUX_HW_CTRL_P7	SAR_MUX_HW_CTRL_P6	SAR_MUX_HW_CTRL_P5	SAR_MUX_HW_CTRL_P4	SAR_MUX_HW_CTRL_P3	SAR_MUX_HW_CTRL_P2	SAR_MUX_HW_CTRL_P1	SAR_MUX_HW_CTRL_P0

SARMUX switch hardware control

Bits	Name	Description
23	SAR_MUX_HW_CTRL_SARBUS1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus1 switches. Default: 0x0
22	SAR_MUX_HW_CTRL_SARBUS0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for sarbus0 switches. Default: 0x0

9.1.36 SAR_MUX_SWITCH_HW_CTRL (continued)

19	SAR_MUX_HW_CTRL_AMUXBUSB	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusb switches. Default: 0x0
18	SAR_MUX_HW_CTRL_AMUXBUSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for amuxbusa switches. Default: 0x0
17	SAR_MUX_HW_CTRL_TEMP	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for temp switch. Default: 0x0
16	SAR_MUX_HW_CTRL_VSSA	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for vssa switch. Default: 0x0
7	SAR_MUX_HW_CTRL_P7	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P7 switches. Default: 0x0
6	SAR_MUX_HW_CTRL_P6	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P6 switches. Default: 0x0
5	SAR_MUX_HW_CTRL_P5	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P5 switches. Default: 0x0
4	SAR_MUX_HW_CTRL_P4	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P4 switches. Default: 0x0
3	SAR_MUX_HW_CTRL_P3	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P3 switches. Default: 0x0
2	SAR_MUX_HW_CTRL_P2	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P2 switches. Default: 0x0
1	SAR_MUX_HW_CTRL_P1	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P1 switches. Default: 0x0
0	SAR_MUX_HW_CTRL_P0	Hardware control: 0=only firmware control, 1=hardware control masked by firmware setting for pin P0 switches. Default: 0x0

9.1.37 SAR_MUX_SWITCH_STATUS

Address: 0x401A0348

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None						0x0	0x0
HW Access	None						W	W
SW Access	None						R	R
Bit Name	Reserved[31:26]						SAR_MUX_FW_SARBUS1_VMINUS	SAR_MUX_FW_SARBUS0_VMINUS

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SAR_MUX_FW_SARBUS1_VPLUS	SAR_MUX_FW_SARBUS0_VPLUS	SAR_MUX_FW_AMUXBUSB_VMINUS	SAR_MUX_FW_AMUXBUSA_VMINUS	SAR_MUX_FW_AMUXBUSB_VPLUS	SAR_MUX_FW_AMUXBUSA_VPLUS	SAR_MUX_FW_TEMP_VPLUS	SAR_MUX_FW_VSSA_VMINUS

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SAR_MUX_FW_P7_VMINUS	SAR_MUX_FW_P6_VMINUS	SAR_MUX_FW_P5_VMINUS	SAR_MUX_FW_P4_VMINUS	SAR_MUX_FW_P3_VMINUS	SAR_MUX_FW_P2_VMINUS	SAR_MUX_FW_P1_VMINUS	SAR_MUX_FW_P0_VMINUS

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SAR_MUX_FW_P7_VPLUS	SAR_MUX_FW_P6_VPLUS	SAR_MUX_FW_P5_VPLUS	SAR_MUX_FW_P4_VPLUS	SAR_MUX_FW_P3_VPLUS	SAR_MUX_FW_P2_VPLUS	SAR_MUX_FW_P1_VPLUS	SAR_MUX_FW_P0_VPLUS

SARMUX switch status

Bits	Name	Description
25	SAR_MUX_FW_SARBUS1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.37 SAR_MUX_SWITCH_STATUS (continued)

24	SAR_MUX_FW_SARBUS0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
23	SAR_MUX_FW_SARBUS1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
22	SAR_MUX_FW_SARBUS0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
21	SAR_MUX_FW_AMUXBUSB_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
20	SAR_MUX_FW_AMUXBUSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
19	SAR_MUX_FW_AMUXBUSB_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
18	SAR_MUX_FW_AMUXBUSA_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
17	SAR_MUX_FW_TEMP_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
16	SAR_MUX_FW_VSSA_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
15	SAR_MUX_FW_P7_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
14	SAR_MUX_FW_P6_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
13	SAR_MUX_FW_P5_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
12	SAR_MUX_FW_P4_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
11	SAR_MUX_FW_P3_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
10	SAR_MUX_FW_P2_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
9	SAR_MUX_FW_P1_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
8	SAR_MUX_FW_P0_VMINUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
7	SAR_MUX_FW_P7_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
6	SAR_MUX_FW_P6_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
5	SAR_MUX_FW_P5_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
4	SAR_MUX_FW_P4_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
3	SAR_MUX_FW_P3_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.37 SAR_MUX_SWITCH_STATUS (continued)

2	SAR_MUX_FW_P2_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
1	SAR_MUX_FW_P1_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0
0	SAR_MUX_FW_P0_VPLUS	switch status of corresponding bit in MUX_SWITCH0 Default: 0x0

9.1.38 SAR_PUMP_CTRL

Address: 0x401A0380

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SAR_ENABLED	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[7:1]							SAR_CLOCK_SEL

Switch pump control

Bits	Name	Description
31	SAR_ENABLED	0=disabled: pump output is VDDA_PUMP, 1=enabled: pump output is boosted. Default: 0x0
0	SAR_CLOCK_SEL	Clock select: 0=external clock, 1=internal clock (deprecated). Default: 0x0

9.1.39 SAR_ANA_TRIM

Address: 0x401A0F00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0		
HW Access	None				R	R		
SW Access	None				RW	RW		
Bit Name	Reserved[7:4]				SAR_TRIM UNIT	SAR_CAP_TRIM [2:0]		

Analog trim register.

Bits	Name	Description
3	SAR_TRIMUNIT	Attenuation cap trimming Default: 0x0
2 : 0	SAR_CAP_TRIM	Attenuation cap trimming Default: 0x0

9.1.40 SAR_WOUNDING

Address: 0x401A0F04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	
HW Access	None						R	
SW Access	None						RW1S	
Bit Name	Reserved[7:2]						SAR_WOUND_RESOLUTION [1:0]	

SAR wounding register

Bits	Name	Description
1 : 0	SAR_WOUND_RESOLUTION	Maximum SAR resolution allowed Default: 0x0 **0x0: 12BIT** unwounded: up to full 12-bit SAR resolution allowed **0x1: 10BIT** wounded: max resolution upto 10-bit SAR resolution allowed **0x2: 8BIT** wounded: only 8-bit SAR resolution allowed

9.1.40 SAR_WOUNDING (continued)

0x3: 8BIT_TOO
wounded: only 8-bit SAR resolution allowed

10 SCB Registers

This section discusses the SCB registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

10.1 SCB Register Mapping Overview

Register Name	Address
SCB_CTRL	0x40060000
SCB_STATUS	0x40060004
SCB_SPI_CTRL	0x40060020
SCB_SPI_STATUS	0x40060024
SCB_UART_CTRL	0x40060040
SCB_UART_TX_CTRL	0x40060044
SCB_UART_RX_CTRL	0x40060048
SCB_UART_RX_STATUS	0x4006004C
SCB_I2C_CTRL	0x40060060
SCB_I2C_STATUS	0x40060064
SCB_I2C_M_CMD	0x40060068
SCB_I2C_S_CMD	0x4006006C
SCB_I2C_CFG	0x40060070
SCB_BIST_CONTROL	0x40060100
SCB_BIST_DATA	0x40060104
SCB_TX_CTRL	0x40060200
SCB_TX_FIFO_CTRL	0x40060204
SCB_TX_FIFO_STATUS	0x40060208
SCB_TX_FIFO_WR	0x40060240
SCB_RX_CTRL	0x40060300
SCB_RX_FIFO_CTRL	0x40060304
SCB_RX_FIFO_STATUS	0x40060308
SCB_RX_MATCH	0x40060310
SCB_RX_FIFO_RD	0x40060340
SCB_RX_FIFO_RD_SILENT	0x40060344
SCB_EZ_DATA	0x40060400

Register Name	Address
SCB_INTR_CAUSE	0x40060E00
SCB_INTR_I2C_EC	0x40060E80
SCB_INTR_I2C_EC_MASK	0x40060E88
SCB_INTR_I2C_EC_MASKED	0x40060E8C
SCB_INTR_SPI_EC	0x40060EC0
SCB_INTR_SPI_EC_MASK	0x40060EC8
SCB_INTR_SPI_EC_MASKED	0x40060ECC
SCB_INTR_M	0x40060F00
SCB_INTR_M_SET	0x40060F04
SCB_INTR_M_MASK	0x40060F08
SCB_INTR_M_MASKED	0x40060F0C
SCB_INTR_S	0x40060F40
SCB_INTR_S_SET	0x40060F44
SCB_INTR_S_MASK	0x40060F48
SCB_INTR_S_MASKED	0x40060F4C
SCB_INTR_TX	0x40060F80
SCB_INTR_TX_SET	0x40060F84
SCB_INTR_TX_MASK	0x40060F88
SCB_INTR_TX_MASKED	0x40060F8C
SCB_INTR_RX	0x40060FC0
SCB_INTR_RX_SET	0x40060FC4
SCB_INTR_RX_MASK	0x40060FC8
SCB_INTR_RX_MASKED	0x40060FCC

10.1.1 SCB_CTRL

Address: 0x40060000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None					0x3	
HW Access	R	None					R	
SW Access	RW	None					RW	
Bit Name	SCB_ENABLED	Reserved[30:26]					SCB_MODE [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[23:18]						SCB_BLOCK	SCB_ADDR_ACCEPT

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[15:11]					SCB_EZ_MODE	SCB_EC_OP_MODE	SCB_EC_AM_MODE

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0xF			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				SCB_OVS [3:0]			

Generic control register.

Bits	Name	Description

10.1.1 SCB_CTRL (continued)

31	SCB_ENABLED	IP enabled (1) or not (0). The proper order in which to initialize the IP is as follows: - Program protocol specific information using SPI_CTRL, UART_CTRL (and UART_TX_CTRL and UART_RX_CTRL) or I2C_CTRL. This includes selection of a submode, master/slave functionality and transmitter/receiver functionality when applicable. - Program generic transmitter (TX_CTRL) and receiver (RX_CTRL) information. This includes enabling of the transmitter and receiver functionality. - Program transmitter FIFO (TX_FIFO_CTRL) and receiver FIFO (RX_FIFO_CTRL) information. - Program CTRL to enable IP, select the specific operation mode and oversampling factor. When the IP is enabled, no control information should be changed. Changes should be made AFTER disabling the IP, e.g. to modify the operation mode (from I2C to SPI) or to go from externally to internally clocked. The change takes effect after the IP is re-enabled. Note that disabling the IP will cause re-initialization of the design and associated state is lost (e.g. FIFO content). Default: 0x0
25 : 24	SCB_MODE	Mode of operation (3: Reserved) Default: 0x3 **0x0: I2C** Inter-Integrated Circuits (I2C) mode. **0x1: SPI** Serial Peripheral Interface (SPI) mode. **0x2: UART** Universal Asynchronous Receiver/Transmitter (UART) mode.
17	SCB_BLOCK	Only used in externally clocked mode. If the externally clocked logic and the MMIO SW accesses to EZ memory coincide/collide, this bit determines whether a SW access should block and result in bus wait states (BLOCK is 1) or not (BLOCK is 0). IF BLOCK is â0â and the accesses collide, MMIO read operations return 0xffff:ffff and MMIO write operations are ignored. Colliding accesses are registered as interrupt causes: field BLOCKED of MMIO registers INTR_TX and INTR_RX. Default: 0x0
16	SCB_ADDR_ACCEPT	Determines whether a received matching address is accepted in the RX FIFO (1) or not (0). This field is used in the I2C mode, to allow the slave to put the received slave address or general call address in the RX FIFO. Note that a received matching address is put in the RX FIFO when ADDR_ACCEPT is 1 for both I2C read and write transfers. This field is used in the multi-processor UART receiver mode, to allow the receiver to put the received address in the RX FIFO. Note: non-matching addresses are never put in the RX FIFO. Default: 0x0
10	SCB_EZ_MODE	Non EZ mode (0) or EZ mode (1). In EZ mode, a meta protocol is applied to the serial interface protocol. This meta protocol adds meaning to the data frames transferred by the serial interface protocol: a data frame can represent a memory address, a write memory data element or a read memory data element. EZ mode is only used for synchronous serial interface protocols: SPI and I2C. In SPI mode, only Motorola mode 0 is supported and the trasmitter should use continuous data frames; i.e. data frames. This mode is only applicable to slave functionality. In EZ mode, the slave can read from and write to an addressable memory structure of 32 bytes. In EZ mode, data frames should 8-bit in size and should be transmitted and received with the Most Significant Bit (MSB) first. In UART mode this field should be 0. Default: 0x0

10.1.1 SCB_CTRL (continued)

9	SCB_EC_OP_MODE	Internally clocked mode (0) or externally clocked mode (1) operation. In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked operation mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode AND EZ mode. In SPI mode, only Motorola mode 0 is supported. The maximum SPI slave, EZ mode bitrate is 48 Mbps (transmission and IO delays outside the IP will degrade the effective bitrate). In UART mode this field should be 0. Default: 0x0
8	SCB_EC_AM_MODE	Internally clocked mode (0) or externally clocked mode (1) address matching (I2C) or selection (SPI). In internally clocked mode, the serial interface protocols run off the peripheral clock. In externally clocked mode, the serial interface protocols run off the clock as provided by the serial interface. Externally clocked mode is only used for synchronous serial interface protocols (SPI and I2C) in slave mode. In SPI mode, only Motorola mode 0 is supported. In UART mode this field should be 0. Default: 0x0

10.1.1 SCB_CTRL (continued)

3 : 0	SCB_OVS	Serial interface bit period oversampling factor expressed in IP clock cycles. Used for SPI and UART functionality. OVS + 1 IP clock cycles constitute a single serial interface clock/bit cycle. The IP clock is provided by the programmable clock IP. This field is NOT used in externally clocked mode. If OVS is odd, the oversampling factor is even and the first and second phase of the interface clock period are the same. If OVS is even, the oversampling factor is odd and the first phase of the interface clock period is 1 peripheral clock cycle longer than the second phase of the interface clock period. In SPI master mode, the valid range is [3, 15] (at a system frequency of 48 MHz, the maximum bit rate is 12 Mbps). In SPI slave mode, the OVS field is NOT used. However, there is a frequency requirement for the IP clock wrt. the interface (IF) clock to guarantee functional correct behavior. This requirement is expressed as a ratio: IP clock/IF clock. The ratio is dependent on the setting of RX_CTRL.MEDIAN and SPI_CTRL.LATE_MISO_SAMPLE: - MEDIAN is 0 and LATE_MISO_SAMPLE is 0: IP clock/IF clock gt;= 6. At a IP frequency of 48 MHz, the maximum bit rate is 8 Mbps. - MEDIAN is 0 and LATE_MISO_SAMPLE is 1: IP clock/IF clock gt;= 3. At a IP frequency of 48 MHz, the maximum bit rate is 16 Mbps. - MEDIAN is 1 and LATE_MISO_SAMPLE is 0: IP clock/IF clock gt;= 8. At a IP frequency of 48 MHz, the maximum bit rate is 6 Mbps. - MEDIAN is 1 and LATE_MISO_SAMPLE is 1: IP clock/IF clock gt;= 4. At a IP frequency of 48 MHz, the maximum bit rate is 12 Mbps. The above requirements provide an IP centric perspective, assuming ideal (0 ns) IO cell and routing delay. The required IP clock/IF clock ratio increases and the calculated maximum bit rate decreases, when realistic chip delays are taken into account. In UART standard submode (including LIN), the valid range is [7, 15]. In UART SmartCard submode, the valid range is [7, 15]. In UART TX IrDA submode this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. Only normal transmission mode is supported, the pulse is roughly 3/16 of the bit period (for all bit rates). There is only one valid OVS value: - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. In UART RX IrDA submode (1.2, 2.4, 9.6, 19.2, 38.4, 57.6 and 115.2 Kbps) this field indirectly specifies the oversampling. The oversampling determines the interface clock/bit cycle and the width of the pulse. In normal transmission mode, this pulse is roughly 3/16 of the bit period (for all bit rates). In low power transmission mode, this pulse is potentially smaller (down to 1.62 us typical and 1.41 us minimal) than 3/16 of the bit period (for lt; 115.2 Kbps bitrates). Pulse widths greater or equal than two IP clock cycles are guaranteed to be detected by the receiver. Pulse widths less than two IP clock cycles and greater or equal than one IP clock cycle may be detected by the receiver. Pulse widths less than one IP clock cycle will not be detected by the receiver. RX_CTRL.MEDIAN should be set to 1 for IrDA receiver functionality. The IP clock (as provided by the programmable clock IP) and the oversampling together determine the IrDA bitrate. Normal mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. IP clock frequency of 16*57.6 KHz for 57.6 Kbps. IP clock frequency of 16*38.4 KHz for 38.4 Kbps. IP clock frequency of 16*19.2 KHz for 19.2 Kbps. IP clock frequency of 16*9.6 KHz for 9.6 Kbps. IP clock frequency of 16*2.4 KHz for 2.4 Kbps. IP clock frequency of 16*1.2 KHz for 1.2 Kbps. - all other values are not used in normal mode. Low power mode, OVS field values (with the required IP clock frequency): - 0: 16 times oversampling. IP clock frequency of 16*115.2 KHz for 115.2 Kbps. - 1: 32 times oversampling. IP clock frequency of 32*57.6 KHz for 57.6 Kbps. - 2: 48 times oversampling. IP clock frequency of 48*38.4 KHz for 38.4 Kbps. - 3: 96 times oversampling. IP clock frequency of 96*19.2 KHz for 19.2 Kbps. - 4: 192 times oversampling. IP clock frequency of 192*9.6 KHz for 9.6 Kbps. - 5: 768 times oversampling. IP clock frequency of 768*2.4 KHz for 2.4 Kbps. - 6: 1536 times oversampling. IP clock frequency of 1536*1.2 KHz for 1.2 Kbps. - all other values are not used in low power mode. Default: 0xF

10.1.2 SCB_STATUS

Address: 0x40060004

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							W
SW Access	None							R
Bit Name	Reserved[7:1]							SCB_EC_BUSY

Generic status register.

Bits	Name	Description
0	SCB_EC_BUSY	Inidicates whether the externaly clocked logic is potentially accessing the EZ memory (this is only possible in EZ mode). This bit can be used by SW to determine whether it is safe to issue a SW access to the EZ memory (without bus wait states (a blocked SW access) or bus errors being generated). Note that the INTR_TX.BLOCKED and INTR_RX.BLOCKED interrupt causes are used to indicate whether a SW access was actually blocked by externally clocked logic. Default: 0x0

10.1.3 SCB_SPI_CTRL

Address: 0x40060020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None			0x0		0x3	
HW Access	R	None			R		R	
SW Access	RW	None			RW		RW	
Bit Name	SCB_MASTER_MODE	Reserved[30:28]			SCB_SLAVE_SELECT [27:26]		SCB_MODE [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[23:17]							SCB_LOOPBACK

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	0x0	0x0	0x0	0x0
HW Access	None			R	R	R	R	R
SW Access	None			RW	RW	RW	RW	RW
Bit Name	Reserved[7:5]			SCB_LATE_MISO_SAMPLE	SCB_CPOL	SCB_CPHA	SCB_SELECT_PRECEDE	SCB_CONTINUOUS

SPI control register.

Bits	Name	Description
31	SCB_MASTER_MODE	Master (1) or slave (0) mode. In master mode, transmission will commence on availability of data frames in the TX FIFO. In slave mode, when selected and there is no data frame in the TX FIFO, the slave will transmit all 1s. In both master and slave modes, received data frames will be lost if the RX FIFO is full. Default: 0x0

10.1.3 SCB_SPI_CTRL (continued)

27 : 26	SCB_SLAVE_SELECT	Selects one of the four SPI slave select signals: - 0: Slave 0, SPI_SELECT[0]. - 1: Slave 1, SPI_SELECT[1]. - 2: Slave 2, SPI_SELECT[2]. - 3: Slave 3, SPI_SELECT[3]. Only used in master mode. The IP should be disabled when changes are made to this field. Default: 0x0
25 : 24	SCB_MODE	Submode of SPI operation (3: Reserved). Default: 0x3 **0x0: SPI_MOTOROLA** SPI Motorola submode. In master mode, when not transmitting data (SELECT is inactive), SCLK is stable at CPOL. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive. **0x1: SPI_TI** SPI Texas Instruments submode. In master mode, when not transmitting data, SCLK is stable at 0. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive; i.e. no pulse is generated. **0x2: SPI_NS** SPI National Semiconducturs submode. In master mode, when not transmitting data, SCLK is stable at 0. In slave mode, when not selected, SCLK is ignored; i.e. it can be either stable or clocking. In master mode, when there is no data to transmit (TX FIFO is empty), SELECT is inactive.
16	SCB_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master mode. Not applicable in National Semiconductors submode. When 0, the SPI master MISO line is connected to the SPI MISO pin. When 1, the SPI master MISO line is connected to the SPI master MOSI line. In other words, in loopback mode the SPI master receives on MISO what it transmits on MOSI. Default: 0x0
4	SCB_LATE_MISO_SAMPLE	Only applicable in master mode. Changes the SCLK edge on which MISO is captured. When 0, the default applies (for Motorola as determined by CPOL and CPHA, for Texas Instruments on the falling edge of SCLK and for National Semiconductors on the rising edge of SCLK). When 1, the alternate clock edge is used (which comes half a SPI SCLK period later). Late sampling addresses the round trip delay associated with transmitting SCLK from the master to the slave and transmitting MISO from the slave to the master. Default: 0x0
3	SCB_CPOL	Only applicable in SPI Motorola submode. Indicates the clock polarity. This field, together with the CPHA field, indicates when MOSI data is driven and MISO data is captured: - CPOL is â0â: SCLK is â0â when not transmitting data. - CPOL is â1â: SCLK is â1â when not transmitting data. Default: 0x0

10.1.3 SCB_SPI_CTRL (continued)

2	SCB_CPHA	Only applicable in SPI Motorola submode. Indicates the clock phase. This field, together with the CPOL field, indicates when MOSI data is driven and MISO data is captured. - CPOL is â0â, CPHA is â0â: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. - CPOL is â0â, CPHA is â1â: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is â1â, CPHA is â0â: MOSI is driven on a rising edge of SCLK. MISO is captured on a falling edge of SCLK. - CPOL is â1â, CPHA is â1â: MOSI is driven on a falling edge of SCLK. MISO is captured on a rising edge of SCLK. Default: 0x0
1	SCB_SELECT_PRECEDE	Only used in SPI Texas Instruments submode. When 1, the data frame start indication is a pulse on the SELECT line that precedes the transfer of the first data frame bit. When 0, the data frame start indication is a pulse on the SELECT line that coincides with the transfer of the first data frame bit. Default: 0x0
0	SCB_CONTINUOUS	Continuous SPI data transfers enabled (1) or not (0). When continuous transfers are enabled individual data frame transfers are not necessarily seperated by slave deselection (as indicated by the SELECT line): if the TX FIFO has multiple data frames, data frames are send out without slave deselection. When continuous transfers are not enabled individual data frame transfers are always seperated by slave deselection: independent of the availability of TX FIFO data frames, data frames are send out with slave deselection. This field is used in master mode. In slave mode, both continuous and non-continuous SPI data transfers are supported. Default: 0x0

10.1.4 SCB_SPI_STATUS

Address: 0x40060024

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00							
HW Access	W							
SW Access	R							
Bit Name	SCB_EZ_ADDR [15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							W
SW Access	None							R
Bit Name	Reserved[7:1]							SCB_BUS_BUSY

SPI status register.

Bits	Name	Description
15 : 8	SCB_EZ_ADDR	SPI slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default: 0x00
0	SCB_BUS_BUSY	SPI bus is busy. The bus is considered busy (1) during an ongoing transaction. For Motorola and National submodes, the busy bit is 1, when the slave selection (low active) is activated. For TI submode, the busy bit is 1 from the time the preceding/coinciding slave select (high active) is activated for the first transmitted data frame, till the last MOSI/MISO bit of the last data frame is transmitted. Default: 0x0

10.1.5 SCB_UART_CTRL

Address: 0x40060040

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None						0x3	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[31:26]						SCB_MODE [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[23:17]							SCB_LOOP BACK

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

UART control register.

Bits	Name	Description
25 : 24	SCB_MODE	Submode of UART operation (3: Reserved) Default: 0x3 **0x0: UART_STD** Standard UART submode. **0x1: UART_SMARTCARD** SmartCard (ISO7816) submode. Support for negative acknowledgement (NACK) on the receiver side and retransmission on the transmitter side.

10.1.5 SCB_UART_CTRL (continued)

		0x2: UART_IRDA Infrared Data Association (IrDA) submode. Return to Zero modulation scheme. In this mode, the oversampling factor should be 16, that is OVS is 15.
16	SCB_LOOPBACK	Local loopback control (does NOT affect the information on the pins). When 0, the transmitter TX line is connected to the TX pin and the receiver RX line is connected to the RX pin. When 1, the transmitter TX line is connected to the receiver RX line. This allows a SCB UART transmitter to communicate with its receiver counterpart. Default: 0x0

10.1.6 SCB_UART_TX_CTRL

Address: 0x40060044

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[15:9]							SCB_RETRY_ON_NACK

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0	0x0	None	0x2		
HW Access	None		R	R	None	R		
SW Access	None		RW	RW	None	RW		
Bit Name	Reserved[7:6]		SCB_PARITY_ENABLED	SCB_PARITY	Reserved	SCB_STOP_BITS [2:0]		

UART transmitter control register.

Bits	Name	Description
8	SCB_RETRY_ON_NACK	When 1, a data frame is retransmitted when a negative acknowledgement is received. Only applicable to the SmartCard submode. Default: 0x0
5	SCB_PARITY_ENABLED	Parity generation enabled (1) or not (0). Only applicable in standard UART submodes. In SmartCard submode, parity generation is always enabled through hardware. In IrDA submode, parity generation is always disabled through hardware Default: 0x0

10.1.6 SCB_UART_TX_CTRL (continued)

4	SCB_PARITY	Parity bit. When 0, the transmitter generates an even parity. When 1, the transmitter generates an odd parity. Only applicable in standard UART and SmartCard submodes. Default: 0x0
2 : 0	SCB_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. Default: 0x2

10.1.7 SCB_UART_RX_CTRL

Address: 0x40060048

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0xA			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[23:20]				SCB_BREAK_WIDTH [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x0	0x0	None	0x0	0x0	0x0
HW Access	None		R	R	None	R	R	R
SW Access	None		RW	RW	None	RW	RW	RW
Bit Name	Reserved[15:14]		SCB_SKIP_START	SCB_LIN_MODE	Reserved	SCB_MP_MODE	SCB_DROP_ON_FRAME_ERROR	SCB_DROP_ON_PARITY_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0	0x0	None	0x2		
HW Access	None	R	R	R	None	R		
SW Access	None	RW	RW	RW	None	RW		
Bit Name	Reserved	SCB_POLARITY	SCB_PARITY_ENABLED	SCB_PARITY	Reserved	SCB_STOP_BITS [2:0]		

UART receiver control register.

Bits	Name	Description

10.1.7 SCB_UART_RX_CTRL (continued)

19 : 16	SCB_BREAK_WIDTH	Break width. BREAK_WIDTH + 1 is the minimum width in bit periods of a break. During a break the transmitted/received line value is 0. This feature is useful for standard UART submode and LIN submode (break field detection). Once, the break is detected, the INTR_RX.BREAK_DETECT bit is set to 1. Note that break detection precedes baud rate detection, which is used to synchronize/refine the receiver clock to the transmitter clock. As a result, break detection operates with an unsynchronized/unrefined receiver clock. Therefore, the receivers definition of a bit period is imprecise and the setting of this field should take this imprecision into account. The LIN standard also accounts for this imprecision: a LIN start bit followed by 8 data bits allows for up to 9 consecutive 0 bit periods during regular transmission, whereas the LIN break detection should be at least 13 consecutive 0 bit periods. This provides for a margin of 4 bit periods. Therefore, the default value of this field is set to 10, representing a minimal break field with of 10+1 = 11 bit periods; a value in between the 9 consecutive bit periods of a regular transmission and the 13 consecutive bit periods of a break field. This provides for slight imprecisions of the receiver clock wrt. the transmitter clock. There should not be a need to program this field to any value other than its default value. Default: 0xA
13	SCB_SKIP_START	Only applicable in standard UART submode. When 1, the receiver skips start bit detection for the first received data frame. Instead, it synchronizes on the first received data frame bit, which should be a 1. This functionality is intended for wake up from DeepSleep when receiving a data frame. The transition from idle (1) to START (0) on the RX line is used to wake up the CPU. The transition detection (and the associated wake up functionality) is performed by the GPIO2 IP. The woken up CPU will enable the SCBs UART receiver functionality. Once enabled, it is assumed that the START bit is ongoing (the CPU wakeup and SCB enable time should be less than the START bit period). The SCB will synchronize to a 0 to 1 transition, which indicates the first data frame bit is received (first data frame bit should be 1). After synchronization to the first data frame bit, the SCB will resume normal UART functionality: subsequent data frames will be synchronized on the receipt of a START bit. Default: 0x0
12	SCB_LIN_MODE	Only applicable in standard UART submode. When 1, the receiver performs break detection and baud rate detection on the incoming data. First, break detection counts the amount of bit periods that have a line value of 0. BREAK_WIDTH specifies the minum required amount of bit periods. Successful break detection sets the INTR_RX.BREAK_DETECT interrupt cause to 1. Second, baud rate detection counts the amount of peripheral clock periods that are use to receive the synchronization byte (0x55; least significant bit first). The count is available through UART_RX_STATUS.BR_COUNTER. Successful baud rate detection sets the INTR_RX.BAUD_DETECT interrupt cause to 1 (BR_COUNTER is reliable). This functionality is used to synchronize/refine the receiver clock to the transmitter clock. The receiver software can use the BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Default: 0x0
10	SCB_MP_MODE	Multi-processor mode. When 1, multi-processor mode is enabled. In this mode, RX_CTRL.DATA_WIDTH should indicate a 9-bit data frame. In multi-processor mode, the 9th received bit of a data frame seperates addresses (bit is 1) from data (bit is 0). A received address is matched with RX_MATCH.DATA and RX_MATCH.MASK. In the case of a match, subsequent received data are sent to the RX FIFO. In the case of NO match, subsequent received data are dropped. Default: 0x0
9	SCB_DROP_ON_FRAME_ERROR	Behaviour when an error is detected in a start or stop period. When 0, received data is send to the RX FIFO. When 1, received data is dropped and lost. Default: 0x0
8	SCB_DROP_ON_PARITY_ERROR	Behaviour when a parity check fails. When 0, received data is send to the RX FIFO. When 1, received data is dropped and lost. Only applicable in standard UART and SmartCard submodes (negatively acknowledged SmartCard data frames may be dropped with this field). Default: 0x0

10.1.7 SCB_UART_RX_CTRL (continued)

6	SCB_POLARITY	Inverts incoming RX line signal. Inversion is after local loopback. This functionality is intended for IrDA receiver functionality. Default: 0x0
5	SCB_PARITY_ENABLED	Parity checking enabled (1) or not (0). Only applicable in standard UART submode. In SmartCard submode, parity checking is always enabled through hardware. In IrDA submode, parity checking is always disabled through hardware. Default: 0x0
4	SCB_PARITY	Parity bit. When 0, the receiver expects an even parity. When 1, the receiver expects an odd parity. Only applicable in standard UART and SmartCard submodes. Default: 0x0
2 : 0	SCB_STOP_BITS	Stop bits. STOP_BITS + 1 is the duration of the stop period in terms of halve bit periods. Valid range is [1, 7]; i.e. a stop period should last at least one bit period. If STOP_BITS is 1, stop bits error detection is NOT performed. If STOP_BITS is in [2, 7], stop bits error detection is performed and the associated interrupt cause INTR_RX.FRAME_ERROR is set to 1 if an error is detected. In other words, the receiver supports data frames with a 1 bit period stop bit sequence, but requires at least 1.5 bit period stop bit sequences to detect errors. This limitation is due to possible transmitter and receiver clock skew that prevents the design from doing reliable stop bit detection for short (1 bit bit period) stop bit sequences. Note that in case of a stop bits error, the successive data frames may get lost as the receiver needs to resynchronize its start bit detection. The amount of lost data frames depends on both the amount of stop bits, the idle (1) time between data frames and the data frame value. Default: 0x2

10.1.8 SCB_UART_RX_STATUS

Address: 0x4006004C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x000			
HW Access	None				W			
SW Access	None				R			
Bit Name	Reserved[15:12]				SCB_BR_COUNTER [11:0]			

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	W							
SW Access	R							
Bit Name	SCB_BR_COUNTER [11 : 0]							

UART receiver status register.

Bits	Name	Description
11 : 0	SCB_BR_COUNTER	Amount of peripheral clock periods that constitute the transmission of a 0x55 data frame (sent least signficant bit first) as determined by the receiver. BR_COUNTER / 8 is the amount of peripheral clock periods that constitute a bit period. This field has valid data when INTR_RX.BAUD_DETECT is set to 1. Default: 0x000

10.1.9 SCB_I2C_CTRL

Address: 0x40060060

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	SCB_MASTER_MODE	SCB_SLAVE_MODE	Reserved[29:24]					

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[23:17]							SCB_LOOPBACK

Bits	15	14	13	12	11	10	9	8
Reset Value	0x1	0x1	0x1	0x1	0x1	None	0x1	0x1
HW Access	R	R	R	R	R	None	R	R
SW Access	RW	RW	RW	RW	RW	None	RW	RW
Bit Name	SCB_S_NOT_READY_DATA_NACK	SCB_S_NOT_READY_ADDR_NACK	SCB_S_READY_DATA_ACK	SCB_S_READY_ADDR_ACK	SCB_S_GENERAL_IGNORE	Reserved	SCB_M_NOT_READY_DATA_NACK	SCB_M_READY_DATA_ACK

Bits	7	6	5	4	3	2	1	0
Reset Value	0x8				0x8			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	SCB_LOW_PHASE_OVS [7:4]				SCB_HIGH_PHASE_OVS [3:0]			

I2C control register.

Bits	Name	Description
31	SCB_MASTER_MODE	Master mode enabled (1) or not (0). Note that both master and slave modes can be enabled at the same time. This allows the IP to address itself. Default: 0x0
30	SCB_SLAVE_MODE	Slave mode enabled (1) or not (0). Default: 0x0

10.1.9 SCB_I2C_CTRL (continued)

16	SCB_LOOPBACK	Local loopback control (does NOT affect the information on the pins). Only applicable in master/slave mode. When 0, the I2C SCL and SDA lines are connected to the I2C SCL and SDA pins. When 1, I2C SCL and SDA lines are routed internally in the peripheral, and as a result unaffected by other I2C devices. This allows a SCB I2C peripheral to address itself. Default: 0x0
15	SCB_S_NOT_READY_DATA_NACK	For internally clocked logic only. Only used when: - non EZ mode. Functionality is as follows: - 1: a received data element byte the slave is immediately NACKd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). Default: 0x1
14	SCB_S_NOT_READY_ADDR_NACK	For internally clocked logic (EC_AM is 0 and EC_OP is 0) on an address match or general call address (and S_GENERAL_IGNORE is 0). Only used when: - EC_AM is 0, EC_OP is 0 and non EZ mode. Functionality is as follows: - 1: a received (matching) slave address is immediately NACKd when the receiver FIFO is full. - 0: clock stretching is performed (till the receiver FIFO is no longer full). For externally clocked logic (EC_AM is 1) on an address match or general call address (and S_GENERAL_IGNORE is 0). Only used when (NOT used when EC_AM is 1 and EC_OP is 1 and address match and EZ mode): - EC_AM is 1 and EC_OP is 0. - EC_AM is 1 and general call address match. - EC_AM is 1 and non EZ mode. Functionality is as follows: - 1: a received (matching or general) slave address is always immediately NACKd. There are two possibilities: 1). the internally clocked logic is enabled (we are in Active system power mode) and it handles the rest of the current transfer. In this case the I2C master will not observe the NACK. 2). the internally clocked logic is not enabled (we are in DeepSleep system power mode). In this case the I2C master will observe the NACK and may retry the transfer in the future (which gives the internally clocked logic the time to wake up from DeepSleep system power mode). - 0: clock stretching is performed (till the internally clocked logic takes over). The internally clocked logic will handle the ongoing transfer as soon as it is enabled. Default: 0x1
13	SCB_S_READY_DATA_ACK	When 1, a received data element by the slave is immediately ACKd when the receiver FIFO is not full. In EZ mode, this field should be set to 1. Default: 0x1
12	SCB_S_READY_ADDR_ACK	When 1, a received (matching) slave address is immediately ACKd when the receiver FIFO is not full. In EZ mode, this field should be set to 1. Default: 0x1
11	SCB_S_GENERAL_IGNORE	When 1, a received general call slave address is immediately NACKd (no ACK or clock stretching) and treated as a non matching slave address. This is useful for slaves that do not need any data supplied within the general call structure. Default: 0x1
9	SCB_M_NOT_READY_DATA_NACK	When 1, a received data element byte the master is immediately NACKd when the receiver FIFO is full. When 0, clock stretching is used instead (till the receiver FIFO is no longer full). Default: 0x1
8	SCB_M_READY_DATA_ACK	When 1, a received data element by the master is immediately ACKd when the receiver FIFO is not full. Default: 0x1

10.1.9 SCB_I2C_CTRL (continued)

7 : 4	SCB_LOW_PHASE_OVS	Serial I2C interface low phase oversampling factor. LOW_PHASE_OVS + 1 peripheral clock periods constitute the low phase of a bit period. The valid range is [7, 15] with input signal median filtering and [6, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular (no stretching) interface (IF) low time to guarantee functional correct behavior. With input signal median filtering, the IF low time should be gt;= 8 IP clock cycles and lt;= 16 IP clock cycles. Without input signal median filtering, the IF low time should be gt;= 7 IP clock cycles and lt;= 16 IP clock cycles. Default: 0x8
3 : 0	SCB_HIGH_PHASE_OVS	Serial I2C interface high phase oversampling factor. HIGH_PHASE_OVS + 1 peripheral clock periods constitute the high phase of a bit period. The valid range is [5, 15] with input signal median filtering and [4, 15] without input signal median filtering. The field is only used in master mode. In slave mode, the field is NOT used. However, there is a frequency requirement for the IP clock wrt. the regular interface (IF) high time to guarantee functional correct behavior. With input signal median filtering, the IF high time should be gt;= 6 IP clock cycles and lt;= 16 IP clock cycles. Without input signal median filtering, the IF high time should be gt;= 5 IP clock cycles and lt;= 16 IP clock cycles. Default: 0x8

10.1.10 SCB_I2C_STATUS

Address: 0x40060064

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00							
HW Access	W							
SW Access	R							
Bit Name	SCB_EZ_ADDR [15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0	0x0	None			0x0
HW Access	None		W	W	None			W
SW Access	None		R	R	None			R
Bit Name	Reserved[7:6]		SCB_M_READ	SCB_S_READ	Reserved[3:1]			SCB_BUS_BUSY

I2C status register.

Bits	Name	Description
15 : 8	SCB_EZ_ADDR	I2C slave EZ address. This field is only reliable in internally clocked mode. In externally clocked mode the field may be unreliable, as clock domain synchronization is not performed in the design. Default: 0x00
5	SCB_M_READ	I2C master read transfer (1) or I2C master write transfer (0). When the I2C master is inactive/idle or transmitting START, REPEATED START, STOP or an address, this field is 0. Default: 0x0
4	SCB_S_READ	I2C slave read transfer (1) or I2C slave write transfer (0). When the I2C slave is inactive/idle or receiving START, REPEATED START, STOP or an address, this field is 0. Default: 0x0

10.1.10 SCB_I2C_STATUS (continued)

0	SCB_BUS_BUSY	I2C bus is busy. The bus is considered busy (1), from the time a START is detected or from the time the SCL line is 0. The bus is considered idle (0), from the time a STOP is detected. If the IP is disabled, BUS_BUSY is 0. After enabling the IP, it takes time for the BUS_BUSY to detect a busy bus. This time is the maximum high time of the SCL line. For a 100 kHz interface frequency, this maximum high time may last roughly 5 us (half a bit period). For single master systems, BUS_BUSY does not have to be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START (no bus collisions). For multi-master systems, BUS_BUSY can be used to detect an idle bus before a master starts a transfer using I2C_M_CMD.M_START_ON_IDLE (to prevent bus collisions). Default: 0x0

10.1.11 SCB_I2C_M_CMD

Address: 0x40060068

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	0x0	0x0	0x0	0x0
HW Access	None			RW1C	RW1C	RW1C	RW1C	RW1C
SW Access	None			RW	RW	RW	RW	RW
Bit Name	Reserved[7:5]			SCB_M_STOP	SCB_M_NACK	SCB_M_ACK	SCB_M_START_ON_IDLE	SCB_M_START

I2C master command register.

Bits	Name	Description
4	SCB_M_STOP	When 1, attempt to transmit a STOP. When this action is performed, the hardware sets this field to 0. This command has a higher priority than I2C_M_CMD.M_START: in situations where both a STOP and a REPEATED START could be transmitted, M_STOP takes precedence over M_START. Default: 0x0
3	SCB_M_NACK	When 1, attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to 0. Default: 0x0
2	SCB_M_ACK	When 1, attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to 0. Default: 0x0

10.1.11 SCB_I2C_M_CMD (continued)

1	SCB_M_START_ON_IDLE	When 1, transmit a START as soon as the bus is idle (I2C_STATUS.BUS_BUSY is 0, note that BUSY has a default value of 0). For bus idle detection the hardware relies on STOP detection. As a result, bus idle detection is only functional after at least one I2C bus transfer has been detected on the bus (default/reset value of BUSY is 0) . A START is only transmitted when the master state machine is in the default state. When this action is performed, the hardware sets this field to 0. Default: 0x0
0	SCB_M_START	When 1, transmit a START or REPEATED START. Whether a START or REPEATED START is transmitted depends on the state of the master state machine. A START is only transmitted when the master state machine is in the default state. A REPEATED START is transmitted when the master state machine is not in the default state, but is working on an ongoing transaction. The REPEATED START can only be transmitted after a NACK or ACK has been received for a transmitted data element or after a NACK has been transmitted for a received data element. When this action is performed, the hardware sets this field to 0. Default: 0x0

10.1.12 SCB_I2C_S_CMD

Address: 0x4006006C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	0x0
HW Access	None						RW1C	RW1C
SW Access	None						RW	RW
Bit Name	Reserved[7:2]						SCB_S_NACK	SCB_S_ACK

I2C slave command register.

Bits	Name	Description
1	SCB_S_NACK	When 1, attempt to transmit a negative acknowledgement (NACK). When this action is performed, the hardware sets this field to 0. In EZ mode, this field should be set to 0 (it is only to be used in non EZ mode). This command has a higher priority than I2C_S_CMD.S_ACK, I2C_CTRL.S_READY_ADDR_ACK or I2C_CTRL.S_READY_DATA_ACK. Default: 0x0
0	SCB_S_ACK	When 1, attempt to transmit an acknowledgement (ACK). When this action is performed, the hardware sets this field to 0. In EZ mode, this field should be set to 0 (it is only to be used in non EZ mode). Default: 0x0

10.1.13 SCB_I2C_CFG

Address: 0x40060070

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None				0x0	0x0	0x1	0x0
HW Access	None				R	R	R	R
SW Access	None				RW	RW	RW	RW
Bit Name	Reserved[31:28]				SCB_SDA_FILT_OUT_ENABLED	SCB_SDA_FILT_OUT_HS	SCB_SCL_FILT_ENABLED	SCB_SCL_FILT_HS

Bits	23	22	21	20	19	18	17	16
Reset Value	None						0x1	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[23:18]						SCB_SDA_FILT_ENABLED	SCB_SDA_FILT_HS

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x3		0x2	
HW Access	None				R		R	
SW Access	None				RW		RW	
Bit Name	Reserved[15:12]				SCB_SDA_FILT_OUT_TRIM [11:10]		SCB_SDA_FILT_OUT_HYS [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x2		0x2		0x2		0x2	
HW Access	R		R		R		R	
SW Access	RW		RW		RW		RW	
Bit Name	SCB_SCL_FILT_TRIM [7:6]		SCB_SCL_FILT_HYS [5:4]		SCB_SDA_FILT_TRIM [3:2]		SCB_SDA_FILT_HYS [1:0]	

I2C configuration register.

Bits	Name	Description
27	SCB_SDA_FILT_OUT_ENABLED	I2C SDA output delay filter enabled. Default: 0x0
26	SCB_SDA_FILT_OUT_HS	When 0: 50 ns filter. When 1: 10 ns filter. Default: 0x0

10.1.13 SCB_I2C_CFG (continued)

25	SCB_SCL_FILT_ENABLED	I2C SCL filter enabled. Default: 0x1
24	SCB_SCL_FILT_HS	When 0: 50 ns filter. When 1: 10 ns filter. Default: 0x0
17	SCB_SDA_FILT_ENABLED	I2C SDA filter enabled. Default: 0x1
16	SCB_SDA_FILT_HS	When 0: 50 ns filter. When 1: 10 ns filter. Default: 0x0
11 : 10	SCB_SDA_FILT_OUT_TRIM	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default: 0x3
9 : 8	SCB_SDA_FILT_OUT_HYS	Trim bits for the I2C SDA filter in the SDA output path (for SCL to SDA hold delay). Default: 0x2
7 : 6	SCB_SCL_FILT_TRIM	Trim bits for the I2C SCL filter. Default: 0x2
5 : 4	SCB_SCL_FILT_HYS	Trim bits for the I2C SCL filter. Default: 0x2
3 : 2	SCB_SDA_FILT_TRIM	Trim bits for the I2C SDA filter. Default: 0x2
1 : 0	SCB_SDA_FILT_HYS	Trim bits for the I2C SDA filter. Default: 0x2

10.1.14 SCB_BIST_CONTROL

Address: 0x40060100

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None		0x0	0x0	0x0	0x0	0x0	
HW Access	None		RW0C	RW	R	R	R	
SW Access	None		RW1S	R	RW	RW	RW	
Bit Name	Reserved[31:30]		SCB_RAM_GO	SCB_RAM_FAIL	SCB_RAM_WORD	SCB_RAM_PREADR	SCB_RAM_OPCNT [25:24]	

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0		0x0		0x0		0x0	
HW Access	R		R		R		R	
SW Access	RW		RW		RW		RW	
Bit Name	SCB_RAM_OP4 [23:22]		SCB_RAM_OP3 [21:20]		SCB_RAM_OP2 [19:18]		SCB_RAM_OP1 [17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[7:5]			SCB_RAM_ADDR [4:0]				

BIST control register.

Bits	Name	Description
29	SCB_RAM_GO	Firmare/Probe sets this field to start a SRAM BIST access sequence to a single SRAM location. When SRAM BIST is executing in hardware, the SRAM is disconnected from the AHB bus and any accesses to SRAM by CPU or Probe will find the AHB HREADY signal de-asserted. Default: 0x0
28	SCB_RAM_FAIL	Indicates pass/fail of the SRAM operation sequence. If any of the read operations in the BIST sequence fail, this bit will be asserted. This bit is valid only when RAM_GO=0 Default: 0x0
27	SCB_RAM_WORD	0: Byte access to SRAM (8 bits). This option is intended test byte write enable functionality 1: Word access to SRAM (16 bits) Default: 0x0

10.1.14 SCB_BIST_CONTROL (continued)

26	SCB_RAM_PREADR	0: Execute sequence as specified 1: In cycle before RAM_OP1 read data (without comparing) from ~RAM_ADDR Default: 0x0
25 : 24	SCB_RAM_OPCNT	Number of SRAM operations to execute when fired using RAM_GO. 0: only execute RAM_OP1 (opt plus PREADDR) 1: execute RAM_OP1, RAM_OP2 (opt plus PREADDR) 2: execute RAM_OP1, RAM_OP2, RAM_OP3 (opt plus PREADDR) 3: execute RAM_OP1, RAM_OP2, RAM_OP3, RAM_OP4 (opt plus PREADDR) Default: 0x0
23 : 22	SCB_RAM_OP4	Fourth SRAM BIST operation: 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
21 : 20	SCB_RAM_OP3	Third SRAM BIST operation: 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
19 : 18	SCB_RAM_OP2	Second SRAM BIST operation: 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
17 : 16	SCB_RAM_OP1	First SRAM BIST operation: 0: Write BIST_DATA 1: Write ~BIST_DATA 2: Read and compare against BIST_DATA 3: Read and compare against ~BIST_DATA Default: 0x0
4 : 0	SCB_RAM_ADDR	Address for SRAM BIST sequence. The lower 1 bit is used to identify a byte location in a 16-bit wide SRAM and are used to test byte write enable functionality. If RAM_WORD is 0, byte write enable functionality is tested and the lower 1 bit is used. If RAM_WORD is 1, 16-bit word functionality is tested and the lower 1 bit is NOT used. Default: 0x00

10.1.15 SCB_BIST_DATA

Address: 0x40060104

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SCB_RAM_DATA [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	SCB_RAM_DATA [15: 0]							

BIST data register.

Bits	Name	Description
15 : 0	SCB_RAM_DATA	Data pattern for BIST sequence. If RAM_WORD=0, only bits [7:0] are used. Default: 0x0000

10.1.16 SCB_TX_CTRL

Address: 0x40060200

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SCB_ENABLED	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x1
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[15:9]							SCB_MSB_FIRST

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x7			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				SCB_DATA_WIDTH [3:0]			

Transmitter control register.

Bits	Name	Description
31	SCB_ENABLED	Transmitter enabled. The transmitter should be enabled for all protocols that transmit data (from either the EZ memory or from the TX FIFO). If not enabled, the protocol may not function as it does not get data to transmit. Default: 0x0
8	SCB_MSB_FIRST	Least significant bit first (0) or most significant bit first (1). For I2C, this field should be 1. Default: 0x1
3 : 0	SCB_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the amount of bits in a transmitted data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. Default: 0x7

10.1.17 SCB_TX_FIFO_CTRL

Address: 0x40060204

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[23:18]						SCB_FREEZE	SCB_CLEAR

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0		
HW Access	None					R		
SW Access	None					RW		
Bit Name	Reserved[7:3]					SCB_TRIGGER_LEVEL [2:0]		

Transmitter FIFO control register.

Bits	Name	Description
17	SCB_FREEZE	When 1, hardware reads from the transmitter FIFO do not remove FIFO entries. Freeze will not advance the TX FIFO read pointer. Default: 0x0
16	SCB_CLEAR	When 1, the transmitter FIFO and transmitter shift register are cleared/invalidated. Invalidation will last for as long as this field is 1. If a quick clear/invalidation is required, the field should be set to 1 and be followed by a set to 0. If a clear/invalidation is required for an extended time period, the field should be set to 1 during the complete time period. Default: 0x0
2 : 0	SCB_TRIGGER_LEVEL	Trigger level. When the transmitter FIFO has less entries than the amount of this field, a transmitter trigger event is generated. Default: 0x0

10.1.18 SCB_TX_FIFO_STATUS

Address: 0x40060208

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None					0x0		
HW Access	None					W		
SW Access	None					R		
Bit Name	Reserved[31:27]					SCB_WR_PTR [26:24]		

Bits	23	22	21	20	19	18	17	16
Reset Value	None					0x0		
HW Access	None					W		
SW Access	None					R		
Bit Name	Reserved[23:19]					SCB_RD_PTR [18:16]		

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	None						
HW Access	W	None						
SW Access	R	None						
Bit Name	SCB_SR_VALID	Reserved[14:8]						

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				W			
SW Access	None				R			
Bit Name	Reserved[7:4]				SCB_USED [3:0]			

Transmitter FIFO status register.

Bits	Name	Description
26 : 24	SCB_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written. Default: 0x0
18 : 16	SCB_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read by the hardware. Default: 0x0
15	SCB_SR_VALID	Indicates whether the TX shift registers holds a valid data frame (1) or not (0). The shift register can be considered the top of the TX FIFO (the data frame is not included in the USED field of the TX FIFO). The shift register is a working register and holds the data frame that is currently transmitted (when the protocol state machine is transmitting a data frame) or the data frame that is tranmitted next (when the protocol state machine is not transmitting a data frame). Default: 0x0
3 : 0	SCB_USED	Amount of enties in the transmitter FIFO. The value of this field ranges from 0 to 8. Default: 0x0

10.1.19 SCB_TX_FIFO_WR

Address: 0x40060240

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	W							
Bit Name	SCB_DATA [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	W							
Bit Name	SCB_DATA [15: 0]							

Transmitter FIFO write register.

Bits	Name	Description
15 : 0	SCB_DATA	Data frame written into the transmitter FIFO. Behavior is similar to that of a PUSH operation. Default: 0x0000

10.1.20 SCB_RX_CTRL

Address: 0x40060300

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SCB_ENABLED	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	0x1
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[15:10]						SCB_MEDIAN	SCB_MSB_FIRST

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x7			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				SCB_DATA_WIDTH [3:0]			

Receiver control register.

Bits	Name	Description
31	SCB_ENABLED	Receiver enabled. The receiver should be enabled for all protocols that receive data (to either the EZ memory or to the RX FIFO). If not enabled, the protocol may not function or received data may get lost. Default: 0x0
9	SCB_MEDIAN	Median filter. When 1, a digital 3 taps median filter is performed on input interface lines. This filter should reduce the susceptability to errors. However, its requires higher oversampling values. For UART IrDA submode, this field should always be 1. Default: 0x0
8	SCB_MSB_FIRST	Least significant bit first (0) or most significant bit first (1). For I2C, this field should be 1. Default: 0x1

10.1.20 SCB_RX_CTRL (continued)

3 : 0	SCB_DATA_WIDTH	Dataframe width. DATA_WIDTH + 1 is the expected amount of bits in received data frame. This number does not include start, parity and stop bits. For UART mode, the valid range is [3, 8]. For SPI, the valid range is [3, 15]. For I2C the only valid value is 7. In EZ mode (for both SPI and I2C), the only valid value is 7. Default: 0x7

10.1.21 SCB_RX_FIFO_CTRL

Address: 0x40060304

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[23:18]						SCB_FREEZE	SCB_CLEAR

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x7		
HW Access	None					R		
SW Access	None					RW		
Bit Name	Reserved[7:3]					SCB_TRIGGER_LEVEL [2:0]		

Receiver FIFO control register.

Bits	Name	Description
17	SCB_FREEZE	When 1, hardware writes to the receiver FIFO have no effect. Freeze will not advance the RX FIFO write pointer. Default: 0x0
16	SCB_CLEAR	When 1, the receiver FIFO and receiver shift register are cleared/invalidated. Invalidation will last for as long as this field is 1. If a quick clear/invalidation is required, the field should be set to 1 and be followed by a set to 0. If a clear/invalidation is required for an extended time period, the field should be set to 1 during the complete time period. Default: 0x0
2 : 0	SCB_TRIGGER_LEVEL	Trigger level. When the receiver FIFO has more entries than the amount of this field, a receiver trigger event is generated. Default: 0x7

10.1.22 SCB_RX_FIFO_STATUS

Address: 0x40060308

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None					0x0		
HW Access	None					W		
SW Access	None					R		
Bit Name	Reserved[31:27]					SCB_WR_PTR [26:24]		

Bits	23	22	21	20	19	18	17	16
Reset Value	None					0x0		
HW Access	None					W		
SW Access	None					R		
Bit Name	Reserved[23:19]					SCB_RD_PTR [18:16]		

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	None						
HW Access	W	None						
SW Access	R	None						
Bit Name	SCB_SR_VALID	Reserved[14:8]						

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				W			
SW Access	None				R			
Bit Name	Reserved[7:4]				SCB_USED [3:0]			

Receiver FIFO status register.

Bits	Name	Description
26 : 24	SCB_WR_PTR	FIFO write pointer: FIFO location at which a new data frame is written by the hardware. Default: 0x0
18 : 16	SCB_RD_PTR	FIFO read pointer: FIFO location from which a data frame is read. Default: 0x0
15	SCB_SR_VALID	Indicates whether the RX shift registers holds a (partial) valid data frame (1) or not (0). The shift register can be considered the bottom of the RX FIFO (the data frame is not included in the USED field of the RX FIFO). The shift register is a working register and holds the data frame that is currently being received (when the protocol state machine is receiving a data frame). Default: 0x0
3 : 0	SCB_USED	Amount of enties in the receiver FIFO. The value of this field ranges from 0 to 8. Default: 0x0

10.1.23 SCB_RX_MATCH

Address: 0x40060310

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SCB_MASK [23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SCB_ADDR [7:0]							

Slave address and mask register.

Bits	Name	Description
23 : 16	SCB_MASK	Slave device address mask. This field is a 8 bit mask that specifies which of the ADDR field bits in the SCB_RX_MATCH_ADDR register take part in the matching of the slave address: MATCH = ((ADDR MASK) == (slave address MASK)). Default: 0x00
7 : 0	SCB_ADDR	Slave device address. For UART multi-processor moden all eight bits a reused. For I2C, bit 0 of the register is not used. This reflects the organization of the first transmitted byte in a I2C transfer: the first 7 bits represent the address of the addressed slave, and the next 1 bit is a read/write indicator (0: write, 1: read). Default: 0x00

10.1.24 SCB_RX_FIFO_RD

Address: 0x40060340

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SCB_DATA [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SCB_DATA [15: 0]							

Receiver FIFO read register.

Bits	Name	Description
15 : 0	SCB_DATA	Data read from the receiver FIFO. Reading a data frame will remove the data frame from the FIFO; i.e. behavior is similar to that of a POP operation. This register has a side effect when read by software: a data frame is removed from the FIFO. This may be undesirable during debug; i.e. a read during debug should NOT have a side effect. To this end, the IP uses the AHB-Lite hmaster[0] input signal. When this signal is 1 in the address cycle of a bus transfer, a read transfer will not have a side effect. As a result, a read from this register will not remove a data frame from the FIFO. As a result, a read from this register behaves as a read from the SCB_RX_FIFO_RD_SILENT register. Default: 0x0000

10.1.25 SCB_RX_FIFO_RD_SILENT

Address: 0x40060344

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SCB_DATA [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	W							
SW Access	R							
Bit Name	SCB_DATA [15: 0]							

Receiver FIFO read register.

Bits	Name	Description
15 : 0	SCB_DATA	Data read from the receiver FIFO. Reading a data frame will NOT remove the data frame from the FIFO; i.e. behavior is similar to that of a PEEK operation. Default: 0x0000

10.1.26 SCB_EZ_DATA

Address: 0x40060400

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	RW							
Bit Name	SCB_EZ_DATA [7:0]							

EZ memory location registers.

Bits	Name	Description
7 : 0	SCB_EZ_DATA	Data in EZ memory location. Default: 0x00

10.1.27 SCB_INTR_CAUSE

Address: 0x40060E00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None		W	W	W	W	W	W
SW Access	None		R	R	R	R	R	R
Bit Name	Reserved[7:6]		SCB_SPI_EC	SCB_I2C_EC	SCB_RX	SCB_TX	SCB_S	SCB_M

Active clocked interrupt signal register

Bits	Name	Description
5	SCB_SPI_EC	Externally clocked SPI interrupt active (interrupt_spi_ec): INTR_SPI_EC_MASKED != 0. Default: 0x0
4	SCB_I2C_EC	Externally clock I2C interrupt active (interrupt_i2c_ec): INTR_I2C_EC_MASKED != 0. Default: 0x0
3	SCB_RX	Receiver interrupt active (interrupt_rx): INTR_RX_MASKED != 0. Default: 0x0
2	SCB_TX	Transmitter interrupt active (interrupt_tx): INTR_TX_MASKED != 0. Default: 0x0
1	SCB_S	Slave interrupt active (interrupt_slave): INTR_S_MASKED != 0. Default: 0x0

10.1.27 SCB_INTR_CAUSE (continued)

0	SCB_M	Master interrupt active (interrupt_master): INTR_M_MASKED != 0. Default: 0x0

10.1.28 SCB_INTR_I2C_EC

Address: 0x40060E80

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					None	None	None
SW Access	None					RW1C	RW1C	RW1C
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked I2C interrupt request register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	STOP detection after a write transfer occurred (only available in EZ mode). Active on detected STOP. Only generated when a write transfer to the EZ memory occurred between the STOP and the preceding START (note that multiple REPEATED STARTs may have happened in between the START and STOP). If a write transfer only modified the EZ address, and not the EZ memory, this event is NOT generated. Only used in EZ mode and when EC_OP is 1. Default: 0x0
1	SCB_EZ_STOP	STOP detection (only available in EZ mode). Active on detected STOP. Only used in EZ mode and when EC_OP is 1. Default: 0x0

10.1.28 SCB_INTR_I2C_EC (continued)

0	SCB_WAKE_UP	Wake up request. Active on incoming slave request (with address match). Only used when EC_AM is 1. Default: 0x0

10.1.29 SCB_INTR_I2C_EC_MASK

Address: 0x40060E88

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked I2C interrupt mask register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
1	SCB_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.30 SCB_INTR_I2C_EC_MASKED

Address: 0x40060E8C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					W	W	W
SW Access	None					R	R	R
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked I2C interrupt masked register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default: 0x0
1	SCB_EZ_STOP	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_WAKE_UP	Logical and of corresponding request and mask bits. Default: 0x0

10.1.31 SCB_INTR_SPI_EC

Address: 0x40060EC0

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					None	None	None
SW Access	None					RW1C	RW1C	RW1C
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked SPI interrupt request register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	STOP detection after a write transfer occurred. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). If a write transfer only transferred the EZ address, this event will not be generated. This event is an indication that a EZ memory location may have changed contents. Only used in EZ mode and when EC_OP is 1. Default: 0x0
1	SCB_EZ_STOP	STOP detection. Active on detected STOP (deselection) when externally clocked operation is on (only available in EZ mode). Only used in EZ mode and when EC_OP is 1. Default: 0x0

10.1.31 SCB_INTR_SPI_EC (continued)

0	SCB_WAKE_UP	Wake up request. Active on incoming slave request when externally clocked selection is 1. Only used when EC_AM is 1. Default: 0x0

10.1.32 SCB_INTR_SPI_EC_MASK

Address: 0x40060EC8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked SPI interrupt mask register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
1	SCB_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_WAKE_UP	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.33 SCB_INTR_SPI_EC_MASKED

Address: 0x40060ECC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					W	W	W
SW Access	None					R	R	R
Bit Name	Reserved[7:3]					SCB_EZ_WRITE_STOP	SCB_EZ_STOP	SCB_WAKE_UP

Externally clocked SPI interrupt masked register

Bits	Name	Description
2	SCB_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default: 0x0
1	SCB_EZ_STOP	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_WAKE_UP	Logical and of corresponding request and mask bits. Default: 0x0

10.1.34 SCB_INTR_M

Address: 0x40060F00

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	0x0
HW Access	None						RW1S	RW1S
SW Access	None						RW1C	RW1C
Bit Name	Reserved[15:10]						SCB_SPI_DONE	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None	0x0	0x0	0x0
HW Access	None			RW1S	None	RW1S	RW1S	RW1S
SW Access	None			RW1C	None	RW1C	RW1C	RW1C
Bit Name	Reserved[7:5]			SCB_I2C_STOP	Reserved	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Master interrupt request register.

Bits	Name	Description
9	SCB_SPI_DONE	SPI master transfer done event: all data frames in the transmit FIFO are sent and the transmit FIFO is empty. Only used when EC_OP is 0. Default: 0x0
8	SCB_I2C_BUS_ERROR	I2C master bus error (unexpected detection of START or STOP condition). Only used when EC_OP is 0. Default: 0x0

10.1.34 SCB_INTR_M (continued)

4	SCB_I2C_STOP	I2C master STOP. Set to 1, when the master has transmitted a STOP. Only used when EC_OP is 0. Default: 0x0
2	SCB_I2C_ACK	I2C master acknowledgement. Set to 1, when the master receives a ACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is 0. Default: 0x0
1	SCB_I2C_NACK	I2C master negative acknowledgement. Set to 1, when the master receives a NACK (typically after the master transmitted the slave address or TX data). Only used when EC_OP is 0. Default: 0x0
0	SCB_I2C_ARB_LOST	I2C master lost arbitration: the value driven by the master on the SDA line is not the same as the value observed on the SDA line. Only used when EC_OP is 0. Default: 0x0

10.1.35 SCB_INTR_M_SET

Address: 0x40060F04

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	0x0
HW Access	None						None	None
SW Access	None						RW1S	RW1S
Bit Name	Reserved[15:10]						SCB_SPI_DONE	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None	0x0	0x0	0x0
HW Access	None			None	None	None	None	None
SW Access	None			RW1S	None	RW1S	RW1S	RW1S
Bit Name	Reserved[7:5]			SCB_I2C_STOP	Reserved	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Master interrupt set request register

Bits	Name	Description
9	SCB_SPI_DONE	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
8	SCB_I2C_BUS_ERROR	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
4	SCB_I2C_STOP	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
2	SCB_I2C_ACK	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.35 SCB_INTR_M_SET (continued)

1	SCB_I2C_NACK	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
0	SCB_I2C_ARB_LOST	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.36 SCB_INTR_M_MASK

Address: 0x40060F08

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[15:10]						SCB_SPI_DONE	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None	0x0	0x0	0x0
HW Access	None			R	None	R	R	R
SW Access	None			RW	None	RW	RW	RW
Bit Name	Reserved[7:5]			SCB_I2C_STOP	Reserved	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Master interrupt mask register.

Bits	Name	Description
9	SCB_SPI_DONE	Mask bit for corresponding bit in interrupt request register. Default: 0x0
8	SCB_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default: 0x0
4	SCB_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
2	SCB_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.36 SCB_INTR_M_MASK (continued)

1	SCB_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.37 SCB_INTR_M_MASKED

Address: 0x40060F0C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	0x0
HW Access	None						W	W
SW Access	None						R	R
Bit Name	Reserved[15:10]						SCB_SPI_DONE	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	None	0x0	0x0	0x0
HW Access	None			W	None	W	W	W
SW Access	None			R	None	R	R	R
Bit Name	Reserved[7:5]			SCB_I2C_STOP	Reserved	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Master interrupt masked request register

Bits	Name	Description
9	SCB_SPI_DONE	Logical and of corresponding request and mask bits. Default: 0x0
8	SCB_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default: 0x0
4	SCB_I2C_STOP	Logical and of corresponding request and mask bits. Default: 0x0
2	SCB_I2C_ACK	Logical and of corresponding request and mask bits. Default: 0x0

10.1.37 SCB_INTR_M_MASKED (continued)

1	SCB_I2C_NACK	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default: 0x0

10.1.38 SCB_INTR_S

Address: 0x40060F40

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW1S	RW1S	RW1S	RW1S
SW Access	None				RW1C	RW1C	RW1C	RW1C
Bit Name	Reserved[15:12]				SCB_SPI_BUS_ERROR	SCB_SPI_EZ_STOP	SCB_SPI_EZ_WRITE_STOP	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	SCB_I2C_GENERAL	SCB_I2C_ADDR_MATCH	SCB_I2C_START	SCB_I2C_STOP	SCB_I2C_WRITE_STOP	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Slave interrupt request register.

Bits	Name	Description
11	SCB_SPI_BUS_ERROR	SPI slave deselected at an unexpected time in the SPI transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is 0. Default: 0x0
10	SCB_SPI_EZ_STOP	SPI slave deselected after any EZ SPI transfer occured. Only used when EC_OP is 0. Default: 0x0

10.1.38 SCB_INTR_S (continued)

9	SCB_SPI_EZ_WRITE_STOP	SPI slave deselected after a write EZ SPI transfer occurred. Only used when EC_OP is 0. Default: 0x0
8	SCB_I2C_BUS_ERROR	I2C slave bus error (unexpected detection of START or STOP condition). This should not occur, it represents erroneous I2C bus behaviour. In case of a bus error, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is 0. Default: 0x0
7	SCB_I2C_GENERAL	I2C slave general call address received. If CTRL.ADDR_ACCEPT, the received address 0x00 (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is 1) and internally clocked operation (CTRL.EC_OP_MODE is 0), this field is set when the event is detected. Only used when EC_OP is 0. Default: 0x0
6	SCB_I2C_ADDR_MATCH	I2C slave matching address received. If CTRL.ADDR_ACCEPT, the received address (including the R/W bit) is available in the RX FIFO. In the case of externally clocked address matching (CTRL.EC_AM_MODE is 1) and internally clocked operation (CTRL.EC_OP_MODE is 0), this field is set when the event is detected. Only used when EC_OP is 0. Default: 0x0
5	SCB_I2C_START	I2C slave START received. Set to 1, when START or REPEATED START event is detected. In the case of externally clocked address matching (CTRL.EC_AM_MODE is 1) and internally clocked operation (CTRL.EC_OP_MODE is 0), this field is NOT set. Instead the Firmware can rely on I2C_ADDR_MATCH and I2C_GENERAL. Only used when EC_OP is 0. Default: 0x0
4	SCB_I2C_STOP	I2C STOP event for I2C (read or write) transfer intended for this slave (address matching is performed). Set to 1, when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is 0. Default: 0x0
3	SCB_I2C_WRITE_STOP	I2C STOP event for I2C write transfer intended for this slave (address matching is performed). In non EZ mode, the event is detected on any I2C write transfer intended for this slave. In EZ mode, the event is detected only on I2C write transfers that have EZ data written to the memory structure (an I2C write transfer that only communicates an EZ address, will not result in this event being detected). Set to 1, when STOP or REPEATED START event is detected. The REPEATED START event is included in this interrupt cause such that the I2C transfers seperated by a REPEATED START can be distinguished and potentially treated seperately by the Firmware. Note that the second I2C transfer may be to a different slave address. Only used when EC_OP is 0. Default: 0x0

10.1.38 SCB_INTR_S (continued)

2	SCB_I2C_ACK	I2C slave acknowledgement received. Set to 1, when the slave receives a ACK (typically after the slave transmitted TX data). Only used when EC_OP is 0. Default: 0x0
1	SCB_I2C_NACK	I2C slave negative acknowledgement received. Set to 1, when the slave receives a NACK (typically after the slave transmitted TX data). Only used when EC_OP is 0. Default: 0x0
0	SCB_I2C_ARB_LOST	I2C slave lost arbitration: the value driven on the SDA line is not the same as the value observed on the SDA line (while the SCL line is 1). This should not occur, it represents erroneous I2C bus behaviour. In case of lost arbitration, the I2C slave state machine abort the ongoing transfer. The Firmware may decide to clear the TX and RX FIFOs in case of this error. Only used when EC_OP is 0. Default: 0x0

10.1.39 SCB_INTR_S_SET

Address: 0x40060F44

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				None	None	None	None
SW Access	None				RW1S	RW1S	RW1S	RW1S
Bit Name	Reserved[15:12]				SCB_SPI_BUS_ERROR	SCB_SPI_EZ_STOP	SCB_SPI_EZ_WRITE_STOP	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
Bit Name	SCB_I2C_GENERAL	SCB_I2C_ADDR_MATCH	SCB_I2C_START	SCB_I2C_STOP	SCB_I2C_WRITE_STOP	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Slave interrupt set request register.

Bits	Name	Description
11	SCB_SPI_BUS_ERROR	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
10	SCB_SPI_EZ_STOP	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
9	SCB_SPI_EZ_WRITE_STOP	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
8	SCB_I2C_BUS_ERROR	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.39 SCB_INTR_S_SET (continued)

7	SCB_I2C_GENERAL	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
6	SCB_I2C_ADDR_MATCH	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
5	SCB_I2C_START	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
4	SCB_I2C_STOP	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
3	SCB_I2C_WRITE_STOP	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
2	SCB_I2C_ACK	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
1	SCB_I2C_NACK	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
0	SCB_I2C_ARB_LOST	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.40 SCB_INTR_S_MASK

Address: 0x40060F48

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				R	R	R	R
SW Access	None				RW	RW	RW	RW
Bit Name	Reserved[15:12]				SCB_SPI_BUS_ERROR	SCB_SPI_EZ_STOP	SCB_SPI_EZ_WRITE_STOP	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	SCB_I2C_GENERAL	SCB_I2C_ADDR_MATCH	SCB_I2C_START	SCB_I2C_STOP	SCB_I2C_WRITE_STOP	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Slave interrupt mask register.

Bits	Name	Description
11	SCB_SPI_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default: 0x0
10	SCB_SPI_EZ_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
9	SCB_SPI_EZ_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
8	SCB_I2C_BUS_ERROR	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.40 SCB_INTR_S_MASK (continued)

7	SCB_I2C_GENERAL	Mask bit for corresponding bit in interrupt request register. Default: 0x0
6	SCB_I2C_ADDR_MATCH	Mask bit for corresponding bit in interrupt request register. Default: 0x0
5	SCB_I2C_START	Mask bit for corresponding bit in interrupt request register. Default: 0x0
4	SCB_I2C_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
3	SCB_I2C_WRITE_STOP	Mask bit for corresponding bit in interrupt request register. Default: 0x0
2	SCB_I2C_ACK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
1	SCB_I2C_NACK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_I2C_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.41 SCB_INTR_S_MASKED

Address: 0x40060F4C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				W	W	W	W
SW Access	None				R	R	R	R
Bit Name	Reserved[15:12]				SCB_SPI_BUS_ERROR	SCB_SPI_EZ_STOP	SCB_SPI_EZ_WRITE_STOP	SCB_I2C_BUS_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	W	W	W	W	W	W	W	W
SW Access	R	R	R	R	R	R	R	R
Bit Name	SCB_I2C_GENERAL	SCB_I2C_ADDR_MATCH	SCB_I2C_START	SCB_I2C_STOP	SCB_I2C_WRITE_STOP	SCB_I2C_ACK	SCB_I2C_NACK	SCB_I2C_ARB_LOST

Slave interrupt masked request register

Bits	Name	Description
11	SCB_SPI_BUS_ERROR	Logical and of corresponding request and mask bits. Default: 0x0
10	SCB_SPI_EZ_STOP	Logical and of corresponding request and mask bits. Default: 0x0
9	SCB_SPI_EZ_WRITE_STOP	Logical and of corresponding request and mask bits. Default: 0x0
8	SCB_I2C_BUS_ERROR	Logical and of corresponding request and mask bits. Default: 0x0

10.1.41 SCB_INTR_S_MASKED (continued)

7	SCB_I2C_GENERAL	Logical and of corresponding request and mask bits. Default: 0x0
6	SCB_I2C_ADDR_MATCH	Logical and of corresponding request and mask bits. Default: 0x0
5	SCB_I2C_START	Logical and of corresponding request and mask bits. Default: 0x0
4	SCB_I2C_STOP	Logical and of corresponding request and mask bits. Default: 0x0
3	SCB_I2C_WRITE_STOP	Logical and of corresponding request and mask bits. Default: 0x0
2	SCB_I2C_ACK	Logical and of corresponding request and mask bits. Default: 0x0
1	SCB_I2C_NACK	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_I2C_ARB_LOST	Logical and of corresponding request and mask bits. Default: 0x0

10.1.42 SCB_INTR_TX

Address: 0x40060F80

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	0x0
HW Access	None					RW1S	RW1S	RW1S
SW Access	None					RW1C	RW1C	RW1C
Bit Name	Reserved[15:11]					SCB_UART_ARB_LOST	SCB_UART_DONE	SCB_UART_NACK

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x1	None		0x1	0x0
HW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
SW Access	RW1C	RW1C	RW1C	RW1C	None		RW1C	RW1C
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	SCB_EMPTY	Reserved[3:2]		SCB_NOT_FULL	SCB_TRIGGER

Transmitter interrupt request register.

Bits	Name	Description
10	SCB_UART_ARB_LOST	UART lost arbitration: the value driven on the TX line is not the same as the value observed on the RX line. This condition event is usefull when transmitter and receiver share a TX/RX line. This is the case in LIN or SmartCard modes. Set to 1, when event is detected. Write with 1 to clear bit. Default: 0x0
9	SCB_UART_DONE	UART transmitter done event. This happens when the IP is done transferring all data in the TX FIFO; i.e. EMPTY is 1. Set to 1, when event is detected. Write with 1 to clear bit. Default: 0x0

10.1.42 SCB_INTR_TX (continued)

8	SCB_UART_NACK	UART transmitter received a negative acknowledgement in SmartCard mode. Set to 1, when event is detected. Write with 1 to clear bit. Default: 0x0
7	SCB_BLOCKED	AHB-Lite write transfer can not get access to the EZ memory (EZ data access), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is 1. Default: 0x0
6	SCB_UNDERFLOW	Attempt to read from an empty TX FIFO. This happens when the IP is ready to transfer data and EMPTY is 1. Only used in non EZ mode and when EC_OP is 0. Default: 0x0
5	SCB_OVERFLOW	Attempt to write to a full TX FIFO. Only used in non EZ mode and when EC_OP is 0. Default: 0x0
4	SCB_EMPTY	TX FIFO is empty; i.e. it has 0 entries. Only used in non EZ mode and when EC_OP is 0. Default: 0x1
1	SCB_NOT_FULL	TX FIFO is not full. Only used in non EZ mode and when EC_OP is 0. Default: 0x1
0	SCB_TRIGGER	Less entries in the TX FIFO than the value specified by TRIGGER_LEVEL in SCB_TX_FIFO_CTL. Only used in non EZ mode and when EC_OP is 0. Default: 0x0

10.1.43 SCB_INTR_TX_SET

Address: 0x40060F84

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	0x0
HW Access	None					None	None	None
SW Access	None					RW1S	RW1S	RW1S
Bit Name	Reserved[15:11]					SCB_UART_ARB_LOST	SCB_UART_DONE	SCB_UART_NACK

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x1	None		0x1	0x0
HW Access	None	None	None	None	None		None	None
SW Access	RW1S	RW1S	RW1S	RW1S	None		RW1S	RW1S
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	SCB_EMPTY	Reserved[3:2]		SCB_NOT_FULL	SCB_TRIGGER

Transmitter interrupt set request register

Bits	Name	Description
10	SCB_UART_ARB_LOST	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
9	SCB_UART_DONE	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
8	SCB_UART_NACK	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
7	SCB_BLOCKED	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.43 SCB_INTR_TX_SET (continued)

6	SCB_UNDERFLOW	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
5	SCB_OVERFLOW	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0
4	SCB_EMPTY	Write with 1 to set corresponding bit in interrupt request register. Default: 0x1
1	SCB_NOT_FULL	Write with 1 to set corresponding bit in interrupt request register. Default: 0x1
0	SCB_TRIGGER	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.44 SCB_INTR_TX_MASK

Address: 0x40060F88

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[15:11]					SCB_UART_ARB_LOST	SCB_UART_DONE	SCB_UART_NACK

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	None		0x0	0x0
HW Access	R	R	R	R	None		R	R
SW Access	RW	RW	RW	RW	None		RW	RW
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	SCB_EMPTY	Reserved[3:2]		SCB_NOT_FULL	SCB_TRIGGER

Transmitter interrupt mask register.

Bits	Name	Description
10	SCB_UART_ARB_LOST	Mask bit for corresponding bit in interrupt request register. Default: 0x0
9	SCB_UART_DONE	Mask bit for corresponding bit in interrupt request register. Default: 0x0
8	SCB_UART_NACK	Mask bit for corresponding bit in interrupt request register. Default: 0x0
7	SCB_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.44 SCB_INTR_TX_MASK (continued)

6	SCB_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default: 0x0
5	SCB_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default: 0x0
4	SCB_EMPTY	Mask bit for corresponding bit in interrupt request register. Default: 0x0
1	SCB_NOT_FULL	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.45 SCB_INTR_TX_MASKED

Address: 0x40060F8C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None					0x0	0x0	0x0
HW Access	None					W	W	W
SW Access	None					R	R	R
Bit Name	Reserved[15:11]					SCB_UART_ARB_LOST	SCB_UART_DONE	SCB_UART_NACK

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	None		0x0	0x0
HW Access	W	W	W	W	None		W	W
SW Access	R	R	R	R	None		R	R
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	SCB_EMPTY	Reserved[3:2]		SCB_NOT_FULL	SCB_TRIGGER

Transmitter interrupt masked request register

Bits	Name	Description
10	SCB_UART_ARB_LOST	Logical and of corresponding request and mask bits. Default: 0x0
9	SCB_UART_DONE	Logical and of corresponding request and mask bits. Default: 0x0
8	SCB_UART_NACK	Logical and of corresponding request and mask bits. Default: 0x0
7	SCB_BLOCKED	Logical and of corresponding request and mask bits. Default: 0x0

10.1.45 SCB_INTR_TX_MASKED (continued)

6	SCB_UNDERFLOW	Logical and of corresponding request and mask bits. Default: 0x0
5	SCB_OVERFLOW	Logical and of corresponding request and mask bits. Default: 0x0
4	SCB_EMPTY	Logical and of corresponding request and mask bits. Default: 0x0
1	SCB_NOT_FULL	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_TRIGGER	Logical and of corresponding request and mask bits. Default: 0x0

10.1.46 SCB_INTR_RX

Address: 0x40060FC0

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW1S	RW1S	RW1S	RW1S
SW Access	None				RW1C	RW1C	RW1C	RW1C
Bit Name	Reserved[15:12]				SCB_BREAK_DETECT	SCB_BAUD_DETECT	SCB_PARITY_ERROR	SCB_FRAME_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	None	0x0	0x0	None	0x0
HW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
SW Access	RW1C	RW1C	RW1C	None	RW1C	RW1C	None	RW1C
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	Reserved	SCB_FULL	SCB_NOT_EMPTY	Reserved	SCB_TRIGGER

Receiver interrupt request register.

Bits	Name	Description
11	SCB_BREAK_DETECT	Break detection is successful: the line is 0 for UART_RX_CTRL.BREAK_WIDTH + 1 bit period. Can occur at any time to address unanticipated break fields; i.e. break-in-data is supported. This feature is supported for the UART standard and LIN submodes. For the UART standard sub-modes, ongoing receipt of data frames is NOT affected; i.e. Firmware is ecpected to take the proper action. For the LIN submode, possible ongoing receipt of a data frame is stopped and the (partially) received data frame is dropped and baud rate detection is started. Set to 1, when event is detected. Write with 1 to clear bit. Default: 0x0

10.1.46 SCB_INTR_RX (continued)

10	SCB_BAUD_DETECT	LIN baudrate detection is completed. The receiver software uses the UART_RX_STATUS.BR_COUNTER value to set the right IP clock (from the programmable clock IP) to guarantee successful receipt of the first LIN data frame (Protected Identifier Field) after the synchronization byte. Set to 1, when event is detected. Write with 1 to clear bit. Default: 0x0
9	SCB_PARITY_ERROR	Parity error in received data frame. Set to 1, when event is detected. Write with 1 to clear bit. If UART_RX_CTL.DROP_ON_PARITY_ERROR is 1, the received frame is dropped. If UART_RX_CTL.DROP_ON_PARITY_ERROR is 0, the received frame is send to the RX FIFO. In SmartCard submode, negatively acknowledged data frames generate a parity error. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO. Default: 0x0
8	SCB_FRAME_ERROR	Frame error in received data frame. Set to 1, when event is detected. Write with 1 to clear bit. This can be either a start or stop bit(s) error: Start bit error: after the detection of the beginning of a start bit period (RX line changes from 1 to 0), the middle of the start bit period is sampled erroneously (RX line is 1). Note: a start bit error is detected BEFORE a data frame is received. Stop bit error: the RX line is sampled as 0, but a 1 was expected. Note: a stop bit error may result in failure to receive successive data frame(s). Note: a stop bit error is detected AFTER a data frame is received. A stop bit error is detected after a data frame is received, and the UART_RX_CTL.DROP_ON_FRAME_ERROR field specifies whether the received frame is dropped or send to the RX FIFO. If UART_RX_CTL.DROP_ON_FRAME_ERROR is 1, the received data frame is dropped. If UART_RX_CTL.DROP_ON_FRAME_ERROR is 0, the received data frame is send to the RX FIFO. Note that Firmware can only identify the erroneous data frame in the RX FIFO if it is fast enough to read the data frame before the hardware writes a next data frame into the RX FIFO; i.e. the RX FIFO does not have error flags to tag erroneous data frames. Default: 0x0
7	SCB_BLOCKED	AHB-Lite read transfer can not get access to the EZ memory (EZ_DATA accesses), due to an externally clocked EZ access. This may happen when STATUS.EC_BUSY is 1. Default: 0x0
6	SCB_UNDERFLOW	Attempt to read from an empty RX FIFO. Only used in non EZ mode and when EC_OP is 0. Default: 0x0
5	SCB_OVERFLOW	Attempt to write to a full RX FIFO. Note: in I2C mode, the OVERFLOW is set when a data frame is received and the RX FIFO is full, independent of whether it is ACKd or NACKd. Only used in non EZ mode and when EC_OP is 0. Default: 0x0
3	SCB_FULL	RX FIFO is full. Note that received data frames are lost when the RX FIFO is full. Only used in non EZ mode and when EC_OP is 0. Default: 0x0
2	SCB_NOT_EMPTY	RX FIFO is not empty. Only used in non EZ mode and when EC_OP is 0. Default: 0x0

10.1.46 SCB_INTR_RX (continued)

0	SCB_TRIGGER	More entries in the RX FIFO than the value specified by TRIGGER_LEVEL in SCB_RX_FIFO_CTL. Only used in non EZ mode and when EC_OP is 0. Default: 0x0

10.1.47 SCB_INTR_RX_SET

Address: 0x40060FC4

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				None	None	None	None
SW Access	None				RW1S	RW1S	RW1S	RW1S
Bit Name	Reserved[15:12]				SCB_BREAK_DETECT	SCB_BAUD_DETECT	SCB_PARITY_ERROR	SCB_FRAME_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	None	0x0	0x0	None	0x0
HW Access	None	None	None	None	None	None	None	None
SW Access	RW1S	RW1S	RW1S	None	RW1S	RW1S	None	RW1S
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	Reserved	SCB_FULL	SCB_NOT_EMPTY	Reserved	SCB_TRIGGER

Receiver interrupt set request register.

Bits	Name	Description
11	SCB_BREAK_DETECT	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
10	SCB_BAUD_DETECT	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
9	SCB_PARITY_ERROR	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
8	SCB_FRAME_ERROR	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0

10.1.47 SCB_INTR_RX_SET (continued)

7	SCB_BLOCKED	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
6	SCB_UNDERFLOW	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
5	SCB_OVERFLOW	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
3	SCB_FULL	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
2	SCB_NOT_EMPTY	Write with 1 to set corresponding bit in interrupt status register. Default: 0x0
0	SCB_TRIGGER	Write with 1 to set corresponding bit in interrupt request register. Default: 0x0

10.1.48 SCB_INTR_RX_MASK

Address: 0x40060FC8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				R	R	R	R
SW Access	None				RW	RW	RW	RW
Bit Name	Reserved[15:12]				SCB_BREAK_DETECT	SCB_BAUD_DETECT	SCB_PARITY_ERROR	SCB_FRAME_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	None	0x0	0x0	None	0x0
HW Access	R	R	R	None	R	R	None	R
SW Access	RW	RW	RW	None	RW	RW	None	RW
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	Reserved	SCB_FULL	SCB_NOT_EMPTY	Reserved	SCB_TRIGGER

Receiver interrupt mask register.

Bits	Name	Description
11	SCB_BREAK_DETECT	Mask bit for corresponding bit in interrupt request register. Default: 0x0
10	SCB_BAUD_DETECT	Mask bit for corresponding bit in interrupt request register. Default: 0x0
9	SCB_PARITY_ERROR	Mask bit for corresponding bit in interrupt request register. Default: 0x0
8	SCB_FRAME_ERROR	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.48 SCB_INTR_RX_MASK (continued)

7	SCB_BLOCKED	Mask bit for corresponding bit in interrupt request register. Default: 0x0
6	SCB_UNDERFLOW	Mask bit for corresponding bit in interrupt request register. Default: 0x0
5	SCB_OVERFLOW	Mask bit for corresponding bit in interrupt request register. Default: 0x0
3	SCB_FULL	Mask bit for corresponding bit in interrupt request register. Default: 0x0
2	SCB_NOT_EMPTY	Mask bit for corresponding bit in interrupt request register. Default: 0x0
0	SCB_TRIGGER	Mask bit for corresponding bit in interrupt request register. Default: 0x0

10.1.49 SCB_INTR_RX_MASKED

Address: 0x40060FCC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				W	W	W	W
SW Access	None				R	R	R	R
Bit Name	Reserved[15:12]				SCB_BREAK_DETECT	SCB_BAUD_DETECT	SCB_PARITY_ERROR	SCB_FRAME_ERROR

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	None	0x0	0x0	None	0x0
HW Access	W	W	W	None	W	W	None	W
SW Access	R	R	R	None	R	R	None	R
Bit Name	SCB_BLOCKED	SCB_UNDERFLOW	SCB_OVERFLOW	Reserved	SCB_FULL	SCB_NOT_EMPTY	Reserved	SCB_TRIGGER

Receiver interrupt masked request register

Bits	Name	Description
11	SCB_BREAK_DETECT	Logical and of corresponding request and mask bits. Default: 0x0
10	SCB_BAUD_DETECT	Logical and of corresponding request and mask bits. Default: 0x0
9	SCB_PARITY_ERROR	Logical and of corresponding request and mask bits. Default: 0x0
8	SCB_FRAME_ERROR	Logical and of corresponding request and mask bits. Default: 0x0

10.1.49 SCB_INTR_RX_MASKED (continued)

7	SCB_BLOCKED	Logical and of corresponding request and mask bits. Default: 0x0
6	SCB_UNDERFLOW	Logical and of corresponding request and mask bits. Default: 0x0
5	SCB_OVERFLOW	Logical and of corresponding request and mask bits. Default: 0x0
3	SCB_FULL	Logical and of corresponding request and mask bits. Default: 0x0
2	SCB_NOT_EMPTY	Logical and of corresponding request and mask bits. Default: 0x0
0	SCB_TRIGGER	Logical and of corresponding request and mask bits. Default: 0x0

11 SFLASH Registers

This section discusses the SFLASH registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

11.1 SFLASH Register Mapping Overview

Register Name	Address
SFLASH_PROT_ROW	0x0FFFF000
SFLASH_PROT_PROTECTION	0x0FFFF07F
SFLASH_AV_PAIRS_8B	0x0FFFF080
SFLASH_AV_PAIRS_32B	0x0FFFF100
SFLASH_CPUSS_WOUNDING	0x0FFFF140
SFLASH_SILICON_ID	0x0FFFF144
SFLASH_CPUSS_PRIV_RAM	0x0FFFF148
SFLASH_CPUSS_PRIV_FLASH	0x0FFFF14C
SFLASH_HIB_KEY_DELAY	0x0FFFF150
SFLASH_DPSLP_KEY_DELAY	0x0FFFF152
SFLASH_GPIO_IOMATRIX	0x0FFFF154
SFLASH_HSIOMG5M_PORT_SEL1	0x0FFFF154
SFLASH_SWD_CONFIG	0x0FFFF154
SFLASH_SWD_LISTEN	0x0FFFF158
SFLASH_FLASH_START	0x0FFFF15C
SFLASH_TSS_RX_CALIBR	0x0FFFF160
SFLASH_CSD_TRIM1_HVIDAC	0x0FFFF160
SFLASH_CSD_TRIM2_HVIDAC	0x0FFFF161
SFLASH_CSD_TRIM1_CSD	0x0FFFF162
SFLASH_CSD_TRIM2_CSD	0x0FFFF163
SFLASH_SAR_TEMP_MULTIPLIER	0x0FFFF164
SFLASH_SAR_TEMP_OFFSET	0x0FFFF166
SFLASH_SKIP_CHECKSUM	0x0FFFF169
SFLASH_PROT_VIRGINKEY	0x0FFFF170
SFLASH_DIE_LOT	0x0FFFF178
SFLASH_DIE_WAFER	0x0FFFF17B

Register Name	Address
SFLASH_DIE_X	0x0FFFF17C
SFLASH_DIE_Y	0x0FFFF17D
SFLASH_DIE_SORT	0x0FFFF17E
SFLASH_DIE_MINOR	0x0FFFF17F
SFLASH_PE_TE_DATA	0x0FFFF180
SFLASH_PP	0x0FFFF1A0
SFLASH_E	0x0FFFF1A4
SFLASH_P	0x0FFFF1A8
SFLASH_EA_E	0x0FFFF1AC
SFLASH_EA_P	0x0FFFF1B0
SFLASH_ES_E	0x0FFFF1B4
SFLASH_ES_P_EO	0x0FFFF1B8
SFLASH_E_VCTAT	0x0FFFF1BC
SFLASH_P_VCTAT	0x0FFFF1BD
SFLASH_MARGIN	0x0FFFF1BE
SFLASH_SPCIF_TRIM1	0x0FFFF1BF
SFLASH_IMO_MAXF0	0x0FFFF1C0
SFLASH_IMO_ABS0	0x0FFFF1C1
SFLASH_IMO_TMPCO0	0x0FFFF1C2
SFLASH_IMO_MAXF1	0x0FFFF1C3
SFLASH_IMO_ABS1	0x0FFFF1C4
SFLASH_IMO_TMPCO1	0x0FFFF1C5
SFLASH_IMO_MAXF2	0x0FFFF1C6
SFLASH_IMO_ABS2	0x0FFFF1C7
SFLASH_IMO_TMPCO2	0x0FFFF1C8
SFLASH_IMO_MAXF3	0x0FFFF1C9
SFLASH_IMO_ABS3	0x0FFFF1CA
SFLASH_IMO_TMPCO3	0x0FFFF1CB
SFLASH_IMO_ABS4	0x0FFFF1CC
SFLASH_IMO_TMPCO4	0x0FFFF1CD
SFLASH_IMO_TRIM	0x0FFFF1D0
SFLASH_CHECKSUM	0x0FFFF1FE
SFLASH_ALT_PROT_ROW	0x0FFFF200
SFLASH_ALT_PP	0x0FFFF3A0
SFLASH_ALT_E	0x0FFFF3A4
SFLASH_ALT_P	0x0FFFF3A8
SFLASH_ALT_EA_E	0x0FFFF3AC
SFLASH_ALT_EA_P	0x0FFFF3B0
SFLASH_ALT_ES_E	0x0FFFF3B4
SFLASH_ALT_ES_P_EO	0x0FFFF3B8

Register Name	Address
SFLASH_ALT_E_VCTAT	0x0FFFF3BC
SFLASH_ALT_P_VCTAT	0x0FFFF3BD
SFLASH_ALT_MARGIN	0x0FFFF3BE
SFLASH_ALT_SPCIF_TRIM2	0x0FFFF3BF

11.1.1 SFLASH_PROT_ROW

Address: 0x0FFFF000

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA8 [7:0]							

Per Page Write Protection

Bits	Name	Description
7 : 0	SFLASH_DATA8	Protection Data (1b per page) Default: 0x00

11.1.2 SFLASH_PROT_PROTECTION

Address: 0x0FFFF07F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	
HW Access	None						None	
SW Access	None						RW	
Bit Name	Reserved[7:2]						SFLASH_PROT_LEVEL [1:0]	

Protection Level

Bits	Name	Description
1 : 0	SFLASH_PROT_LEVEL	Current Protection Mode - note that encoding is different from CPUSS_PROTECTION !! Default: 0x0 **0x1: VIRGIN** 0000: VIRGIN **0x0: OPEN** 0001: OPEN **0x2: PROTECTED** 001X: PROTECTED **0x3: KILL** 01XX: KILL

11.1.3 SFLASH_AV_PAIRS_8B

Address: 0x0FFFF080

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA8 [7:0]							

8b Addr/Value pair Section

Bits	Name	Description
7 : 0	SFLASH_DATA8	Address or Value Byte Default: 0x00

11.1.4 SFLASH_AV_PAIRS_32B

Address: 0x0FFFF100

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

32b Addr/Value pair Section

Bits	Name	Description
31 : 0	SFLASH_DATA32	Address or Value Word Default: 0x00000000

11.1.5 SFLASH_CPUSS_WOUNDING

Address: 0x0FFFF140

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

CPUSS Wounding Register

Bits	Name	Description
31 : 0	SFLASH_DATA32	Data to use for register Default: 0x00000000

11.1.6 SFLASH_SILICON_ID

Address: 0x0FFFF144

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ID [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ID [15: 0]							

Silicon ID

Bits	Name	Description
15 : 0	SFLASH_ID	Silicon ID Default: 0x0000

11.1.7 SFLASH_CPUSS_PRIV_RAM

Address: 0x0FFFF148

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

RAM Privileged Limit

Bits	Name	Description
31 : 0	SFLASH_DATA32	Data to use for register Default: 0x00000000

11.1.8 SFLASH_CPUSS_PRIV_FLASH

Address: 0x0FFFF14C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Flash Privileged Limit

Bits	Name	Description
31 : 0	SFLASH_DATA32	Data to use for register Default: 0x00000000

11.1.9 SFLASH_HIB_KEY_DELAY

Address: 0x0FFFF150

Retention: Retained

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x000	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						SFLASH_WAKEUP_HOLDOFF [9:0]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	SFLASH_WAKEUP_HOLDOFF [9 : 0]							

Hibernate wakeup value for PWR_KEY_DELAY

Bits	Name	Description
9 : 0	SFLASH_WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default: 0x000

11.1.10 SFLASH_DPSLP_KEY_DELAY

Address: 0x0FFFF152

Retention: Retained

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x000	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						SFLASH_WAKEUP_HOLDOFF [9:0]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	SFLASH_WAKEUP_HOLDOFF [9 : 0]							

DeepSleep wakeup value for PWR_KEY_DELAY

Bits	Name	Description
9 : 0	SFLASH_WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default: 0x000

11.1.11 SFLASH_GPIO_IOMATRIX

Address: 0x0FFFF154

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

IO-Matrix Default Setting (TSG4 only)

Bits	Name	Description
31 : 0	SFLASH_DATA32	Data to use for register Default: 0x00000000

11.1.12 SFLASH_HSIOMG5M_PORT_SEL1

Address: 0x0FFFF154

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA32 [31: 0]							

IO-Matrix Default Setting (TSG5-M only)

Bits	Name	Description
31 : 0	SFLASH_DATA32	Data to use for register Default: 0x00000000

11.1.13 SFLASH_SWD_CONFIG

Address: 0x0FFFF154

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None							0x0
HW Access	None							None
SW Access	None							RW
Bit Name	Reserved[7:1]							SFLASH_SWD_SELECT

SWD pinout selector (not present in TSG4/TSG5-M)

Bits	Name	Description
0	SFLASH_SWD_SELECT	0: Use Primary SWD location 1: Use Alternate SWD location Default: 0x0

11.1.14 SFLASH_SWD_LISTEN

Address: 0x0FFFF158

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CYCLES [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CYCLES [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CYCLES [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CYCLES [31: 0]							

Listen Window Length

Bits	Name	Description
31 : 0	SFLASH_CYCLES	Number of clock cycles Default: 0x00000000

11.1.15 SFLASH_FLASH_START

Address: 0x0FFFF15C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ADDRESS [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ADDRESS [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ADDRESS [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_ADDRESS [31: 0]							

Flash Image Start Address

Bits	Name	Description
31 : 0	SFLASH_ADDRESS	Start Address Default: 0x00000000

11.1.16 SFLASH_TSS_RX_CALIBR

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CAL [7:0]							

TSS RX Calibration Data

Bits	Name	Description
7 : 0	SFLASH_CAL	Calibration constant for channel n. Default: 0x00

11.1.17 SFLASH_CSD_TRIM1_HVIDAC

Address: 0x0FFFF160

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TRIM8 [7:0]							

CSD Trim Data for HVIDAC operation

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default: 0x00

11.1.18 SFLASH_CSD_TRIM2_HVIDAC

Address: 0x0FFFF161

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TRIM8 [7:0]							

CSD Trim Data for HVIDAC operation

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default: 0x00

11.1.19 SFLASH_CSD_TRIM1_CSD

Address: 0x0FFFF162

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TRIM8 [7:0]							

CSD Trim Data for (normal) CSD operation

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default: 0x00

11.1.20 SFLASH_CSD_TRIM2_CSD

Address: 0x0FFFF163

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TRIM8 [7:0]							

CSD Trim Data for (normal) CSD operation

Bits	Name	Description
7 : 0	SFLASH_TRIM8	Trim data Default: 0x00

11.1.21 SFLASH_SAR_TEMP_MULTIPLIER

Address: 0x0FFFF164

Retention: Retained

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TEMP_MULTIPLIER [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TEMP_MULTIPLIER [15: 0]							

SAR Temperature Sensor Multiplication Factor

Bits	Name	Description
15 : 0	SFLASH_TEMP_MULTIPLIER	Multiplier value for SAR temperature sensor in fixed point 0.16 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default: 0x0000

11.1.22 SFLASH_SAR_TEMP_OFFSET

Address: 0x0FFFF166

Retention: Retained

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TEMP_OFFSET [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_TEMP_OFFSET [15: 0]							

SAR Temperature Sensor Offset

Bits	Name	Description
15 : 0	SFLASH_TEMP_OFFSET	Offset value for SAR temperature sensor in fixed point 10.6 format. Note: this field exists in products that contain SAR (m0s8sar) only. Default: 0x0000

11.1.23 SFLASH_SKIP_CHECKSUM

Address: 0x0FFFF169

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_SKIP [7:0]							

Checksum Skip Option Register

Bits	Name	Description
7 : 0	SFLASH_SKIP	0: Perform checksum check (see CHECKSUM fueld below) 1: Skip checksum check gt;1: Undefined - do not use Default: 0x00

11.1.24 SFLASH_PROT_VIRGINKEY

Address: 0x0FFFF170

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_KEY8 [7:0]							

Virgin Protection Mode Key

Bits	Name	Description
7 : 0	SFLASH_KEY8	Key Byte Default: 0x00

11.1.25 SFLASH_DIE_LOT

Address: 0x0FFFF178

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_LOT [7:0]							

Lot Number (3 bytes)

Bits	Name	Description
7 : 0	SFLASH_LOT	Lot Number Byte Default: 0x00

11.1.26 SFLASH_DIE_WAFER

Address: 0x0FFFF17B

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_WAFER [7:0]							

Wafer Number

Bits	Name	Description
7 : 0	SFLASH_WAFER	Wafer Number Default: 0x00

11.1.27 SFLASH_DIE_X

Address: 0x0FFFF17C

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x00					
HW Access	None		None					
SW Access	RW		RW					
Bit Name	SFLASH_CRI_PASS [7:6]		SFLASH_X [5:0]					

X Position on Wafer, CRI Pass/Fail Bin

Bits	Name	Description
7 : 6	SFLASH_CRI_PASS	CRI Pass Bin (1-3) or 0 (Fail Bin) Default: 0x0
5 : 0	SFLASH_X	X Position Default: 0x00

11.1.28 SFLASH_DIE_Y

Address: 0x0FFFF17D

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x00					
HW Access	None		None					
SW Access	RW		RW					
Bit Name	SFLASH_CHI_PASS [7:6]		SFLASH_Y [5:0]					

Y Position on Wafer, CHI Pass/Fail Bin

Bits	Name	Description
7 : 6	SFLASH_CHI_PASS	CHI Pass Bin (1-3) or 0 (Fail Bin) Default: 0x0
5 : 0	SFLASH_Y	Y Position Default: 0x00

11.1.29 SFLASH_DIE_SORT

Address: 0x0FFFF17E

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0		0x0		0x0	
HW Access	None		None		None		None	
SW Access	None		RW		RW		RW	
Bit Name	Reserved[7:6]		SFLASH_S3_PASS [5:4]		SFLASH_S2_PASS [3:2]		SFLASH_S1_PASS [1:0]	

Sort1/2/3 Pass/Fail Bin

Bits	Name	Description
5 : 4	SFLASH_S3_PASS	SORT3 Pass Bin (1-3) or 0 (Fail Bin) Default: 0x0
3 : 2	SFLASH_S2_PASS	SORT2 Pass Bin (1-3) or 0 (Fail Bin) Default: 0x0
1 : 0	SFLASH_S1_PASS	SORT1 Pass Bin (1-3) or 0 (Fail Bin) Default: 0x0

11.1.30 SFLASH_DIE_MINOR

Address: 0x0FFFF17F

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_MINOR [7:0]							

Minor Revision Number

Bits	Name	Description
7 : 0	SFLASH_MINOR	Minor revision number Default: 0x00

11.1.31 SFLASH_PE_TE_DATA

Address: 0x0FFFF180

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA8 [7:0]							

PE/TE Data

Bits	Name	Description
7 : 0	SFLASH_DATA8	PE/TE Data Default: 0x00

11.1.32 SFLASH_PP

Address: 0x0FFFF1A0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Preprogram Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.33 SFLASH_E

Address: 0x0FFFF1A4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.34 SFLASH_P

Address: 0x0FFFF1A8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Program Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.35 SFLASH_EA_E

Address: 0x0FFFF1AC

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase All - Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.36 SFLASH_EA_P

Address: 0x0FFFF1B0

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase All - Program Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.37 SFLASH_ES_E

Address: 0x0FFFF1B4

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Sector - Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.38 SFLASH_ES_P_EO

Address: 0x0FFFF1B8

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0				0x0			
HW Access	None				None			
SW Access	RW				RW			
Bit Name	SFLASH_NDAC [31:28]				SFLASH_PDAC [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23:0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Sector - Program EO Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.39 SFLASH_E_VCTAT

Address: 0x0FFFF1BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0		0x0			
HW Access	None	None	None		None			
SW Access	None	RW	RW		RW			
Bit Name	Reserved	SFLASH_VCTAT_ENABLE	SFLASH_VCTAT_VOLTAGE [5:4]		SFLASH_VCTAT_SLOPE [3:0]			

Bandgap Trim Register

Bits	Name	Description
6	SFLASH_VCTAT_ENABLE	Enable VCTAT block Default: 0x0
5 : 4	SFLASH_VCTAT_VOLTAGE	Output voltage absolute trim Default: 0x0
3 : 0	SFLASH_VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default: 0x0

11.1.40 SFLASH_P_VCTAT

Address: 0x0FFFF1BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0		0x0			
HW Access	None	None	None		None			
SW Access	None	RW	RW		RW			
Bit Name	Reserved	SFLASH_VCTAT_ENABLE	SFLASH_VCTAT_VOLTAGE [5:4]		SFLASH_VCTAT_SLOPE [3:0]			

Bandgap Trim Register

Bits	Name	Description
6	SFLASH_VCTAT_ENABLE	Enable VCTAT block Default: 0x0
5 : 4	SFLASH_VCTAT_VOLTAGE	Output voltage absolute trim Default: 0x0
3 : 0	SFLASH_VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default: 0x0

11.1.41 SFLASH_MARGIN

Address: 0x0FFFF1BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_MDAC [7:0]							

Margin DAC Control Register

Bits	Name	Description
7 : 0	SFLASH_MDAC	Margin DAC input. Each increment increases the VMARG by ~15.6mV Default: 0x00

11.1.42 SFLASH_SPCIF_TRIM1

Address: 0x0FFFF1BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				None			
SW Access	None				RW			
Bit Name	Reserved[7:4]				SFLASH_BDAC [3:0]			

BDAC control register

Bits	Name	Description
3 : 0	SFLASH_BDAC	BDAC flash input. Trims flash bitline program inhibit voltage. Each increment causes an increase of 0.12V (0V-1.8V) Default: 0x0

11.1.43 SFLASH_IMO_MAXF0

Address: 0x0FFFF1C0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_MAXFREQ [5:0]					

Max frequency for trim pair

Bits	Name	Description
5 : 0	SFLASH_MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default: 0x00

11.1.44 SFLASH_IMO_ABS0

Address: 0x0FFFF1C1

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_ABS_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x00

11.1.45 SFLASH_IMO_TMPCO0

Address: 0x0FFFF1C2

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_TMPCO_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x00

11.1.46 SFLASH_IMO_MAXF1

Address: 0x0FFFF1C3

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_MAXFREQ [5:0]					

Max frequency for trim pair

Bits	Name	Description
5 : 0	SFLASH_MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default: 0x00

11.1.47 SFLASH_IMO_ABS1

Address: 0x0FFFF1C4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_ABS_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x00

11.1.48 SFLASH_IMO_TMPCO1

Address: 0x0FFFF1C5

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_TMPCO_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x00

11.1.49 SFLASH_IMO_MAXF2

Address: 0x0FFFF1C6

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_MAXFREQ [5:0]					

Max frequency for trim pair

Bits	Name	Description
5 : 0	SFLASH_MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default: 0x00

11.1.50 SFLASH_IMO_ABS2

Address: 0x0FFFF1C7

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_ABS_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x00

11.1.51 SFLASH_IMO_TMPCO2

Address: 0x0FFFF1C8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_TMPCO_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x00

11.1.52 SFLASH_IMO_MAXF3

Address: 0x0FFFF1C9

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_MAXFREQ [5:0]					

Max frequency for trim pair

Bits	Name	Description
5 : 0	SFLASH_MAXFREQ	Max frequency (3..48) at which IMO_ABS/TMPCO3 is valid (range is IMO_MAXF2+1 .. IMO_MAXF3). Default: 0x00

11.1.53 SFLASH_IMO_ABS3

Address: 0x0FFFF1CA

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_ABS_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x00

11.1.54 SFLASH_IMO_TMPCO3

Address: 0x0FFFF1CB

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_TMPCO_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x00

11.1.55 SFLASH_IMO_ABS4

Address: 0x0FFFF1CC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_ABS_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM4 (ICTAT trim for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x00

11.1.56 SFLASH_IMO_TMPCO4

Address: 0x0FFFF1CD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		None					
SW Access	None		RW					
Bit Name	Reserved[7:6]		SFLASH_TMPCO_TRIM_IMO [5:0]					

Value for PWR_BG_TRIM5 (ICTAT tempco for IMO current reference).

Bits	Name	Description
5 : 0	SFLASH_TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x00

11.1.57 SFLASH_IMO_TRIM

Address: 0x0FFFF1D0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_OFFSET [7:0]							

IMO Trim Register

Bits	Name	Description
7 : 0	SFLASH_OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. Default: 0x00

11.1.58 SFLASH_CHECKSUM

Address: 0x0FFFF1FE

Retention: Retained

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CHECKSUM [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_CHECKSUM [15: 0]							

Boot Checksum

Bits	Name	Description
15 : 0	SFLASH_CHECKSUM	Checksum of fixed data checked during boot. This checksum covers all of rows 1,2,3 of macro 0 + row 3 of macro 1 (except this checksum, and row 3 of macro 1 only if it exists). Default: 0x0000

11.1.59 SFLASH_ALT_PROT_ROW

Address: 0x0FFFF200

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_DATA8 [7:0]							

Per Page Write Protection

Bits	Name	Description
7 : 0	SFLASH_DATA8	Protection Data (1b per page) Default: 0x00

11.1.60 SFLASH_ALT_PP

Address: 0x0FFFF3A0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Preprogram Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.61 SFLASH_ALT_E

Address: 0x0FFFF3A4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.62 SFLASH_ALT_P

Address: 0x0FFFF3A8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Program Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.63 SFLASH_ALT_EA_E

Address: 0x0FFFF3AC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase All - Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.64 SFLASH_ALT_EA_P

Address: 0x0FFFF3B0

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase All - Program Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.65 SFLASH_ALT_ES_E

Address: 0x0FFFF3B4

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Sector - Erase Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.66 SFLASH_ALT_ES_P_EO

Address: 0x0FFFF3B8

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000000							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_PERIOD [23: 0]							

Erase Sector - Program EO Settings

Bits	Name	Description
31 : 28	SFLASH_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
27 : 24	SFLASH_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0
23 : 0	SFLASH_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x000000

11.1.67 SFLASH_ALT_E_VCTAT

Address: 0x0FFFF3BC

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0		0x0			
HW Access	None	None	None		None			
SW Access	None	RW	RW		RW			
Bit Name	Reserved	SFLASH_VCTAT_ENABLE	SFLASH_VCTAT_VOLTAGE [5:4]		SFLASH_VCTAT_SLOPE [3:0]			

Bandgap Trim Register

Bits	Name	Description
6	SFLASH_VCTAT_ENABLE	Enable VCTAT block Default: 0x0
5 : 4	SFLASH_VCTAT_VOLTAGE	Output voltage absolute trim Default: 0x0
3 : 0	SFLASH_VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default: 0x0

11.1.68 SFLASH_ALT_P_VCTAT

Address: 0x0FFFF3BD

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x0	0x0		0x0			
HW Access	None	None	None		None			
SW Access	None	RW	RW		RW			
Bit Name	Reserved	SFLASH_VCTAT_ENABLE	SFLASH_VCTAT_VOLTAGE [5:4]		SFLASH_VCTAT_SLOPE [3:0]			

Bandgap Trim Register

Bits	Name	Description
6	SFLASH_VCTAT_ENABLE	Enable VCTAT block Default: 0x0
5 : 4	SFLASH_VCTAT_VOLTAGE	Output voltage absolute trim Default: 0x0
3 : 0	SFLASH_VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default: 0x0

11.1.69 SFLASH_ALT_MARGIN

Address: 0x0FFFF3BE

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	SFLASH_MDAC [7:0]							

Margin DAC Control Register

Bits	Name	Description
7 : 0	SFLASH_MDAC	Margin DAC input. Each increment increases the VMARG by ~15.6mV Default: 0x00

11.1.70 SFLASH_ALT_SPCIF_TRIM2

Address: 0x0FFFF3BF

Retention: Retained

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0			0x00				
HW Access	None			None				
SW Access	RW			RW				
Bit Name	SFLASH_SLOPE [7:5]			SFLASH_IDAC [4:0]				

Second Flash Trim Registers

Bits	Name	Description
7 : 5	SFLASH_SLOPE	Trim DAC for trimming SA current ref. PTAT slope (nA/C). Note: This field applies to the first Flash macro only. Trim values for other flash macros are stored in supervisory row data (of the first macro). Default: 0x0
4 : 0	SFLASH_IDAC	To control base SA Reference Current in ~0.6A increments (50C): Lower settings for BL leakage. Note: This field applies to the first Flash macro only. Trim values for other flash macros are stored in supervisory row data (of the first macro). Default: 0x00

12 SPCIF Registers

This section discusses the SPCIF registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

12.1 SPCIF Register Mapping Overview

Register Name	Address
SPCIF_GEOMETRY	0x400E0000
SPCIF_ADDRESS	0x400E0004
SPCIF_TIMER	0x400E0008
SPCIF_FLASH_CONTROL	0x400E000C
SPCIF_FLASH_WR_DATA	0x400E0010
SPCIF_NVL_CONTROL	0x400E0014
SPCIF_NVL_RD_DATA	0x400E0018
SPCIF_NVL_WR_DATA	0x400E001C
SPCIF_DFT	0x400E0020
SPCIF_MDAC	0x400E0024
SPCIF_BOOKMARK	0x400E0028
SPCIF_PNDAC	0x400E002C
SPCIF_TRIM1	0x400EFF00
SPCIF_TRIM2	0x400EFF04

12.1.1 SPCIF_GEOMETRY

Address: 0x400E0000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x08						
HW Access	R	R						
SW Access	RW	R						
Bit Name	SPCIF_DE_CPD_LP	SPCIF_NVL [30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	0x1		0x1		0x2			
HW Access	R		R		R			
SW Access	R		R		R			
Bit Name	SPCIF_FLASH_ROW [23:22]		SPCIF_NUM_FLASH [21:20]		SPCIF_SFLASH [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0080							
HW Access	R							
SW Access	R							
Bit Name	SPCIF_FLASH [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0080							
HW Access	R							
SW Access	R							
Bit Name	SPCIF_FLASH [15: 0]							

Flash/NVL geometry information

Bits	Name	Description
31	SPCIF_DE_CPD_LP	0: SRAM busy wait loop has not been copied. 1: Busy wait loop has been written into SRAM. Default: 0x0
30 : 24	SPCIF_NVL	NVL Size in bytes Default: 0x08
23 : 22	SPCIF_FLASH_ROW	Flash row size in 128B units Default: 0x1
21 : 20	SPCIF_NUM_FLASH	Number of flash arrays Default: 0x1

12.1.1 SPCIF_GEOMETRY (continued)

19 : 16	SPCIF_SFLASH	Supervisory Flash Size in 256B segments Default: 0x2
15 : 0	SPCIF_FLASH	Flash size in 256B segments Default: 0x0080

12.1.2 SPCIF_ADDRESS

Address: 0x400E0004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None				0x0	0x0	0x000	
HW Access	None				R	R	R	
SW Access	None				RW	RW	RW	
Bit Name	Reserved[31:28]				SPCIF_ALL_FLSH_SELECT	SPCIF_AXA	SPCIF_ROW_ADDR [25:16]	

Bits	23	22	21	20	19	18	17	16
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_ROW_ADDR [25: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[15:9]							SPCIF_INC

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	RW							
Bit Name	SPCIF_WR_ADDR [7:0]							

Flash/NVL Address Register

Bits	Name	Description
27	SPCIF_ALL_FLSH_SELECT	0: Normal operation 1: When multiple flash macros are present, select all of them instead of the one indicated by ROW_ADDR. Default: 0x0
26	SPCIF_AXA	Indicates whether address pertains to regular or supervisory Flash rows. This bit has no effect on NVL operations. Default: 0x0 **0x0: REGULAR** ROW_ADDR is a row address in the regular flash array area

12.1.2 SPCIF_ADDRESS (continued)

		0x1: SUPERVISORY ROW_ADDR is a row address in the supervisory array area
25 : 16	SPCIF_ROW_ADDR	Flash row address for program/erase operations. Supports up to 256KB of flash on a chip. Unused MSB bits are ignored. Default: 0x000
8	SPCIF_INC	0: Dont change WR_ADDR after a write to SPCIF_FLASH_WR_DATA 1: Increment WR_ADDR after each write to SPCIF_FLASH_WR_DATA Default: 0x0
7 : 0	SPCIF_WR_ADDR	Flash: indicates the byte address for writes to the page/row latch. NVL: for read/write operations, indicates the byte address in the NVL array. Unused MSB bits are ignored. Default: 0x00

12.1.3 SPCIF_TIMER

Address: 0x400E0008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_PERIOD [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_PERIOD [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_PERIOD [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_PERIOD [31: 0]							

SPCIF Timer Register

Bits	Name	Description
31 : 0	SPCIF_PERIOD	Period of timer (in units of 36 MHz IMO clock periods). Default: 0x00000000

12.1.4 SPCIF_FLASH_CONTROL

Address: 0x400E000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None	0x0	0x0	0x0	0x0		0x0	0x0
HW Access	None	R	RW1S	R	R		RW0C	R
SW Access	None	RW	RW1C	RW	RW		RW1S	RW
Bit Name	Reserved	SPCIF_NO_READS	SPCIF_INTR_REQ	SPCIF_INTR_EN	SPCIF_PE_SELECT [11:10]		SPCIF_START_COUNT	SPCIF_PE_OVERRIDE

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0		0x0			
HW Access	R	RW	R		R			
SW Access	RW	RW	RW		RW			
Bit Name	SPCIF_PE_ENABLE	SPCIF_ACLK_EN	SPCIF_SEQ [5:4]		SPCIF_MODE [3:0]			

Flash Control Register

Bits	Name	Description
14	SPCIF_NO_READS	Firmware sets this bit to block read accelerator from issueing more requests to flash. When set Flash Accelerator will return HRESP=1 on any read requests. Firmware must ensure no read accesses are pending or must not take control of the Flash immediately with setting this bit. Default: 0x0
13	SPCIF_INTR_REQ	Interrupt request. Hardware asserts this bit when counter expires (if INTR_EN = 1) and firmware clears when interrupt handled. Default: 0x0
12	SPCIF_INTR_EN	Timer interrupt enable. When this bit is set, the SPCIF generates an interrupt when timer expires. Default: 0x0

12.1.4 SPCIF_FLASH_CONTROL (continued)

11 : 10	SPCIF_PE_SELECT	Selects which of the 3 pump enable outputs to drive with the signal driven from the PE_ENABLE and PE_OVERRIDE bits. (3: Reserved) Default: 0x0 **0x0: FLASH** Drive Flash PE **0x1: NVL** Drive NVL PE **0x2: TEST** Drive test PE
9	SPCIF_START_COUNT	This bit should be enabled so that the timer can start counting down. This bit is cleared by hardware when counter period expires. Initial count value set in SPCIF_TIMER register. Default: 0x0
8	SPCIF_PE_OVERRIDE	Manual override for pump enables: 0: Pumps operate normally (per PE_ENABLE) 1: Pumps are enabled as long as this bit is set Default: 0x0
7	SPCIF_PE_ENABLE	Configures the timer to assert the PE output while the timer is active: 0: Pumps off 1: Pumps on while timer is counting Default: 0x0
6	SPCIF_ACLK_EN	Enables a single cycle high time of the Aclk to the Flash. Default: 0x0
5 : 4	SPCIF_SEQ	Flash Seq input, see BROS for details on values. Default: 0x0
3 : 0	SPCIF_MODE	Flash Mode input. (5-8: Not used.) Default: 0x0 **0x0: NORMAL_READ** Normal mode, read array enabled **0x1: SET_PRE_PGM** Set pre-program (PEP/EPP) bit for soft pre-program **0x2: PAGE_WR_ALL** Set page write all for filling page buffer with a single byte write **0x3: PSEUDO_IDLE** Pseudo Idle mode. **0x4: CLEAR_HVPL** Clear HVPL **0x9: ERASE_BULK** Erase bulk all rows

12.1.4 SPCIF_FLASH_CONTROL (continued)

0xA: ERASE_SECTOR
Erase sector, each sector is 64 rows

0xB: ERASE_PAGE
Erase selected page in flash

0xC: PGM_BULK
Program bulk all rows â to support Microwire spec.

0xD: PGM_BULK_EVENODD
Program bulk even/odd rows, ra[0] -gt; even/odd row

0xE: PGM_SECTOR_EVENODD
Program sector - ra[0] -gt; even/odd rows, each sector is 64 rows

0xF: PGM_PAGE
Program selected page in flash

12.1.5 SPCIF_FLASH_WR_DATA

Address: 0x400E0010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_DATA [7:0]							

Flash Write Data Register

Bits	Name	Description
7 : 0	SPCIF_DATA	Data byte for HV Page/Row Latch Default: 0x00

12.1.6 SPCIF_NVL_CONTROL

Address: 0x400E0014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x0	0x0	0x0	0x0	0x0	
HW Access	None		R	R	R	R	R	
SW Access	None		RW	RW	RW	RW	RW	
Bit Name	Reserved[15:14]		SPCIF_TEST_VLOADX	SPCIF_TEST_TSLOW	SPCIF_TEST_TFAST	SPCIF_TEST_EN	SPCIF_MARG_SEL [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	0x0	0x0	0x0	0x0
HW Access	None			R	R	R	R	R
SW Access	None			RW	RW	RW	RW	RW
Bit Name	Reserved[7:5]			SPCIF_ERASE	SPCIF_PROGRAM	SPCIF_READ	SPCIF_WRITE	SPCIF_LOAD

NVL Control Register

Bits	Name	Description
13	SPCIF_TEST_VLOADX	Enables vloadx test mode in the NVL Default: 0x0
12	SPCIF_TEST_TSLOW	Enables slow recall timing test mode in the NVL Default: 0x0
11	SPCIF_TEST_TFAST	Enables fast recall timing test mode in the NVL Default: 0x0
10	SPCIF_TEST_EN	Enables margin test mode for the NVL Default: 0x0

12.1.6 SPCIF_NVL_CONTROL (continued)

9 : 8	SPCIF_MARG_SEL	These bits directly select the voltages that connect to the NVL test_p test_n inputs for margin mode reads. Only pertinent if NVL Test Mode Enable (TEST_EN) = 1. Do not set this to any value other than 2âb00 unless the NVL Test Mode Enable bit is already set. Default: 0x0 **0x0: HIZ_HIZ** test_p=HiZ, test_n=HiZ **0x1: GND_GND** test_p=vgnd, test_n=vgnd **0x2: MRG_GND** test_p=vmarg_aux, test_n=vgnd **0x3: GND_MRG** test_p=vgnd, test_n=vmarg_aux
4	SPCIF_ERASE	When high sets the NVL mode to erase the nonvolatile cell. Default: 0x0
3	SPCIF_PROGRAM	When high sets the NVL mode to program the nonvolatile cell Default: 0x0
2	SPCIF_READ	When high reads the voltaile data from NVL Default: 0x0
1	SPCIF_WRITE	When high writes data into volatile portion of NVL Default: 0x0
0	SPCIF_LOAD	When high moves the data from non-volatile portion to volatile portion of NVL. Default: 0x0

12.1.7 SPCIF_NVL_RD_DATA

Address: 0x400E0018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	R							
Bit Name	SPCIF_DATA [7:0]							

NVL Read Data Register

Bits	Name	Description
7 : 0	SPCIF_DATA	Data read from NVL array Default: 0xFF

12.1.8 SPCIF_NVL_WR_DATA

Address: 0x400E001C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_DATA [7:0]							

NVL Write Data Register

Bits	Name	Description
7 : 0	SPCIF_DATA	Data to be written to NVL array Default: 0x00

12.1.9 SPCIF_DFT

Address: 0x400E0020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	SPCIF_PARAM_LOC	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	RW	R
SW Access	RW	RW	RW	RW	RW	RW	R	RW
Bit Name	SPCIF_EN_TP2	SPCIF_EN_TP1	SPCIF_TM_ITIM	SPCIF_TM_IREF_EXTRM	SPCIF_TM_ISA	SPCIF_TM_VDAC_FORCE	SPCIF_TM_XYOUT	SPCIF_TM_XYDEC

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x00					
HW Access	R	R	R					
SW Access	RW	RW	RW					
Bit Name	SPCIF_TM_SADC	SPCIF_TM_RDSTRB	SPCIF_TM_DAA_SEL [13:8]					

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0		
HW Access	R	R	R	R	R	R		
SW Access	RW	RW	RW	RW	RW	RW		
Bit Name	SPCIF_TM_DAA	SPCIF_TM_ENCOL	SPCIF_TM_DISROW	SPCIF_TM_RDHVPL	SPCIF_PNB	SPCIF_TM [2:0]		

Flash Test Mode Register

Bits	Name	Description
31	SPCIF_PARAM_LOC	Remaps parameters used by the SROM from being mapped in the flash hidden row to the SRAM instead. Default: 0x0
23	SPCIF_EN_TP2	Enables connection of Flash TP2 pad to analog route Default: 0x0

12.1.9 SPCIF_DFT (continued)

22	SPCIF_EN_TP1	Enables connection of Flash TP1 pad to analog route Default: 0x0
21	SPCIF_TM_ITIM	1: Enables sense amp timing current test mode Default: 0x0
20	SPCIF_TM_IREF_EXTRM	1: Places IREFM into Extreme Timing mode Default: 0x0
19	SPCIF_TM_ISA	1: Isaref current input is used as sense amp reference Default: 0x0
18	SPCIF_TM_VDAC_FORCE	Gates the analog voltage outputs of the VDAC circuit. Default: 0x0 **0x0: VMARG** VMARG output is valid, VMARG_AUX is Hi-Z. **0x1: VMARG_AUX** VMARG output is Hi-Z, VMARG_AUX is valid.
17	SPCIF_TM_XYOUT	When Tm_xydec = 1, if one and only one WL or Y select address is on, this signal is asserted. Default: 0x0
16	SPCIF_TM_XYDEC	1: Addressed WL or Y select signal with Mode[0] reads are checked. If one and only one WL or Y select address is on, then a â1â is output on xy_out. WL and Y select checked simultaneously. Default: 0x0
15	SPCIF_TM_SADC	1: Places sense amp into DC mode to sense low current on BL. Relax timing. Default: 0x0
14	SPCIF_TM_RDSTRB	1: Accessed bit line is connected to vpwr to accelerate read disturb Default: 0x0
13 : 8	SPCIF_TM_DAA_SEL	Selects 1 of the bits on the data output of the FM array to drive to the muxbus to use for current voltage measurements. Default: 0x00
7	SPCIF_TM_DAA	Direct Memory Access enable for Flash Default: 0x0
6	SPCIF_TM_ENCOL	1: Enables all columns, not connected to ground Default: 0x0
5	SPCIF_TM_DISROW	1: Disable all rows to check for column leakage Default: 0x0
4	SPCIF_TM_RDHVPL	1: Enable HV Page Latch read out Default: 0x0
3	SPCIF_PNB	Positive/Negative Margin Voltage select. Default: 0x0 **0x0: VNEG** Use Vneg **0x1: VPOS** Use Vpos
2 : 0	SPCIF_TM	Flash Test Mode Select, see BROS for details on each value. Default: 0x0

12.1.10 SPCIF_MDAC

Address: 0x400E0024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_MDAC [7:0]							

Margin DAC Control Register

Bits	Name	Description
7 : 0	SPCIF_MDAC	Margin DAC input. Each increment increases the VMARG by ~15.6mV Default: 0x00

12.1.11 SPCIF_BOOKMARK

Address: 0x400E0028

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_BOOKMARK [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_BOOKMARK [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_BOOKMARK [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	SPCIF_BOOKMARK [31: 0]							

Bookmark Pointer Register

Bits	Name	Description
31 : 0	SPCIF_BOOKMARK	SROM Bookmark Default: 0x00000000

12.1.12 SPCIF_PNDAC

Address: 0x400E002C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	SPCIF_NDAC [7:4]				SPCIF_PDAC [3:0]			

PDAC/NDAC Settings

Bits	Name	Description
7 : 4	SPCIF_NDAC	NDAC input. Each increment in NDAC causes an increase of ~0.10V in VNEG Default: 0x0
3 : 0	SPCIF_PDAC	PDAC input. Each increment in PDAC causes an increase of ~0.10V in VPOS Default: 0x0

12.1.13 SPCIF_TRIM1

Address: 0x400EFF00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				SPCIF_BDAC [3:0]			

SPC Trim Register

Bits	Name	Description
3 : 0	SPCIF_BDAC	BDAC flash input. Trims flash bitline program inhibit voltage. Each increment causes an increase of 0.12V (0V-1.8V) Default: 0x0

12.1.14 SPCIF_TRIM2

Address: 0x400EFF04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0			0x00				
HW Access	R			R				
SW Access	RW			RW				
Bit Name	SPCIF_SLOPE [7:5]			SPCIF_IDAC [4:0]				

Second Flash Trim Registers

Bits	Name	Description
7 : 5	SPCIF_SLOPE	Trim DAC for trimming SA current ref. PTAT slope (nA/C). Note: This field applies to the first Flash macro only. Trim values for other flash macros are stored in supervisory row data (of the first macro). Default: 0x0
4 : 0	SPCIF_IDAC	To control base SA Reference Current in ~0.6A increments (50C): Lower settings for BL leakage. Note: This field applies to the first Flash macro only. Trim values for other flash macros are stored in supervisory row data (of the first macro). Default: 0x00

13 SRSS Registers

This section discusses the SRSS registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

13.1 SRSS Register Mapping Overview

Register Name	Address
PWR_CONTROL	0x400B0000
PWR_INTR	0x400B0004
PWR_INTR_MASK	0x400B0008
PWR_KEY_DELAY	0x400B000C
PWR_PWRSYS_CONFIG	0x400B0010
PWR_BG_CONFIG	0x400B0014
PWR_VMON_CONFIG	0x400B0018
PWR_DFT_SELECT	0x400B001C
PWR_DDFT_SELECT	0x400B0020
PWR_DFT_KEY	0x400B0024
PWR_BOD_KEY	0x400B0028
PWR_STOP	0x400B002C
CLK_SELECT	0x400B0100
CLK_ILO_CONFIG	0x400B0104
CLK_IMO_CONFIG	0x400B0108
CLK_IMO_SPREAD	0x400B010C
CLK_DFT_SELECT	0x400B0110
WDT_CTRLOW	0x400B0200
WDT_CTRHIGH	0x400B0204
WDT_MATCH	0x400B0208
WDT_CONFIG	0x400B020C
WDT_CONTROL	0x400B0210
RES_CAUSE	0x400B0300
RES_DFT_SELECT	0x400B0304
PWR_PWRSYS_TRIM1	0x400BFF00
PWR_PWRSYS_TRIM2	0x400BFF04

Register Name	Address
PWR_PWRSYS_TRIM3	0x400BFF08
PWR_PWRSYS_TRIM4	0x400BFF0C
PWR_BG_TRIM1	0x400BFF10
PWR_BG_TRIM2	0x400BFF14
PWR_BG_TRIM3	0x400BFF18
PWR_BG_TRIM4	0x400BFF1C
PWR_BG_TRIM5	0x400BFF20
CLK_ILO_TRIM	0x400BFF24
CLK_IMO_TRIM1	0x400BFF28
CLK_IMO_TRIM2	0x400BFF2C
CLK_IMO_TRIM3	0x400BFF30
CLK_IMO_TRIM4	0x400BFF34
PWR_RSVD_TRIM	0x400BFF38

13.1.1 PWR_CONTROL

Address: 0x400B0000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x1	None	0x0	0x0	0x0	None	0x0	0x1
HW Access	R	None	R	R	None	None	RW0C	R
SW Access	RW	None	RW	RW1S	RW	None	RW1S	RW
Bit Name	HIBER-NATE	Reserved	LFCLK_SHORT	HIBERNATE_DISABLE	FIMO_DISABLE	Reserved	HVMON_RELOAD	HVMON_ENABLE

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	EXT_VCCD	Reserved[22:16]						

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0	0x0	0x0			
HW Access	None		RW	RW	RW			
SW Access	None		R	R	R			
Bit Name	Reserved[7:6]		LPM_READY	DEBUG_SESSION	POWER_MODE [3:0]			

Power Mode Control

Bits	Name	Description
31	HIBERNATE	Selects between HIBERNATE/DEEPSLEEP modes when Cortex-M0 enters low power mode (SleepDeep). Note: this bit is ignored when HIBERNATE_DISABLE=1. Default: 0x1 **0x0: DEEP_SLEEP** Enter DeepSleep mode when CPU asserts SLEEPDEEP signal **0x1: HIBERNATE** Enter Hibernate mode when CPU asserts SLEEPDEEP signal

13.1.1 PWR_CONTROL (continued)

29	LFCLK_SHORT	Short Vcclfclk and Vccdpslp power rails in DeepSleep power mode. This mode selection affects the accuracy specifications of the ILO oscillator due to supply noise. See Data Sheet for more details. 0: Do not short power domains 1: Short power domains Default: 0x0
28	HIBERNATE_DISABLE	0: Normal operation, HIBERNATE works as described 1: HIBERNATE bit is ignored, Hibernate mode is permanently disabled (part will go to DeepSleep instead. Note: This bit is a write-once bit until the next reset. Default: 0x0
27	FIMO_DISABLE	This bit is asserted during the boot process 0: Forces IMO to operate at 12MHz, ignore its frequency and trim settings and operate independent on its external references. 1: Turns IMO into normal operational mode Default: 0x0
25	HVMON_RELOAD	Firmware writes 1 to reload HV State in hibernate shadow copy. Hardware clears this bit after reload was successful. Wait at least 9 cycles after writing/recalling NVL before reloading the HVMON. Default: 0x0
24	HVMON_ENABLE	0: HV State Monitoring is disabled 1: HV State Monitoring is automatically enable by sleep controller Default: 0x1
23	EXT_VCCD	Indicates that Vccd is provided externally (on Vccd pin). Setting this bit turns off the active regulator and will lead to system reset (PBOD) unless both Vddd and Vccd pins are supplied externally. Default: 0x0
5	LPM_READY	Indicates whether the low power mode regulators are ready to enter DEEPSLEEP or HIBERNATE mode. 0: If DEEPSLEEP or HIBERNATE mode is requested, device will enter SLEEP mode. When low power regulators are ready, device will automatically enter the originally requested mode. 1: Normal operation. DEEPSLEEP and HIBERNATE work as described. Default: 0x0
4	DEBUG_SESSION	Indicates whether a debug session is active (CDBGPWRUPREQ signal is 1) Default: 0x0 **0x0: NO_SESSION** No debug session active **0x1: SESSION_ACTIVE** Debug session is active
3 : 0	POWER_MODE	Current power mode of the device. Note that this field cannot be read in all power modes on actual silicon. Default: 0x0 **0x0: RESET** RESET state **0x1: ACTIVE** ACTIVE state

13.1.1 PWR_CONTROL (continued)

0x2: SLEEP
SLEEP state

0x3: DEEP_SLEEP
DEEP_SLEEP state

0x4: HIBERNATE
HIBERNATE state

13.1.2 PWR_INTR

Address: 0x400B0004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	None
HW Access	None						None	None
SW Access	None						RW1C	None
Bit Name	Reserved[7:2]						LVD	Reserved

Power System Interrupt Register

Bits	Name	Description
1	LVD	Indicates an Low Voltage Detect interrupt Default: 0x0

13.1.3 PWR_INTR_MASK

Address: 0x400B0008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None						0x0	None
HW Access	None						R	None
SW Access	None						RW	None
Bit Name	Reserved[7:2]						LVD	Reserved

Power System Interrupt Mask Register

Bits	Name	Description
1	LVD	1: Propagate interrupt to CPU Default: 0x0

13.1.4 PWR_KEY_DELAY

Address: 0x400B000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x000	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						WAKEUP_HOLDOFF [9:0]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x000							
HW Access	R							
SW Access	RW							
Bit Name	WAKEUP_HOLDOFF [9 : 0]							

Power System KeyDelay Register

Bits	Name	Description
9 : 0	WAKEUP_HOLDOFF	Delay (in 12MHz IMO clock cycles) to wait for references to settle on wakeup from hibernate/ deepsleep. PBOD is ignored and system does not resume until this delay expires. Note that the same delay on POR is hard-coded. Default: 0x30C

13.1.5 PWR_PWRSYS_CONFIG

Address: 0x400B0010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x1	0x0
HW Access	None						R	R
SW Access	None						RW	RW
Bit Name	Reserved[15:10]						HIB_TEST_REP	HIB_TEST_EN

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

Power System Trim and Configuration

Bits	Name	Description
9	HIB_TEST_REP	When set the enhanced replica load regulation circuit is enabled. When clear, the enhancments are disabled at the cost of higher current. (engineering only) Default: 0x1
8	HIB_TEST_EN	Bias control for the DSBOD/HBOD. (engineering only) 0: low power biasing 1: turbo biasing Default: 0x0

13.1.6 PWR_BG_CONFIG

Address: 0x400B0014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None					0x0		
HW Access	None					R		
SW Access	None					RW		
Bit Name	Reserved[23:19]					VREF_EN [18:16]		

Bits	15	14	13	12	11	10	9	8
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[15:9]							BG_DFT_VCORE_SEL

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x0	0x0				0x0
HW Access	R		R	R				R
SW Access	RW		RW	RW				RW
Bit Name	BG_DFT_ICORE_SEL [7:6]		BG_DFT_CORE_SEL	BG_DFT_VREF_SEL [4:1]				BG_DFT_EN

Bandgap Trim and Configuration

Bits	Name	Description
18 : 16	VREF_EN	Reference voltage enable. Each bit enables a reference voltage used by a peripheral. Default: 0x0
8	BG_DFT_VCORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core voltage to output on mux2out 0=vout 1=vgnd Default: 0x0

13.1.6 PWR_BG_CONFIG (continued)

7 : 6	BG_DFT_ICORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects a BG core current to output on mux1out 0=iptat (current 1=ictat (current) 2=inl_cross_over detect (voltage) 3=iref9p6u_dft (dedicated output for DFT) Also selects a currect for iref_dft (when BG_DFT_VREF_SEL=13) 0=iref2p4u[1] 1=iptat2p4u[7] 2=iref_imo (9.6uA current output from IMO IBG) 3=iref3u_dft (dedicated output for DFT) Default: 0x0
5	BG_DFT_CORE_SEL	ADFT mux select for Bandgap characterization (engineering only). Selects which BG core signal to output on adft_bg_core 0=BG core voltage selected by BG_DFT_VCORE_SEL (mux2out) 1=BG core current selected by BG_DFT_ICORE_SEL (mux1out) Default: 0x0
4 : 1	BG_DFT_VREF_SEL	ADFT mux select for Reference System characterization (engineering only). Select a voltage reference to output on adft_bg_ref 0=vgnd 1=vref_fast[0] 2=vref_fast[1] 3=vref_fast[2] 4=vref_fast[3] 5=vref_fast[4] 6=vref_fast[5] 7=vref_fast[6] 8=vref_fast[7] 9=vref[0] 10=vref[1] 11=vref[2] 12=vctat 13=iref_dft (see BG_DFT_ICORE_SEL) 14=imo_iref (current) 15=inl_imoref (voltage) Default: 0x0
0	BG_DFT_EN	Enables DFT capability for Bandgap. (engineering only) Default: 0x0

13.1.7 PWR_VMON_CONFIG

Address: 0x400B0018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None						0x0	
HW Access	None						R	
SW Access	None						RW	
Bit Name	Reserved[15:10]						VMON_ADFT_SEL [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0			0x0				0x0
HW Access	R			R				R
SW Access	RW			RW				RW
Bit Name	VMON_DDFT_SEL [7:5]			LVD_SEL [4:1]				LVD_EN

Voltage Monitoring Trim and Configuration

Bits	Name	Description
9 : 8	VMON_ADFT_SEL	ADFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: Hi-Z 1: Comparator Input of pbod Monitor 2: Comparator Input of hvpbod Monitor 3: Comparator Input of lvi Monitor Default: 0x0

13.1.7 PWR_VMON_CONFIG (continued)

7 : 5	VMON_DDFT_SEL	DDFT mux select for HVPOR, PBOD, and LVD circuits (engineering only). Selects a signal to output on adft_vmon 0: 0 1: pbod_out 2: Pulse Strecher output of pbod Monitor 3: hvpbod_out 4: Pulse Strecher output of hvpbod Monitor 5: lvi_out 6: Pulse Strecher output of lvi Monitor 7: 0 Default: 0x0
4 : 1	LVD_SEL	Threshold selection for Low Voltage Detect circuit. Threshold variation is +/- 2.5% from these typical voltage choices: 0: 1.7500 V 1: 1.8000 V 2: 1.9000 V 3: 2.0000 V 4: 2.1000 V 5: 2.2000 V 6: 2.3000 V 7: 2.4000 V 8: 2.5000 V 9: 2.6000 V 10: 2.7000 V 11: 2.8000 V 12: 2.9000 V 13: 3.0000 V 14: 3.2000 V 15: 4.5000 V Default: 0x0
0	LVD_EN	Enable Low Voltage Detect circuit. Default: 0x0

13.1.8 PWR_DFT_SELECT

Address: 0x400B001C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x1	0x1
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	POWER_UP_HIBDPSLP	POWER_UP_ACTIVE	IMO_REFGEN_DIS	HVMON_DFT_OVR	NWELL_DIS	BREF_TESTMODE	BREF_REFSW	BREF_OUTEN

Bits	23	22	21	20	19	18	17	16
Reset Value	0x1	0x0	None	0x0	0x1	0x0	0x0	0x0
HW Access	R	R	None	R	R	R	R	R
SW Access	RW	RW	None	RW	RW	RW	RW	RW
Bit Name	BREF_EN	QUIET_EN	Reserved	LFCLK_OPEN	QUIET_OPEN	DEEPSLEEP_OPEN	HIBERNATE_OPEN	NWELL_OPEN

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	RSVD_BYPASS	DEEPSLEEP_EN	POWER_UP_RAW_CTL	POWER_UP_RAW_BYP	IPOR_EN	BLEED_EN	LPCOMP_DIS	ACTIVE_INRUSH_DIS

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0			0x0		
HW Access	R	R	R			R		
SW Access	RW	RW	RW			RW		
Bit Name	ACTIVE_EN	BYPASS	TVMON2_SEL [5:3]			TVMON1_SEL [2:0]		

Power DFT Mode Selection Register

Bits	Name	Description
31	POWER_UP_HIBDPSLP	When set, forces pwrg_actdig=1 for hibernate/deepsleep circuits. Combined with POWER_UP_RAW_CTL=0, this gives full control on this input for characterization and testing. Default: 0x0

13.1.8 PWR_DFT_SELECT (continued)

30	POWER_UP_ACTIVE	When set, forces pwrgood=1 for active regulator. Combined with POWER_UP_RAW_CTL=0, this gives full control on this input for characterization and testing. Default: 0x0
29	IMO_REFGEN_DIS	Disables the IMO reference generator to allow testing the current references. A side-effect of setting this bit is that the SRSS outputs vbias_ptat and vbias_casc_ptat are shorted to vccq. Default: 0x0
28	HVMON_DFT_OVR	Overrides the trim values coming from NVLatches to the values stored in the HV Monitor. Allows char test of the NVLatches without disturbing trims. Default: 0x0
27	NWELL_DIS	Controls the vnwell level during deep sleep and hibernate. When set, the nwell regulator is disabled. When this bit is set, the Vnwell rail will be shorted to Vcchib rail (nwell_short). Default: 0x0
26	BREF_TESTMODE	Puts the bootref in testmode. Intended for characterization and testing. Default: 0x0
25	BREF_REFSW	Controls the power system reference source 0: boot reference 1: Low voltage bandgap (LVBG) Using the LVBG reference improves PSRR. Only works when BYPASS=1. Intended for characterization and testing. Default: 0x1
24	BREF_OUTEN	Enables the output stage of the LDO reference selector. Do not clear this bit when the active regulator is operating. Only works when BYPASS=1. Intended for characterization and testing. Default: 0x1
23	BREF_EN	Enables the boot reference currents. Do not clear this bit unless he active regulator, quiet regulator, or LPCOMP are bypassed. Only works when BYPASS=1. Intended for characterization and testing. Default: 0x1
22	QUIET_EN	Force Vccq regulator on/off. Only works when BYPASS=1. Intended for IDDQ testing. Default: 0x0
20	LFCLK_OPEN	Force switch between Vcclfclk and Vccdpslp open. Only works when BYPASS=1. Intended for IDDQ testing. Default: 0x0
19	QUIET_OPEN	Force switch between Vccq and Vccdpslp open. Only works when BYPASS=1. Intended for IDDQ testing. Default: 0x1
18	DEEPSLEEP_OPEN	Force switch between Vccdpslp and Vccd open. Only works when BYPASS=1. Intended for IDDQ testing. Default: 0x0
17	HIBERNATE_OPEN	Force switch between Vcchib and Vccdpslp open. Only works when BYPASS=1, PWR_DFT_KEY.KEY16 is set to the key, and PWR_DFT_KEY.DFT_MODE=1. Intended for IDDQ testing. Default: 0x0
16	NWELL_OPEN	Force switch between Vnwell and Vcchib open. Only works when BYPASS=1. Intended for IDDQ testing. Default: 0x0
15	RSVD_BYPASS	Reserved, unused register. Only works when BYPASS=1. Default: 0x0

13.1.8 PWR_DFT_SELECT (continued)

14	DEEPSLEEP_EN	Force DeepSleep Regulator on. Only works when BYPASS=1. Intended for DeepSleep Regulator IDDQ testing. Default: 0x0
13	POWER_UP_RAW_CTL	Value to force onto power_up_raw_hv. Only works when POWER_UP_RAW_BYP=1. Default: 0x0
12	POWER_UP_RAW_BYP	When set, the LPCOMP output is controllable by POWER_UP_RAW_CTL. Only works when BYPASS=1. Intended for testing quiet regulator delayline, active regulator, and hibernate/deepsleep regulator. Default: 0x0
11	IPOR_EN	Force IPOR_EN signal high. Only works when BYPASS=1. Intended for IPOR/HVPOR IDDQ testing. You must bypass the IO cells using PWR_DFT_KEY.IO_DISABLE_BYPASS and .KEY16 before setting this bit. Default: 0x0
10	BLEED_EN	When set enables bleeder cells on various switched power nets to accelerate discharge during retention testing. Default: 0x0
9	LPCOMP_DIS	When set disables the LPCOMP. Only do this when the LPCOMP outputs are properly bypassed using the POWER_UP_* bits and also PWR_DFT_KEY.DFT_MODE=1. Only works when BYPASS=1. Intended for LPCOMP testing. Default: 0x0
8	ACTIVE_INRUSH_DIS	Force disable of active regulator inrush current limiter. Only works when BYPASS=1. Intended for characterization and testing. Default: 0x0
7	ACTIVE_EN	Force active regulator on. Only works when BYPASS=1. Intended for characterization and testing. Default: 0x0
6	BYPASS	Forces regulator into bypass mode. Disables active mode regulator and allows most switches and other regulators to be manually controlled though other bits in this register.. Default: 0x0
5 : 3	TVMON2_SEL	Select source for PWRSYS ADFT output #2: 0: not connected (default) 1: not connected 2: Boot Reference biasn 3: Boot Reference nprot 4: DO NOT USE. Unsafely diode couples vccd_sw to bootref 800mV reference. 5: Boot Reference 800mv 6: not connected 7: not connected Default: 0x0
2 : 0	TVMON1_SEL	Select source for PWRSYS ADFT output #1: 0: not connected (default) 1: vnwell 2: vccq 3: vccd_sw 4: vcclfclk 5: vcchib 6: vccdpslp 7: vccqr Default: 0x0

13.1.9 PWR_DDFT_SELECT

Address: 0x400B0020

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	DDFT2_SEL [7:4]				DDFT1_SEL [3:0]			

Digital DFT Select

Bits	Name	Description

13.1.9 PWR_DDFT_SELECT (continued)

7 : 4	DDFT2_SEL	Signal select for ddft2 output: 0: act_power_en_a 1: power_up_raw 2: act_power_good_a 3: fastrefs_valid 4: vmon 5: bootref_outen 6: bootref_refsw 7: active_inrush_dis 8: awake 9: hvpor_reset_n 10: lpcomp_dis 11: wakeup_a 12: vmon_valid 13: block_rst_awake 14: slpholdreq_n 15: io_disable_delayed Default: 0x0
3 : 0	DDFT1_SEL	Signal select for ddft1 output: 0: wakeup_a 1: ipor_reset 2: hbod_reset_raw_n 3: lpcomp_dis 4: power_up_delayed 5: awake 6: hvmon_out_of_sync 7: pbod_reset 8: hvbod_reset 9: lpm_ready 10: io_disable_req_lv (excluding por_force_in_hv) 11: bootref_en Default: 0x0

13.1.10 PWR_DFT_KEY

Address: 0x400B0024

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None			0x0	0x0	0x0	0x0	0x0
HW Access	None			R	R	R	R	R
SW Access	None			RW	RW	RW	RW	RW
Bit Name	Reserved[23:21]			VMON_PD	IO_DISABLE_BYPASS	DFT_MODE	BODS_OFF	HBOD_OFF_AWAKE

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	KEY16 [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	KEY16 [15: 0]							

DFT Safety Override

Bits	Name	Description
20	VMON_PD	Disables the VMON block, which includes PBOD, HVBOD, and LVD circuits. Set BODS_OFF=1 in a previous write cycle to prevent an unintended reset. Default: 0x0
19	IO_DISABLE_BYPASS	Bypasses the IO disable logic for testing the delay-line that is part of the glitch-free IO reset circuitry. Internally, prevents the outputs from getting disabled (io_disable_req_hv=0) and blocks resets (io_disable_ack_hv=0). The delay-line continues to function and can be routed to DDFT for testing. Default: 0x0
18	DFT_MODE	Enable DfT modes other than the above. Currently gates power_up comparator for characterization. Default: 0x0

13.1.10 PWR_DFT_KEY (continued)

17	BODS_OFF	Forces all outputs of BOD detectors to be ignored, effectively disabling all brown-out detection. Can be used in conjunction with DDFT to test the detectors without triggering reset. Default: 0x0
16	HBOD_OFF_AWAKE	Forces the output of the HBOD to be blocked (ignored) while in Active or Sleep mode (i.e. when under the umbrella of PBOD). Default: 0x0
15 : 0	KEY16	This field must be set to 0xE4C5 for any of the other fields in this register to have effect and for scan_mode to be allowed. When this fields has any other value, all other fields in this register are ignored and assumed to be 0 by the hardware, and scan_mode is ignored inside the power generation system. It is assumed that this register will always be set to 0xE4C5 before entering scan. Default: 0x0000

13.1.11 PWR_BOD_KEY

Address: 0x400B0028

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	KEY16 [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	None							
SW Access	RW							
Bit Name	KEY16 [15: 0]							

BOD Detection Key

Bits	Name	Description
15 : 0	KEY16	To detect brown-outs firmware should do this on boot: 1. Set key= KEY16 2. Set KEY16= 0x3A71 3. If key==0x3A71 this was a brown-out event. Default: 0x0000

13.1.12 PWR_STOP

Address: 0x400B002C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	None	None						
SW Access	RW	None						
Bit Name	STOP	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None						0x0	0x0
HW Access	None						None	None
SW Access	None						RW	RW
Bit Name	Reserved[23:18]						FREEZE	POLARITY

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	UNLOCK [15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	None							
SW Access	RW							
Bit Name	TOKEN [7:0]							

STOP Mode Register

Bits	Name	Description
31	STOP	Firmware sets this bit to enter STOP mode. Both UNLOCK and FREEZE must have been set correctly in a previous write operation. Otherwise, writes to this bit will affect the freeze override but will not actually set the STOP bit. The system will enter STOP mode immediately after writing to this bit and will wakeup only in response to XRES or WAKEUP event. Default: 0x0
17	FREEZE	Firmware sets this bit to freeze the configuration, mode and state of all GPIOs and SIOs in the system. Two identical write cycles are required to freeze the IO explicitly. The first cycle instructs DEEPSLEEP and HIBERNATE peripherals whether they can override upcoming freeze command(s). UNLOCK setting does not affect this. If firmware writes FREEZE=1 and STOP=0, peripherals can override the freeze and remain functional according to their configuration. If firmware writes FREEZE=1 and STOP=1, peripherals cannot override the next freeze command. The second write cycle freezes the IO if UNLOCK is set and the peripheral does not override the freeze. While FREEZE=1, peripherals will automatically freeze according to the override directive when entering DEEPSLEEP or HIBERNATE, regardless of the UNLOCK setting. Default: 0x0

13.1.12 PWR_STOP (continued)

16	POLARITY	0: WAKEUP=0 will wakeup the part from STOP 1: WAKEUP=1 will wakeup the part from STOP Default: 0x0
15 : 8	UNLOCK	This byte must be set to 0x3A for FREEZE or STOP fields to operate. Any other value in this register will cause FREEZE/STOP to have no effect, except as noted in the FREEZE description. Default: 0x00
7 : 0	TOKEN	Contains a 8-bit token that is retained through a STOP/WAKEUP sequence that can be used by firmware to differentiate WAKEUP from a general RESET event. Note that waking up from STOP using XRES will reset this register. Default: 0x00

13.1.13 CLK_SELECT

Address: 0x400B0100

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None		0x0			0x0	0x0	
HW Access	None		R			R	R	
SW Access	None		RW			RW	RW	
Bit Name	Reserved[23:22]		SYSCLK_DIV [21:19]			HALF_EN	HFCLK_SEL [17:16]	

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0		0x0		0x0			0x0
HW Access	None		R		R			R
SW Access	RW		RW		RW			RW
Bit Name	WDT_LOCK [15:14]		DPLLREF_SEL [13:12]		DPLLIN_SEL [11:9]			PLL_SEL [8:6]

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x0			0x0		
HW Access	R		R			R		
SW Access	RW		RW			RW		
Bit Name	PLL_SEL [8: 6]		DBL_SEL [5:3]			DIRECT_SEL [2:0]		

Clock Select Register

Bits	Name	Description
21 : 19	SYSCLK_DIV	SYSCLK Pre-Scaler Value. Default: 0x0 **0x0: NO_DIV** SYSCLK= HFCLK/1 **0x1: DIV_BY_2** SYSCLK= HFCLK/2 **0x2: DIV_BY_4** SYSCLK= HFCLK/4

13.1.13 CLK_SELECT (continued)

		0x3: DIV_BY_8 SYSCLK= HFCLK/8 **0x4: DIV_BY_16** SYSCLK= HFCLK/16 **0x5: DIV_BY_32** SYSCLK= HFCLK/32 **0x6: DIV_BY_64** SYSCLK= HFCLK/64 **0x7: DIV_BY_128** SYSCLK= HFCLK/128
18	HALF_EN	This bit impact products using CPUSSv1 only. It has no effect on products using CPUSSv2. FLASH Wait-state selection. This must be set to 1 when clk_sys is set to a frequency greater than 24MHz. 0: Access FLASH using 0 wait-states. Only use this setting when HFCLK is lt;=24MHz. 1: Access FLASH using 1 wait-state. Safe to use this setting for any clock frequency. Default: 0x0
17 : 16	HFCLK_SEL	Selects the source for HFCLK. Default: 0x0 **0x0: DIRECT_SEL** Source selected by DIRECT_SEL **0x1: DBL** Output of DBL (Doubler) **0x2: PLL** Output of PLL
15 : 14	WDT_LOCK	Prohibits writing to WDT_* registers and CLK_ILO/WCO_CONFIG registerst when not equal 0. Requires at least two different writes to unlock. Note that this field is 2 bits to force multiple writes only. It represents only a single write protect signal protecting all WATCHDOG registers at the same time. Default: 0x0 **0x0: NO_CHG** No effect **0x1: CLR0** Clears bit 0 **0x2: CLR1** Clears bit 1 **0x3: SET01** Sets both bits 0 and 1

13.1.13 CLK_SELECT (continued)

13 : 12	DPLLREF_SEL	Selects a source for the reference (tracking) input of DPLL: 0: DSI_OUT[0] 1: DSI_OUT[1] 2: DSI_OUT[2] 3: DSI_OUT[3] Default: 0x0 **0x0: DSI0** DSI_OUT[0] **0x1: DSI1** DSI_OUT[1] **0x2: DSI2** DSI_OUT[2] **0x3: DSI3** DSI_OUT[3]
11 : 9	DPLLIN_SEL	Selects a source for the input of DPLL. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default: 0x0 **0x0: IMO** IMO - Internal R/C Oscillator **0x1: EXTCLK** EXTCLK - External Clock Pin **0x2: ECO** ECO - Internal Crystal Oscillator **0x4: DSI0** DSI_OUT[0] **0x5: DSI1** DSI_OUT[1] **0x6: DSI2** DSI_OUT[2] **0x7: DSI3** DSI_OUT[3]
8 : 6	PLL_SEL	Selects a source for the input of the PLL. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default: 0x0 **0x0: IMO** IMO - Internal R/C Oscillator

13.1.13 CLK_SELECT (continued)

		0x1: EXTCLK EXTCLK - External Clock Pin **0x2: ECO** ECO - Internal Crystal Oscillator **0x3: DPLL** DPLL - DPLL Output **0x4: DSI0** DSI_OUT[0] **0x5: DSI1** DSI_OUT[1] **0x6: DSI2** DSI_OUT[2] **0x7: DSI3** DSI_OUT[3]
5 : 3	DBL_SEL	Selects a source for the input of DBL. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default: 0x0 **0x0: IMO** IMO - Internal R/C Oscillator **0x1: EXTCLK** EXTCLK - External Clock Pin **0x2: ECO** ECO - Internal Crystal Oscillator **0x4: DSI0** DSI_OUT[0] **0x5: DSI1** DSI_OUT[1] **0x6: DSI2** DSI_OUT[2] **0x7: DSI3** DSI_OUT[3]

13.1.13 CLK_SELECT (continued)

2 : 0	DIRECT_SEL	Selects a source for HFCLK (when HFCLK_SEL=0) and DSI_IN[0]. Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Note that using DSI_OUT[3:0] as HFCLK source will also result in undefined behavior. These values are available strictly to provide a clock in DSI_IN[0]. Default: 0x0 **0x0: IMO** IMO - Internal R/C Oscillator **0x1: EXTCLK** EXTCLK - External Clock Pin **0x2: ECO** ECO - Internal Crystal Oscillator **0x4: DSI0** DSI_OUT[0] **0x5: DSI1** DSI_OUT[1] **0x6: DSI2** DSI_OUT[2] **0x7: DSI3** DSI_OUT[3]

13.1.14 CLK_ILO_CONFIG

Address: 0x400B0104

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	ENABLE	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x1	0x1	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[7:3]					SATBIAS	TURBO	PD_MODE

ILO Configuration

Bits	Name	Description
31	ENABLE	Master enable for ILO oscillator Default: 0x0
2	SATBIAS	PFET bias Default: 0x1 **0x0: SATURATED** Enable saturated PFET bias **0x1: SUBTHRESHOLD** Enable subthreshold PFET bias

13.1.14 CLK_ILO_CONFIG (continued)

1	TURBO	Turbo mode for faster startup from coma power down 0: turbo disabled 1: turbo enabled Default: 0x1
0	PD_MODE	Power down mode. Note: this bit must always be set to 0 and never changed. Behavior is un-defined when set to 1. Default: 0x0 **0x0: SLEEP** Sleep (faster startup - enables pulsegen block) **0x1: COMA** Coma (slower startup)

13.1.15 CLK_IMO_CONFIG

Address: 0x400B0108

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x1	0x0	0x0	0x0	0x0			0x0
HW Access	R	R	R	R	R			R
SW Access	RW	RW	RW	RW	RW			RW
Bit Name	ENABLE	EN_CLK2X	EN_CLK36	TEST_USB_MODE	PUMP_SEL [27:25]			TEST_FASTBIAS

Bits	23	22	21	20	19	18	17	16
Reset Value	0x1	0x0	None					
HW Access	R	R	None					
SW Access	RW	RW	None					
Bit Name	EN_FASTBIAS	FLASHPUMP_SEL	Reserved[21:16]					

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

IMO Configuration

Bits	Name	Description
31	ENABLE	Master enable for IMO oscillator. Clearing this bit will disable the IMO but not disconnect it from the power rail. This bit can also be used during IDDQ testing. Default: 0x1
30	EN_CLK2X	Enables main oscillator doubler circuit that can be used for TSS Charge Pumps. This circuit is not available to generate any digital clocks. Default: 0x0

13.1.15 CLK_IMO_CONFIG (continued)

29	EN_CLK36	Enables 36MHz secondary oscillator that can be used for Pump or Flash Pump. Note: Since there are two consumers of the 36MHz clock, care should be taken when clearing this bit. The correct procedure for clearing this bit is: 1. Disable interrupts 2. Check if both FLASHPUMP_SELlt;gt;1 and PUMP_SELlt;gt;3 3. If so, set EN_CLK36=0 4. Enable interrupts Default: 0x0
28	TEST_USB_MODE	Forces IMO into USB mode. Engineering only. 1: Software can write FSOFFSET, OFFSET, and GAIN settings for characterization. Hardware updates to these registers are not blocked, so disable USB peripheral updates if they are not desired. 0: Normal operation. IMO operates in either USB or non-USB mode, depending on the USB peripheral setting. Default: 0x0
27 : 25	PUMP_SEL	Selects operating source for Pump clock. This clock is not guaranteed to be glitch free when changing IMO parameters or clock divider settings. 5-7: reserved, do not use Default: 0x0 **0x0: GND** No clock, connect to gnd **0x1: IMO** Use main IMO output **0x2: DBL** Use doubler output **0x3: CLK36** Use 36MHz oscillator **0x4: FF1** Use divided clock FF1
24	TEST_FASTBIAS	Forces the IMO into FIMO mode (engineering only). Only works when EN_FASTBIAS=1. Default: 0x0
23	EN_FASTBIAS	Forces the FIMOs fast bias circuits to remain powered (engineering only). This bit must be cleared by BootROM after FIMO is no longer required. Default: 0x1
22	FLASHPUMP_SEL	Selects operating source for SPCIF Timer/Flash Pump clock. Default: 0x0 **0x0: GND** No clock, connect to gnd **0x1: CLK36** Use 36MHz oscillator

13.1.16 CLK_IMO_SPREAD

Address: 0x400B010C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		0x0		None			
HW Access	R		R		None			
SW Access	RW		RW		None			
Bit Name	SS_MODE [31:30]		SS_RANGE [29:28]		Reserved[27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None			0x00				
HW Access	None			R				
SW Access	None			RW				
Bit Name	Reserved[15:13]			SS_MAX [12:8]				

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x00				
HW Access	None			None				
SW Access	None			RW				
Bit Name	Reserved[7:5]			SS_VALUE [4:0]				

IMO Spread Spectrum Configuration

Bits	Name	Description
31 : 30	SS_MODE	Spread Spectrum Mode. Default: 0x0 **0x0: OFF** Off, do not change SS_VALUE **0x1: TRIANGLE** Modulate using triangle wave (see SS_MAX) **0x2: LFSR** Modulate using pseudo random sequence (using LFSR)

13.1.16 CLK_IMO_SPREAD (continued)

		0x3: DSI Take value directly from DSI (synchronized by divided clock FF1)
29 : 28	SS_RANGE	Spread spectrum range (downspread when SS_VALUE=16). 3: reserved, do not use Default: 0x0 **0x0: M1** 0 .. -1% **0x1: M2** 0 .. -2% **0x2: M4** 0 .. -4%
12 : 8	SS_MAX	Maximum counter value for spread spectrum. Counter will count from 0..SS_MAX..0 and keep repeating this indefinitely. Only works when SS_MODE=1. Default: 0x00
4 : 0	SS_VALUE	Current offset value for spread spectrum modulation. IMO supports values 0..16. Step size is determined by SS_RANGE. Value is encoded in proper thermometric format for IMO in hardware. Value can be modified in firmware only when SS_MODE=0. Default: 0x00

13.1.17 CLK_DFT_SELECT

Address: 0x400B0110

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x0		0x0			
HW Access	None		R		R			
SW Access	None		RW		RW			
Bit Name	Reserved[15:14]		DFT_DIV2 [13:12]		DFT_SEL2 [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0		0x0			
HW Access	None		R		R			
SW Access	None		RW		RW			
Bit Name	Reserved[7:6]		DFT_DIV1 [5:4]		DFT_SEL1 [3:0]			

Clock DFT Mode Selection Register

Bits	Name	Description
13 : 12	DFT_DIV2	DFT Output Divide Down. Default: 0x0 **0x0: NO_DIV** Direct Output **0x1: DIV_BY_2** Divide by 2 **0x2: DIV_BY_4** Divide by 4

13.1.17 CLK_DFT_SELECT (continued)

0x3: DIV_BY_8
Divide by 8

11 : 8	DFT_SEL2	Select signal for DFT output #2. Default: 0x0 **0x0: NC** Disabled - output is not connected **0x1: ILO** ILO output **0x2: WCO** WCO output **0x3: IMO** IMO primary output **0x4: ECO** ECO output **0x5: PLL** PLL output **0x6: DPLL_OUT** DPLL output **0x7: DPLL_REF** DPLL reference input **0x8: DBL** DBL output **0x9: IMO2X** IMO 2x Clock Output **0xA: IMO36** IMO 36MHz Clock Output **0xB: HFCLK** HFCLK **0xC: LFCLK** LFCLK **0xD: SYSCLK** SYSCLK

13.1.17 CLK_DFT_SELECT (continued)

		0xE: EXTCLK EXTCLK **0xF: HALFSYSCLK** 0 - removed
5 : 4	DFT_DIV1	DFT Output Divide Down. Default: 0x0 **0x0: NO_DIV** Direct Output **0x1: DIV_BY_2** Divide by 2 **0x2: DIV_BY_4** Divide by 4 **0x3: DIV_BY_8** Divide by 8
3 : 0	DFT_SEL1	Select signal for DFT output #1. Default: 0x0 **0x0: NC** Disabled - output is not connected **0x1: ILO** ILO output **0x2: WCO** WCO output **0x3: IMO** IMO primary output **0x4: ECO** ECO output **0x5: PLL** PLL output **0x6: DPLL_OUT** DPLL output **0x7: DPLL_REF** DPLL reference input

13.1.17 CLK_DFT_SELECT (continued)

0x8: DBL
DBL output

0x9: IMO2X
IMO 2x Clock Output

0xA: IMO36
IMO 36MHz Clock Output

0xB: HFCLK
HFCLK

0xC: LFCLK
LFCLK

0xD: SYSCLK
SYSCLK

0xE: EXTCLK
EXTCLK

0xF: HALFSYSCLK
0 - removed

13.1.18 WDT_CTRLOW

Address: 0x400B0200

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR1 [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR1 [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR0 [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR0 [15: 0]							

Watchdog Counters 0/1

Bits	Name	Description
31 : 16	WDT_CTR1	Current value of WDT Counter 1 Default: 0x0000
15 : 0	WDT_CTR0	Current value of WDT Counter 0 Default: 0x0000

13.1.19 WDT_CTRHIGH

Address: 0x400B0204

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR2 [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR2 [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR2 [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	RW							
SW Access	R							
Bit Name	WDT_CTR2 [31: 0]							

Watchdog Counter 2

Bits	Name	Description
31 : 0	WDT_CTR2	Current value of WDT Counter 2 Default: 0x00000000

13.1.20 WDT_MATCH

Address: 0x400B0208

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	WDT_MATCH1 [31:16]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	WDT_MATCH1 [31: 16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	WDT_MATCH0 [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	R							
SW Access	RW							
Bit Name	WDT_MATCH0 [15: 0]							

Watchdog counter match values

Bits	Name	Description
31 : 16	WDT_MATCH1	Match value for Watchdog Counter 1 Default: 0x0000
15 : 0	WDT_MATCH0	Match value for Watchdog Counter 0 Default: 0x0000

13.1.21 WDT_CONFIG

Address: 0x400B020C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0		None	0x00				
HW Access	R		None	R				
SW Access	RW		None	RW				
Bit Name	LFCLK_SEL [31:30]		Reserved	WDT_BITS2 [28:24]				

Bits	23	22	21	20	19	18	17	16
Reset Value	None							0x0
HW Access	None							R
SW Access	None							RW
Bit Name	Reserved[23:17]							WDT_MODE2

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	
HW Access	None				R	R	R	
SW Access	None				RW	RW	RW	
Bit Name	Reserved[15:12]				WDT_CASCADE1_2	WDT_CLEAR1	WDT_MODE1 [9:8]	

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	
HW Access	None				R	R	R	
SW Access	None				RW	RW	RW	
Bit Name	Reserved[7:4]				WDT_CASCADE0_1	WDT_CLEAR0	WDT_MODE0 [1:0]	

Watchdog Counters Configuration

Bits	Name	Description
31 : 30	LFCLK_SEL	Select source for LFCLK: 0: ILO - Internal R/C Oscillator 1: WCO - Internal Crystal Oscillator 2-3: Reserved - do not use Note that not all products support all clock sources. Selecting a clock source that is not supported will result in undefined behavior. Default: 0x0

13.1.21 WDT_CONFIG (continued)

28 : 24	WDT_BITS2	Bit to observe for WDT_INT2: 0: Assert when bit0 of WDT_CTR2 toggles (one int every tick) .. 31: Assert when bit31 of WDT_CTR2 toggles (one int every 2^31 ticks) Default: 0x00
16	WDT_MODE2	Watchdog Counter 2 Mode. Default: 0x0 **0x0: NOTHING** Free running counter with no interrupt requests **0x1: INT** Free running counter with interrupt request when a specified bit in CTR2 toggles (see WDT_BITS2)
11	WDT_CASCADE1_2	Cascade Watchdog Counters 1,2. Counter 2 increments the cycle after WDT_CTR1=WDT_MATCH1. It is allowed to cascade all three WDT counters. 0: Independent counters 1: Cascaded counters Default: 0x0
10	WDT_CLEAR1	Clear Watchdog Counter when WDT_CTR1=WDT_MATCH1. In other words WDT_CTR1 divides LFCLK by (WDT_MATCH1+1). 0: Free running counter 1: Clear on match Default: 0x0
9 : 8	WDT_MODE1	Watchdog Counter Action on Match (WDT_CTR1=WDT_MATCH1). Default: 0x0 **0x0: NOTHING** Do nothing **0x1: INT** Assert WDT_INTx **0x2: RESET** Assert WDT Reset **0x3: INT_THEN_RESET** Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt
3	WDT_CASCADE0_1	Cascade Watchdog Counters 0,1. Counter 1 increments the cycle after WDT_CTR0=WDT_MATCH0. 0: Independent counters 1: Cascaded counters Default: 0x0
2	WDT_CLEAR0	Clear Watchdog Counter when WDT_CTR0=WDT_MATCH0. In other words WDT_CTR0 divides LFCLK by (WDT_MATCH0+1). 0: Free running counter 1: Clear on match Default: 0x0
1 : 0	WDT_MODE0	Watchdog Counter Action on Match (WDT_CTR0=WDT_MATCH0). Default: 0x0

13.1.21 WDT_CONFIG (continued)

0x0: NOTHING
Do nothing

0x1: INT
Assert WDT_INTx

0x2: RESET
Assert WDT Reset

0x3: INT_THEN_RESET
Assert WDT_INTx, assert WDT Reset after 3rd unhandled interrupt

13.1.22 WDT_CONTROL

Address: 0x400B0210

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW0C	None	RW	R
SW Access	None				RW1S	RW1C	R	RW
Bit Name	Reserved[23:20]				WDT_RESET2	WDT_INT2	WDT_ENABLED2	WDT_ENABLE2

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW0C	None	RW	R
SW Access	None				RW1S	RW1C	R	RW
Bit Name	Reserved[15:12]				WDT_RESET1	WDT_INT1	WDT_ENABLED1	WDT_ENABLE1

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0	0x0	0x0	0x0
HW Access	None				RW0C	None	RW	R
SW Access	None				RW1S	RW1C	R	RW
Bit Name	Reserved[7:4]				WDT_RESET0	WDT_INT0	WDT_ENABLED0	WDT_ENABLE0

Watchdog Counters Control

Bits	Name	Description
19	WDT_RESET2	Resets counter 2 back to 0000_0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default: 0x0
18	WDT_INT2	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Default: 0x0
17	WDT_ENABLED2	Indicates actual state of counter. May lag WDT_ENABLE2 by up to 3 LFCLK cycles. Default: 0x0

13.1.22 WDT_CONTROL (continued)

16	WDT_ENABLE2	Enable Counter 2 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default: 0x0
11	WDT_RESET1	Resets counter 1 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default: 0x0
10	WDT_INT1	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default: 0x0
9	WDT_ENABLED1	Indicates actual state of counter. May lag WDT_ENABLE1 by up to 3 LFCLK cycles. Default: 0x0
8	WDT_ENABLE1	Enable Counter 1 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default: 0x0
3	WDT_RESET0	Resets counter 0 back to 0000. Hardware will reset this bit after counter was reset. This will take several LFCLK cycles to take effect. Default: 0x0
2	WDT_INT0	WDT Interrupt Request. This bit is set by hardware as configured by this registers. This bit must be cleared by firmware. Clearing this bit also prevents Reset from happening when WDT_MODEx=3. Default: 0x0
1	WDT_ENABLED0	Indicates actual state of counter. May lag WDT_ENABLE0 by up to 3 LFCLK cycles. Default: 0x0
0	WDT_ENABLE0	Enable Counter 0 0: Counter is disabled (not clocked) 1: Counter is enabled (counting up) Note: This field takes considerable time (up to 3 LFCLK cycles) to take effect. It must not be changed more than once in that period. Default: 0x0

13.1.23 RES_CAUSE

Address: 0x400B0300

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S	RW1S
SW Access	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C	RW1C
Bit Name	RESET_XRES	RESET_PBOD	RESET_HVBOD	RESET_SOFT	RESET_PROT_FAULT	RESET_LOCKUP	RESET_DSBOD	RESET_WDT

Reset Cause Observation Register

Bits	Name	Description
7	RESET_XRES	This field is deprecated and will always read 0. Default: 0x0
6	RESET_PBOD	This field is deprecated and will always read 0. Default: 0x0
5	RESET_HVBOD	This field is deprecated and will always read 0. Default: 0x0
4	RESET_SOFT	Cortex-M0 requested a system reset through its SYSRESETREQ. This can be done via a debugger probe or in firmware. Default: 0x0

13.1.23 RES_CAUSE (continued)

3	RESET_PROT_FAULT	A protection violation occurred that requires a RESET. This includes, but is not limited to, hitting a debug breakpoint while in Privileged Mode. Default: 0x0
2	RESET_LOCKUP	This field is deprecated and will always read 0. Cortex-M0 LOCKUP is no longer a reset source. Default: 0x0
1	RESET_DSBOD	This field is deprecated and will always read 0. Default: 0x0
0	RESET_WDT	A WatchDog Timer reset has occurred since last power cycle. Default: 0x0

13.1.24 RES_DFT_SELECT

Address: 0x400B0304

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None			0x0	0x0			
HW Access	None			R	R			
SW Access	None			RW	RW			
Bit Name	Reserved[7:5]			DFT_EN	DFT_SEL [3:0]			

Reset DFT Mode Selection Register

Bits	Name	Description
4	DFT_EN	Reset DFT Output enable. Setting this bit will drive the selected reset signal directly onto the designated DDFT output pin. See PAS for details on product pinout. Note that this register field is reset only on power-on and not by any other reset happening in the system. This bit is protected by HVMON, so the HVMON must be disabled before writing a new value or the device will reset. Default: 0x0
3 : 0	DFT_SEL	Select signal for reset DFT output. Note that this register field is never reset and therefore has a random power on value. Default: 0x0 **0x0: GND** 0 (output always grounded)

13.1.24 RES_DFT_SELECT (continued)

0x1: RST_DEBUG_N
rst_debug_n

0x2: RST_SLPCTRL_N
rst_slpctrl_n

0x3: RST_SYSTEM_N
rst_system_n

0x4: HBOD_RESET_N
~por_force

0x5: XRES_RESET_N
0 (output always grounded).

0x6: PBOD_RESETREQ
0 (output always grounded). Use PWR_DDFT_SELECT instead.

0x7: HVBOD_RESETREQ
0 (output always grounded). Use PWR_DDFT_SELECT instead.

0x8: SYSRESETREQ
sysresetreq

0x9: PROTECTION_FAULT
protection_fault

0xA: LOCKUP
lockup

0xB: DSBOD_RESETREQ
0 (output always grounded). Use PWR_DDFT_SELECT instead.

0xC: WDT_RESETREQ
wdt_resetreq

13.1.25 PWR_PWRSYS_TRIM1

Address: 0x400BFF00

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0				0x0	0x0		
HW Access	R				R	R		
SW Access	RW				RW	RW		
Bit Name	BOD_TRIM_TRIP [7:4]				BOD_TURBO_THRESH	HIB_BIAS_TRIM [2:0]		

Power System Trim Register

Bits	Name	Description
7 : 4	BOD_TRIM_TRIP	BOD trip point trim. BOD_TRIM_TRIP[2] is ignored and controlled by hardware directly. 0X00: Default trim setting 0X01: Default trim setting - 30mV 0X10: Default trim setting + 30mV 0X11: Invalid Setting (Do Not Use) 1X00: Default trim setting + 90mV 1X01: Default trim setting + 60mV 1X10: Default trim setting + 120mV 1X11: Invalid Setting (Do Not Use) Default: 0x0

13.1.25 PWR_PWRSYS_TRIM1 (continued)

3	BOD_TURBO_THRESH	BOD Turbo Threshold Control 0 Turbo Threshold is set to 100mV above BOD trip point 1 Turbo Threshold is set to 50mV above BOD trip point Default: 0x0
2 : 0	HIB_BIAS_TRIM	Current reference trim. This is internally overridden to 3b010 for startup during POR and STOP wakeup. Afterward, it uses this setting for hibernate and sleep. Default: 0x0

13.1.26 PWR_PWRSYS_TRIM2

Address: 0x400BFF04

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x3		0x0		0x3	
HW Access	R	R	R		R		R	
SW Access	RW	RW	RW		RW		RW	
Bit Name	DPSLP_TRIM_VOLTAGE	DPSLP_TRIM_LEAKAGE	DPSLP_TRIM_LOAD [5:4]		LFCLK_TRIM_VOLTAGE [3:2]		LFCLK_TRIM_LOAD [1:0]	

Power System Trim Register

Bits	Name	Description
7	DPSLP_TRIM_VOLTAGE	Raise output voltage 1= regulator hibernate 200mV higher 0= nominal 1.4-1.6V range Default: 0x0
6	DPSLP_TRIM_LEAKAGE	Enable Vcchib pass gate leakage control Default: 0x0
5 : 4	DPSLP_TRIM_LOAD	Current load trim capability 00= Min current load capability 11= Max current load capability Default: 0x3

13.1.26 PWR_PWRSYS_TRIM2 (continued)

3 : 2	LFCLK_TRIM_VOLTAGE	Output voltage trim 00= default 01= Trim lfclk by -50mV 10= Trim lfclk by +50mV 11= illegal Default: 0x0
1 : 0	LFCLK_TRIM_LOAD	Current load trim capability 00= Min current load capability 11= Max current load capability Default: 0x3

13.1.27 PWR_PWRSYS_TRIM3

Address: 0x400BFF08

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00					0x1		
HW Access	R					R		
SW Access	RW					RW		
Bit Name	QUIET_TRIM [7:3]					NWELL_TRIM [2:0]		

Power System Trim Register

Bits	Name	Description
7 : 3	QUIET_TRIM	Vccq (quiet regulator) trim Default: 0x1F
2 : 0	NWELL_TRIM	Vnwell (nwell regulator) trim [0]: Vcchib + nhv(0.6V -1V) [1]: Vcchib + nlowvt(0.4 -0.8V) [2]: Vcchib + nhvnat(0.1-0.3) Default: 0x1

13.1.28 PWR_PWRSYS_TRIM4

Address: 0x400BFF0C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x0		0x0	0x1	0x0	
HW Access	None		R		R	R	R	
SW Access	None		RW		RW	RW	RW	
Bit Name	Reserved[7:6]		HIB_TRIM_REFERENCE [5:4]		HIB_TRIM_ VOLTAGE	HIB_TRIM_ LEAKAGE	HIB_TRIM_NWELL [1:0]	

Power System Trim Register

Bits	Name	Description
5 : 4	HIB_TRIM_REFERENCE	Hibernate Reference trim 10=Trim reference by -27mV 01=Trim reference by +27mV 00= no trim Default: 0x0
3	HIB_TRIM_VOLTAGE	Elevate output voltage 1= regulator hibernate 200mV higher 0= nominal 1.4-1.6V range Default: 0x0
2	HIB_TRIM_LEAKAGE	Enable Vcchib pass gate leakage control Default: 0x1

13.1.28 PWR_PWRSYS_TRIM4 (continued)

1 : 0	HIB_TRIM_NWELL	Vnwell Leakage control 00= smart nwell regulation 01= regulate nwell to constant voltage. 10= regulate nwell to vcchib + nfet diode 11= regulate nwell to vcchib + nfet diode Default: 0x0

13.1.29 PWR_BG_TRIM1

Address: 0x400BFF10

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0x8				0x3		
HW Access	None	R				R		
SW Access	None	RW				RW		
Bit Name	Reserved	INL_CROSS_MAIN [6:3]				INL_TRIM_MAIN [2:0]		

Bandgap Trim Register

Bits	Name	Description
6 : 3	INL_CROSS_MAIN	Bandgap INL cross-over point control for centering curve at 30C (main current reference). Default: 0x8
2 : 0	INL_TRIM_MAIN	Bandgap nonlinear current trim for curvature correction (main current reference). Default: 0x3

13.1.30 PWR_BG_TRIM2

Address: 0x400BFF14

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0	0x0	0x0		0x8			
HW Access	R	R	R		R			
SW Access	RW	RW	RW		RW			
Bit Name	VCTAT_VOLTAGE_MSB	VCTAT_ENABLE	VCTAT_VOLTAGE [5:4]		VCTAT_SLOPE [3:0]			

Bandgap Trim Register

Bits	Name	Description
7	VCTAT_VOLTAGE_MSB	Output voltage absolute trim (MSB) Default: 0x0
6	VCTAT_ENABLE	Enable VCTAT block Default: 0x0
5 : 4	VCTAT_VOLTAGE	Output voltage absolute trim (LSBs). MSB is in VCTAT_VOLTAGE_MSB field. Default: 0x0
3 : 0	VCTAT_SLOPE	Output slope setting controls. The slope of the voltage with temperature varies from ~0% to ~15% from the value at 55C over the temperature range -40C to 150C based on control signal settings 0 to 15 Default: 0x8

13.1.31 PWR_BG_TRIM3

Address: 0x400BFF18

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None	0xB				0x7		
HW Access	None	R				R		
SW Access	None	RW				RW		
Bit Name	Reserved	INL_CROSS_IMO [6:3]				INL_TRIM_IMO [2:0]		

Bandgap Trim Register

Bits	Name	Description
6 : 3	INL_CROSS_IMO	IMO Irefgen INL cross-over point control for centering curve at 30C. Default: 0xB
2 : 0	INL_TRIM_IMO	IMO Irefgen nonlinear current trim for curvature correction. Default: 0x7

13.1.32 PWR_BG_TRIM4

Address: 0x400BFF1C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		ABS_TRIM_IMO [5:0]					

Bandgap Trim Register

Bits	Name	Description
5 : 0	ABS_TRIM_IMO	IMO-irefgen output current magnitude trim Default: 0x20

13.1.33 PWR_BG_TRIM5

Address: 0x400BFF20

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		TMPCO_TRIM_IMO [5:0]					

Bandgap Trim Register

Bits	Name	Description
5 : 0	TMPCO_TRIM_IMO	IMO-irefgen output current temperature co-efficient trim Default: 0x20

13.1.34 CLK_ILO_TRIM

Address: 0x400BFF24

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x3				0x8			
HW Access	R				R			
SW Access	RW				RW			
Bit Name	COARSE_TRIM [7:4]				TRIM [3:0]			

ILO Trim Register

Bits	Name	Description
7 : 4	COARSE_TRIM	Adjusts the bias in the event of high current after fab: Bias trim: bit3=0: Normal Mode bit3=1:Low Current Mode Resistor Trim (Short R to gnd): bit2=0: Normal Mode bit2=1: Short R/4 bit1=0: Unshort R/2 bit1=1: Normal Mode (Short R/2) bit0=0: Unshort R/4 bit0=1: Normal Mode (Short 3R/4) Default: 0x3

13.1.34 CLK_ILO_TRIM (continued)

3 : 0	TRIM	Trim bits to control frequency 0: Minimum frequency 15: Maximum frequency Default: 0x8

13.1.35 CLK_IMO_TRIM1

Address: 0x400BFF28

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00							
HW Access	RW							
SW Access	RW							
Bit Name	OFFSET [7:0]							

IMO Trim Register

Bits	Name	Description
7 : 0	OFFSET	Frequency trim bits. These bits are determined at manufacturing time for each FREQ setting (IMO_TRIM2) and stored in SFLASH. This field is hardware updated during USB osclock mode. Default: 0x80

13.1.36 CLK_IMO_TRIM2

Address: 0x400BFF2C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x19					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		FREQ [5:0]					

IMO Trim Register

Bits	Name	Description
5 : 0	FREQ	Frequency to be selected (default 24MHz). Frequencies can be selected from 3..48MHz. When changing this field approriate values for IMO_CLK_TRIM1, PWR_BG_TRIM4 and PWR_BG_TRIM5 must be selected from trim tables determined at manufacturing time and stored in SFLASH. This process is documented in the SAS under Clocks - Selecting IMO Frequency. For encoding of this field a lookup table is required, where the frequency increases in 1MHz steps in the regions listed below. Unspecified values have undefined behavior. A complete lookup table is in BROS 001-59652 Sec 4.2.2. [3-12] =gt; [3MHz-12MHz] [14-25] =gt; [13MHz-24MHz] [27-35] =gt; [25MHz-33MHz] [37-43] =gt; [34MHz-40MHz] [46-53] =gt; [41MHz-48MHz] Default: 0x19

13.1.37 CLK_IMO_TRIM3

Address: 0x400BFF30

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				TRIM_CLK36 [3:0]			

IMO Trim Register

Bits	Name	Description
3 : 0	TRIM_CLK36	Trim bits for 36MHz oscillator. Typically stored in SFLASH and copied here on boot. Default: 0x0

13.1.38 CLK_IMO_TRIM4

Address: 0x400BFF34

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0			0x00				
HW Access	RW			R				
SW Access	RW			RW				
Bit Name	FSOFFSET [7:5]			GAIN [4:0]				

IMO Trim Register

Bits	Name	Description
7 : 5	FSOFFSET	Full-speed USB offset. Updated by hardware during USB osclock mode. Can be updated by software when TEST_USB_MODE=1. Otherwise writes are ignored. Engineering only. Default: 0x0
4 : 0	GAIN	Gain for IMO. Typically stored in SFLASH and copied here on boot. Only used during USB mode, either during USB operation or when CLK_IMO_CONFIG.TEST_USB_MODE=1. When not in USB mode, this register is not used and the actual IMO gain is forced to a setting of 0. Default: 0x00

13.1.39 PWR_RSVD_TRIM

Address: 0x400BFF38

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				RSVD_TRIM [3:0]			

Reserved, unused registers

Bits	Name	Description
3 : 0	RSVD_TRIM	Reserved, unused registers. Default: 0x0

14 TCPWM Registers

This section discusses the TCPWM registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

14.1 TCPWM Register Mapping Overview

Register Name	Address
TCPWM_CTRL	0x40050000
TCPWM_CMD	0x40050008
TCPWM_INTR_CAUSE	0x4005000C

14.1.1 TCPWM_CTRL

Address: 0x40050000

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				R			
SW Access	None				RW			
Bit Name	Reserved[7:4]				TCPWM_COUNTER_ENABLED [3:0]			

TCPWM control register 0.

Bits	Name	Description
3 : 0	TCPWM_COUNTER_ENABLED	Counter enables for counters 0 up to CNT_NR-1. When 0: counter disabled. When 1: counter enabled. Counter control information should only be modified when the counter is disabled. When a counter is disabled, the associated counter triggers in the MMIO CMD register are set to 0. Default: 0x0

14.1.2 TCPWM_CMD

Address: 0x40050008

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None				0x0			
HW Access	None				RW1C			
SW Access	None				RW1S			
Bit Name	Reserved[31:28]				TCPWM_COUNTER_START [27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None				0x0			
HW Access	None				RW1C			
SW Access	None				RW1S			
Bit Name	Reserved[23:20]				TCPWM_COUNTER_STOP [19:16]			

Bits	15	14	13	12	11	10	9	8
Reset Value	None				0x0			
HW Access	None				RW1C			
SW Access	None				RW1S			
Bit Name	Reserved[15:12]				TCPWM_COUNTER_RELOAD [11:8]			

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				RW1C			
SW Access	None				RW1S			
Bit Name	Reserved[7:4]				TCPWM_COUNTER_CAPTURE [3:0]			

TCPWM command register.

Bits	Name	Description
27 : 24	TCPWM_COUNTER_START	Counters SW start trigger. For HW behavior, see COUNTER_CAPTURE field. Default: 0x0
19 : 16	TCPWM_COUNTER_STOP	Counters SW stop trigger. For HW behavior, see COUNTER_CAPTURE field. Default: 0x0
11 : 8	TCPWM_COUNTER_RELOAD	Counters SW reload trigger. For HW behavior, see COUNTER_CAPTURE field. Default: 0x0
3 : 0	TCPWM_COUNTER_CAPTURE	Counters SW capture trigger. When written with 1, a capture trigger is generated and the HW sets the field to 0 when the SW trigger has taken effect. It should be noted that the HW operates on the counter frequency. If the counter is disabled through CTRL.COUNTER_ENABLED, the field is immediately set to 0. Default: 0x0

14.1.3 TCPWM_INTR_CAUSE

Address: 0x4005000C

Retention: Not Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None				0x0			
HW Access	None				W			
SW Access	None				R			
Bit Name	Reserved[7:4]				TCPWM_COUNTER_INT [3:0]			

TCPWM Counter interrupt cause register.

Bits	Name	Description
3 : 0	TCPWM_COUNTER_INT	Counters interrupt signal active. Default: 0x0

15 TST Registers

This section discusses the TST registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

15.1 TST Register Mapping Overview

Register Name	Address
TST_CTRL	0x40030000
TST_ADFT_CTRL	0x40030004
TST_DDFT_CTRL	0x40030008
TST_ADFT_TSG4_A	0x4003000C
TST_ADFT_TSG4_B	0x40030010
TST_MODE	0x40030014
TST_TRIM_CNTR1	0x40030018
TST_TRIM_CNTR2	0x4003001C

15.1.1 TST_CTRL

Address: 0x40030000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	None	R	R	R	R	R	R	R
SW Access	None	RW	RW1S	RW	RW	RW	RW	RW
Bit Name	Reserved	TST_PTM_MODE_EN	TST_SCAN_MODE	TST_SCAN_COMPRESS	TST_SCAN_IDDQ	TST_SCAN_TRF	TST_SCAN_TRF1	TST_SCAN_OCC_OBSERVE

Bits	23	22	21	20	19	18	17	16
Reset Value	None					0x0	0x0	0x0
HW Access	None					R	R	R
SW Access	None					RW	RW	RW
Bit Name	Reserved[23:19]					TST_TEST_SPARE2_EN	TST_TEST_SPARE1_EN	TST_TEST_SYSRETAIN_EN

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
HW Access	R	R	R	R	R	R	R	R
SW Access	RW	RW	RW	RW	RW	RW	RW	RW
Bit Name	TST_TEST_SLPRETAIN_EN	TST_TEST_SYSISOLATE_EN	TST_TEST_SLPISOLATE_EN	TST_TEST_OCC0_2_EN_N	TST_TEST_OCC0_1_EN_N	TST_TEST_ICG_EN_N	TST_TEST_SET_EN_N	TST_TEST_RESET_EN_N

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	0x0	0x0
HW Access	None					RW	R	R
SW Access	None					R	RW1S	RW1S
Bit Name	Reserved[7:3]					TST_SWD_CONNECT-ED	TST_DAP_NO_DEBUG	TST_DAP_NO_ACCESS

Main Test Control Register

Bits	Name	Description
30	TST_PTM_MODE_EN	0: PTM interface disabled 1: PTM interface enabled (only when SCAN_MODE=0) Default: 0x0

15.1.1 TST_CTRL (continued)

29	TST_SCAN_MODE	0: Normal (non-scan) mode 1: Scan mode enabled Setting this bit will cause scan mode to activate, after which SWD ports stops operating (it is itself scannable) and no other register accesses can be made. This bit will override PTM_MODE_EN when set. Default: 0x0
28	TST_SCAN_COMPRESS	0: Uncompressed scan test 1: Compressed scan test Default: 0x0
27	TST_SCAN_IDDQ	0: Normal scan test 1: IDDQ scan test (can be used concurrent with SCAN_COMPRESS but not SCAN_TRF). Default: 0x0
26	TST_SCAN_TRF	0: Normal (SAF/IDDQ) scan test 1: Transition Fault scan test (can be used concurrent with SCAN_COMPRESS but not SCAN_IDDQ). Default: 0x0
25	TST_SCAN_TRF1	0: Do not include lt;48MHz logic in TRF when SCAN_TRF=1 1: Include lt;48MHz logic in TRF when SCAN_TRF=1 Default: 0x0
24	TST_SCAN_OCC_OBSERVE	0: Normal scan mode 1: Bring out OCC clock on scan_out[0] Default: 0x0
18	TST_TEST_SPARE2_EN	Enable bit for spare signal in scan control chain. See SAS for more details. Default: 0x0
17	TST_TEST_SPARE1_EN	Enable bit for spare signal in scan control chain. See SAS for more details. Default: 0x0
16	TST_TEST_SYSRETAIN_EN	Enable sleepb test points for retention registers in Active domain. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
15	TST_TEST_SLPRETAIN_EN	Enable sleepb test points for retention registers in DeepSleep domain. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
14	TST_TEST_SYSISOLATE_EN	Enable sleep test points in Active domain. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
13	TST_TEST_SLPISOLATE_EN	Enable sleep test points in DeepSleep domain. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
12	TST_TEST_OCC0_2_EN_N	Enable the OCC test point of Bit 2 in TRF mode. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
11	TST_TEST_OCC0_1_EN_N	Enable the OCC test point of Bit 1 in TRF mode. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
10	TST_TEST_ICG_EN_N	Enable clock gater test points during scan. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0

15.1.1 TST_CTRL (continued)

9	TST_TEST_SET_EN_N	Enable async set test points during scan. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
8	TST_TEST_RESET_EN_N	Enable async reset test points during scan. This bit is further gated using a scan control chain. See SAS for more details. Default: 0x0
2	TST_SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset Connect sequence passed) (Note this bit is duplicated in TST_MODE.SWD_CONNECTED for user mode access) Default: 0x0
1	TST_DAP_NO_DEBUG	1: Block all AHB accesses to CM0 Debug (PPB) Registers (effectively disabling debugger capability). Default: 0x0
0	TST_DAP_NO_ACCESS	1: Block all AHB accesses from SWD port (effectively disabling it) Default: 0x0

15.1.2 TST_ADFT_CTRL

Address: 0x40030004

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	TST_ENABLE	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[7:0]							

Analog DFT Control Register

Bits	Name	Description
31	TST_ENABLE	Enables ADFT functionality. Must be set for any of the ADFT switches and muxes to operate. Default: 0x0

15.1.3 TST_DDFT_CTRL

Address: 0x40030008

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	0x0		0x0	None			
HW Access	R	R		R	None			
SW Access	RW	RW		RW	None			
Bit Name	TST_ENABLE	TST_DIVIDE [30:29]		TST_EDGE	Reserved[27:24]			

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[15:14]		TST_DFT_SEL2 [13:8]					

Bits	7	6	5	4	3	2	1	0
Reset Value	None		0x00					
HW Access	None		R					
SW Access	None		RW					
Bit Name	Reserved[7:6]		TST_DFT_SEL1 [5:0]					

Digital DFT Control Register

Bits	Name	Description
31	TST_ENABLE	1: Enables DDFT functionality. Connects output of DDFT mux to designated DDFT pin. Default: 0x0
30 : 29	TST_DIVIDE	Controls in-line divider for DDFT output #1 (used for high-speed clock measurements). Default: 0x0 **0x0: DIRECT** Connect output directly **0x1: DIV_BY_2** Divide output by 2

15.1.3 TST_DDFT_CTRL (continued)

		0x2: DIV_BY_4 Divide output by 4 **0x3: DIV_BY_8** Divide output by 8
28	TST_EDGE	Edge sensitivity for in-line divider on DDFT output #1 (only relevant when DIVIDEgt;0). Default: 0x0 **0x0: POSEDGE** Use posedge for divider **0x1: NEGEDGE** Use negedge for divider
13 : 8	TST_DFT_SEL2	Select signal for DDFT output #2 Default: 0x00 **0x00: VSS** Vss **0x01: CLK1** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x02: CLK2** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x03: PWR1** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x04: PWR2** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x05: VMON** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x06: TSS_VDDA_OK** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x07: ADFT_TRIP1** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x08: ADFT_TRIP2** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments **0x09: TSS1** Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

15.1.3 TST_DDFT_CTRL (continued)

0x0A: TSS2
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0B: TSS3
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0C: TSS4
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0D: I2CS_CLK_I2CS
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0E: I2CS_SDAIN_SI
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

5 : 0 TST_DFT_SEL1 Select signal for DDFT output #1
Default: 0x00

0x00: VSS
Vss

0x01: CLK1
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x02: CLK2
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x03: PWR1
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x04: PWR2
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x05: VMON
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x06: TSS_VDDA_OK
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x07: ADFT_TRIP1
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x08: ADFT_TRIP2
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x09: TSS1
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

15.1.3 TST_DDFT_CTRL (continued)

0x0A: TSS2
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0B: TSS3
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0C: TSS4
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0D: I2CS_CLK_I2CS
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

0x0E: I2CS_SDAIN_SI
Refer to M0S8-MemoryMap.xls Tab: DDFT Assignments

15.1.4 TST_ADFT_TSG4_A

Address: 0x4003000C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None			0x0			0x0	
HW Access	None			R			R	
SW Access	None			RW			RW	
Bit Name	Reserved[23:21]			TST_ADFT_MUX_SEL_7 [20:18]			TST_ADFT_MUX_SEL_6 [17:15]	

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0	0x0			0x0			0x0
HW Access	R	R			R			R
SW Access	RW	RW			RW			RW
Bit Name	TST_ADFT_MUX_SEL_6 [17: 15]	TST_ADFT_MUX_SEL_5 [14:12]			TST_ADFT_MUX_SEL_4 [11:9]			TST_ADFT_MUX_SEL_3 [8:6]

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x0			0x0		
HW Access	R		R			R		
SW Access	RW		RW			RW		
Bit Name	TST_ADFT_MUX_SEL_3 [8: 6]		TST_ADFT_MUX_SEL_2 [5:3]			TST_ADFT_MUX_SEL_1 [2:0]		

ADFT Multiplexers

Bits	Name	Description
20 : 18	TST_ADFT_MUX_SEL_7	ADFT Mux 7. Connects inputs to ADFT bus lv_d. Default: 0x0 **0x0: NC0** All the switches inside ADFT mux7 are open **0x1: IN1** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

15.1.4 TST_ADFT_TSG4_A (continued)

0x2: IN2
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x3: IN3
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x4: IN4
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x5: IN5
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x6: IN6
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x7: NC7
All the switches inside ADFT mux7 are open

17 : 15	TST_ADFT_MUX_SEL_6	ADFT Mux 6. Connects inputs to ADFT bus hv_d. Default: 0x0

0x0: NC0
All the switches inside ADFT mux6 are open

0x1: IN1
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x2: IN2
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x3: IN3
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x4: IN4
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x5: IN5
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x6: IN6
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x7: NC7
All the switches inside ADFT mux6 are open

14 : 12	TST_ADFT_MUX_SEL_5	ADFT Mux 5. Connects inputs to ADFT bus lv_d. Default: 0x0

15.1.4 TST_ADFT_TSG4_A (continued)

0x0: NC0
All the switches inside ADFT mux5 are open

0x1: IN1
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x2: IN2
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x3: IN3
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x4: IN4
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x5: IN5
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x6: IN6
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x7: NC7
All the switches inside ADFT mux5 are open

11 : 9	TST_ADFT_MUX_SEL_4	ADFT Mux 4. Connects inputs to ADFT bus hv_alt;1gt;. Default: 0x0

0x0: NC0
All the switches inside ADFT mux4 are open

0x1: IN1
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x2: IN2
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x3: IN3
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x4: IN4
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x5: IN5
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

0x6: IN6
Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

15.1.4 TST_ADFT_TSG4_A (continued)

		0x7: NC7 All the switches inside ADFT mux4 are open
8 : 6	TST_ADFT_MUX_SEL_3	ADFT Mux 3. Connects inputs to ADFT bus hv_alt;1gt;. Default: 0x0 **0x0: NC0** All the switches inside ADFT mux3 are open **0x1: IN1** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x2: IN2** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x3: IN3** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x4: IN4** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x5: IN5** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x6: IN6** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x7: NC7** All the switches inside ADFT mux3 are open
5 : 3	TST_ADFT_MUX_SEL_2	ADFT Mux 2. Connects inputs to ADFT bus hv_alt;0gt;. Default: 0x0 **0x0: NC0** All the switches inside ADFT mux2 are open **0x1: IN1** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x2: IN2** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x3: IN3** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x4: IN4** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments

15.1.4 TST_ADFT_TSG4_A (continued)

		0x5: IN5 Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x6: IN6** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x7: NC7** All the switches inside ADFT mux2 are open
2 : 0	TST_ADFT_MUX_SEL_1	ADFT Mux 1. Connects inputs to ADFT bus hv_alt;0gt;. Default: 0x0 **0x0: NC0** All the switches inside ADFT mux1 are open **0x1: IN1** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x2: IN2** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x3: IN3** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x4: IN4** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x5: IN5** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x6: IN6** Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments **0x7: NC7** All the switches inside ADFT mux1 are open

15.1.5 TST_ADFT_TSG4_B

Address: 0x40030010

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0		0x0		0x0		0x0	
HW Access	R		R		R		R	
SW Access	RW		RW		RW		RW	
Bit Name	TST_ADFT_MUX_SEL_14 [7:6]		TST_ADFT_MUX_SEL_13 [5:4]		TST_ADFT_MUX_SEL_12 [3:2]		TST_ADFT_MUX_SEL_11 [1:0]	

ADFT Multiplexers

Bits	Name	Description
7 : 6	TST_ADFT_MUX_SEL_14	ADFT Mux 14. Connects outputs to ADFT bus. Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments for which bus connects to which ADFT mux Default: 0x0 **0x0: NC0** All the switches inside ADFT mux14 are open **0x1: IN1** Route ADFT bus line to adft1 **0x2: IN2** Route ADFT bus line to adft2

15.1.5 TST_ADFT_TSG4_B (continued)

		0x3: NC3 All the switches inside ADFT mux14 are open
5 : 4	TST_ADFT_MUX_SEL_13	ADFT Mux 13. Connects outputs to ADFT bus. Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments for which bus connects to which ADFT mux Default: 0x0 **0x0: NC0** All the switches inside ADFT mux13 are open **0x1: IN1** Route ADFT bus line to adft1 **0x2: IN2** Route ADFT bus line to adft2 **0x3: NC3** All the switches inside ADFT mux13 are open
3 : 2	TST_ADFT_MUX_SEL_12	ADFT Mux 12. Connects outputs to ADFT bus. Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments for which bus connects to which ADFT mux Default: 0x0 **0x0: NC0** All the switches inside ADFT mux12 are open **0x1: IN1** Route ADFT bus line to adft1 **0x2: IN2** Route ADFT bus line to adft2 **0x3: NC3** All the switches inside ADFT mux12 are open
1 : 0	TST_ADFT_MUX_SEL_11	ADFT Mux 11. Connects outputs to ADFT bus. Refer to M0S8-MemoryMap.xls Tab: ADFT Assignments for which bus connects to which ADFT mux Default: 0x0 **0x0: NC0** All the switches inside ADFT mux11 are open **0x1: IN1** Route ADFT bus line to adft1 **0x2: IN2** Route ADFT bus line to adft2 **0x3: NC3** All the switches inside ADFT mux11 are open,

15.1.6 TST_MODE

Address: 0x40030014

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x0	None						
HW Access	R	None						
SW Access	RW	None						
Bit Name	TST_TEST_MODE	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[15:8]							

Bits	7	6	5	4	3	2	1	0
Reset Value	None					0x0	None	
HW Access	None					RW	None	
SW Access	None					R	None	
Bit Name	Reserved[7:3]					TST_SWD_CONNECT-ED	Reserved[1:0]	

Test Mode Control Register

Bits	Name	Description
31	TST_TEST_MODE	0: Normal operation mode 1: Test mode (any test mode) Setting this bit will prevent BootROM from yielding execution to Flash image. Default: 0x0
2	TST_SWD_CONNECTED	0: SWD not active 1: SWD activated (Line Reset Connect sequence passed) (Note: this bit is a duplicate of TST_CTRL.SWD_CONNECTED and is present in all M0S8 products except TSG4) Default: 0x0

15.1.7 TST_TRIM_CNTR1

Address: 0x40030018

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x1	None						
HW Access	W	None						
SW Access	R	None						
Bit Name	TST_COUNTER_DONE	Reserved[30:24]						

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	RW							
SW Access	RW							
Bit Name	TST_COUNTER [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	RW							
SW Access	RW							
Bit Name	TST_COUNTER [15: 0]							

IMO trim down-counter and status (clk_sys)

Bits	Name	Description
31	TST_COUNTER_DONE	Status bit indicating that TRIM_CNTR1.COUNTER==0 and TRIM_CNT2.COUNTER stopped counting up Default: 0x1
15 : 0	TST_COUNTER	Down-counter clocked on clk_sys. By writing non-zero value to this counter TRIM_CNTR2.COUNTER clears and counts up. TRIM_CNTR1.COUNTER counts down until TRIM_CNTR1.COUNTER==0 Default: 0x0000

15.1.8 TST_TRIM_CNTR2

Address: 0x4003001C

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[31:24]							

Bits	23	22	21	20	19	18	17	16
Reset Value	None							
HW Access	None							
SW Access	None							
Bit Name	Reserved[23:16]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	TST_COUNTER [15:0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x0000							
HW Access	RW							
SW Access	R							
Bit Name	TST_COUNTER [15: 0]							

IMO trim up-counter (ddft)

Bits	Name	Description
15 : 0	TST_COUNTER	Up-counter clocked on DDFT output #2. When TRIM_CNTR1.COUNT_DONE==1 counter stopped and can be read by SW Default: 0x0000

16 UDB Registers

This section discusses the UDB registers of PSoC 4 device. It lists all the registers in mapping tables, in address order.

16.1 UDB Register Mapping Overview

Register Name	Address
UDB_INT_CFG	0x400F8000

16.1.1 UDB_INT_CFG

Address: 0x400F8000

Retention: Retained

Bits	31	30	29	28	27	26	25	24
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	UDB_INT_MODE_CFG [31:0]							

Bits	23	22	21	20	19	18	17	16
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	UDB_INT_MODE_CFG [31: 0]							

Bits	15	14	13	12	11	10	9	8
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	UDB_INT_MODE_CFG [31: 0]							

Bits	7	6	5	4	3	2	1	0
Reset Value	0x00000000							
HW Access	R							
SW Access	RW							
Bit Name	UDB_INT_MODE_CFG [31: 0]							

UDB Subsystem Interrupt Configuration

Bits	Name	Description
31 : 0	UDB_INT_MODE_CFG	Interrupt Mode; bit position corresponds to interrupt Default: 0x00000000 **0x00000000: LEVEL** Level **0x00000001: PULSE** Pulse

Revision History

Revision History

Document Title: PSoC 4100/4200 Family PSoC® 4 Registers TRM (Technical Reference Manual) Document Number: 001-85847				
Revision	**ECN#**	**Issue Date**	**Origin of Change**	**Description of Change**
**	3971396	04/17/2013	OWEN	New TRM