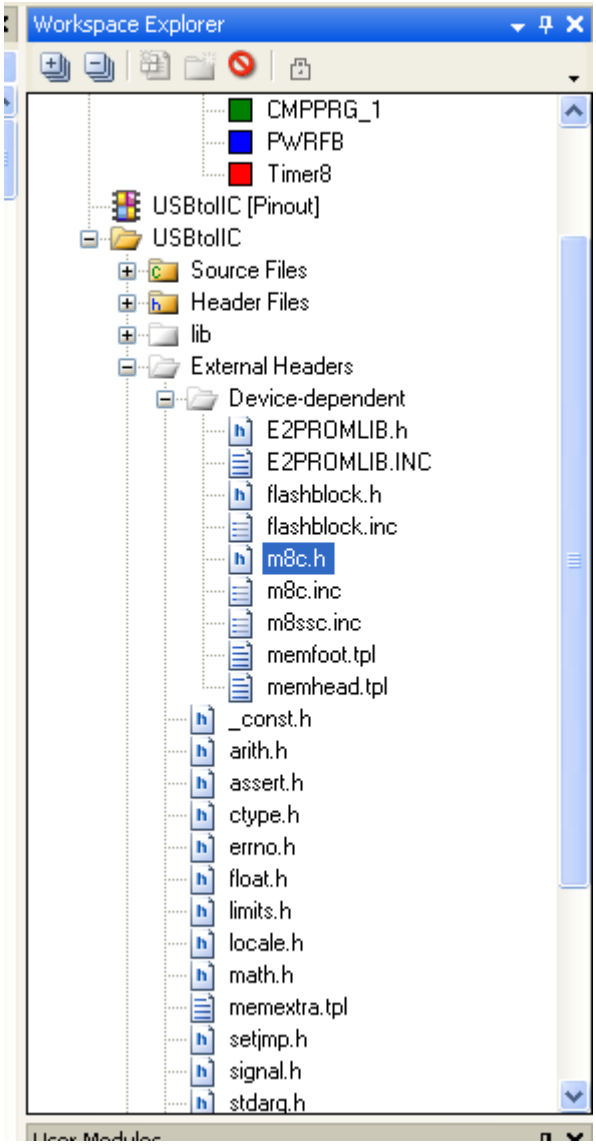
**Location of m8c.h – Source Files/External Headers/Device-dependent**



**Definition of the registers and bits of PSoC 1 in m8c.h**

Start Page | USBtoIIC [Chip] | main.c | **m8c.h**

```
298
299 //-------------------------------------------------
300 //  Analog Control Registers
301 //-------------------------------------------------
302
303 #pragma  ioport    AMX_IN:      0x060  // Analog Input Multiplexor Control
304 BYTE               AMX_IN;
305 #define AMX_IN_ACI1        (0x0C)
306 #define AMX_IN_ACIO        (0x03)
307
308 #pragma  ioport    AMUXCFG:     0x061  // Analog MUX Configuration
309 BYTE               AMUXCFG;
310 #define AMUXCFG_BCOL1MUX   (0x80)
311 #define AMUXCFG_ACOLOMUX   (0x40)
312 #define AMUXCFG_INTCAP     (0x30)
313 #define AMUXCFG_MUXCLK     (0x0E)
314 #define AMUXCFG_EN         (0x01)
315
316 #pragma  ioport    ARF_CR:      0x063  // Analog Reference Control Register
317 BYTE               ARF_CR;
318 #define ARF_CR_HBE       (0x40)
319 #define ARF_CR_REF       (0x38)
320 #define ARF_CR_REFPWR    (0x07)
321 #define ARF_CR_SCPWR     (0x03)
322
323 #pragma  ioport    CMP_CR0:     0x064  // Analog Comparator Bus Register 0
324 BYTE               CMP_CR0;
325 #define CMP_CR0_COMP1     (0x20)
326 #define CMP_CR0_COMP0     (0x10)
327 #define CMP_CR0_AINT1     (0x02)
328 #define CMP_CR0_AINT0     (0x01)
329
330 #pragma  ioport    ASY_CR:      0x065  // Analog Synchronizaton Control Register
331 BYTE               ASY_CR;
332 #define ASY_CR_SARCOUNT (0x70)
333 #define ASY_CR_SARSIGN   (0x08)
334 #define ASY_CR_SARCOL    (0x06)
335 #define ASY_CR_SYNCEN    (0x01)
336
337 #pragma  ioport  CMP_CR1:     0x066   // Analog Comparator Bus Register 1
338 BYTE             CMP_CR1;
```