DDS24 custom component Application Note
0.0

AN-DDS24_00_A

DDS24 basic applications

Associated Project: Yes
Associated Part Family: PSoC5LP
Software version: PSoC® Creator™ 3.3 SP1
Related application Notes: DDS24 datasheet

This application note comments several basic examples using custom DDS24 component. Projects presented show various modes of operation of the component, including tunable frequency and phase using API and digital input and output buses.

Projects described in this AN:

1. Sweep generator using API control.
2. Sweep generator with hardware load.
3. Voltage ramp generator.
4. Triangle wave generator.
5. Arbitrary wave generator.
6. Voltage controlled oscillator (VCO).
7. Frequency shifter (upconverter).
8. Hardware controlled sweep generator.
9. Frequency chirp generator.
10. Frequency sweep oscillator.

Introduction

DDS24 component allows for easy generation of tunable frequency using PSoC5LP. Presented below are some application ideas utilizing the component. Several basic projects are provided alongside the Application Note.

Advanced demos: sine wave generator, lock-in detector, phase-locked loop (PLL), AM and FM modulators, FSK/PSK modulators are not included in this Application Note.

It should be clear that DDS24 component is not a substitute to the commercially manufactured DDS chips, and can't compete with them in performance and features. Due to the limited UDB resources available on PSoC, many standard DDS features can't be implemented or had to be scaled down considerably. Benefits of using the component is that it fits PSoC ecosystem and may save external parts for non-demanding applications. The component may also have its niche as educational resource and as part of the PSoC Community Components library.

Advantages of using DDS24 are: possibility to set output frequency directly; same (high) resolution over entire frequency range; readily available harmonics of the prime frequency; synchronous reference output with tunable phase delay; options for API or digital bus control.

As provided, for demonstration purposes projects are configured to operate at slow frequencies. Since DDS24 implemented in UDB, they also can operate in high-speed real-time domain (MHz-scale, please refer to DDS24 datasheet for practical limits).

Examples were developed using FreeSoC board having CY8C5868AXI-LP035 chip, and selectively tested using CY8CKIT-059 PSoC5LP Prototyping Kit. Depending on prototyping board available, pins may have to be reassigned. For portability, all examples have their master clock derived from the IMO, which has relatively low stability (>0.01%). If board equipped with crystal oscillator (XO), configure it as a source for the master clock for stable (ppm) frequency output.

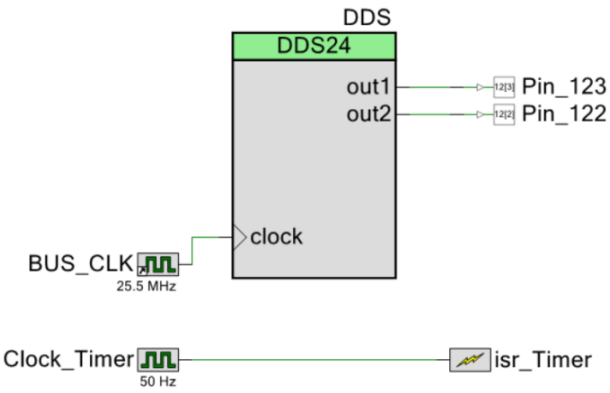

Figure 1. Updating DDS settings via API calls.

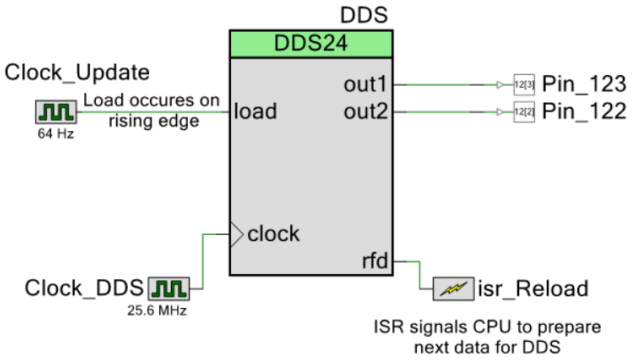

Figure 2. Updating DDS settings on hardware load.

Sweep generator with API control.

Associated project[(*)]: DDS24_sw

Example of sweep frequency/phase generator using DDS24 API functions to update control parameters. Here the update rate is set by the Clock_Timer triggering interrupt, which signals CPU to update DDS parameters. The resulting frequency and phase sweeps are shown on the accompanying video, available online. This is the simplest mode of DDS24 component use. It may be useful for stimulus-response type applications, where response data is being collected after new DDS parameters are set.

Supplementary project: DDS24_encoder.

Example of manually tunable frequency/phase generator using rotary encoder with a switch button. Switch button is used to select between frequency and phase parameter to be updated, while encoder is used to change the value using API call.

Sweep generator with hardware load.

Associated project: DDS2_hw

Sweep frequency generator demo with hardware controlled update of the frequency and phase. In this mode DDS parameters are being written to the control registers using API calls (CPU domain), but their update occurs only on hardware controlled strobe signal (real-time digital domain). Once new data has been loaded, the ready-for-data ("rfd") output triggers the interrupt (isr_Reload) signaling CPU to prepare fresh parameters for the next step.

This mode of operation allows maintaining deterministic timing at much higher update rates (>10 kHz) as compared to simple API update.

[*] Associated video: https://youtu.be/TlcyHED8B5c

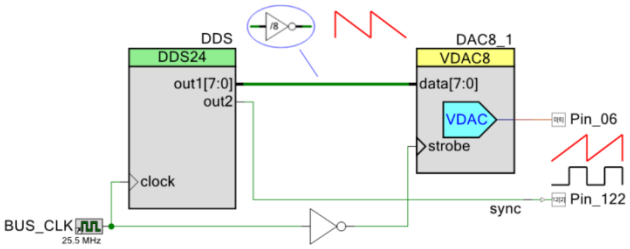

Figure 3. Voltage ramp generator.

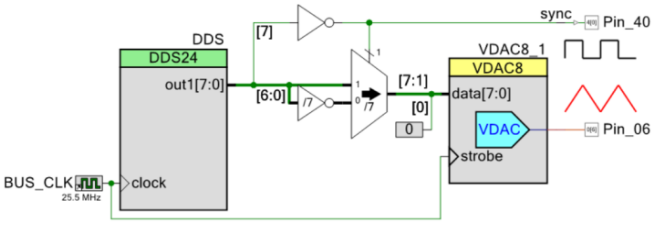

Figure 4. Triangle wave generator.

Voltage ramp generator.

Associated project: DDS24_ramp

Voltage ramp (sawtooth) generator demo using DDS output bus for VDAC control. This is basic example of generating analog waveform without a lookup table. Add NOT8 element to invert the slope of the ramp. Optional NOT element on the VDAC strobe may improve VDAC sampling at high frequencies (>100 kHz) by adding ½ clock delay.

Triangle wave generator.

Associated project: DDS24_triangle

Triangle wave generator demo using DDS output bus for VDAC control. The hardware mux inverts bits [6:0] providing 128 steps for positive and negative slopes of the triangle waveform. The MSB of out1 controls the slope sign and provides synchronous reference. Unused LSB of VDAC input is terminated with “0”.

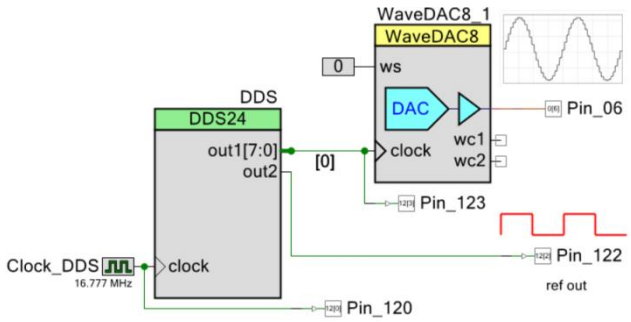

Figure 5. Arbitrary wave generator.

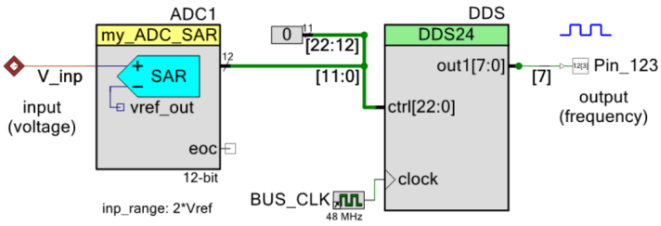

Figure 6. Voltage controlled oscillator (VCO).

Arbitrary wave generator.

Associated project: DDS24_wDAC

Arbitrary wave generator demo using DDS24 as sampling clock for WaveDAC8. The wave source is provided by the WaveDAC8, with number of points per period set to 128. The WaveDAC8 sampling clock is derived from the LSB of the DDS bus, oscillating at the 128x rate of the DDS set frequency. This ensures that output wave (sine) frequency exactly equals the DDS set frequency. As shown, the WaveDAC8 output frequency resolution is 1 Hz (limited by DDS clock), and maximum frequency attainable is about 17 kHz, limited by the bus clock (66 MHz), DMA transfer rate (~14 bus clocks), and number of points per period (128). DDS out2 provides synchronous reference with optional phase shift.

Voltage controlled oscillator.

Associated project: DDS24_VCO

Voltage controlled oscillator (VCO) demo using DDS24 and ADC_SAR. For this demo ADC_SAR has been modified, providing access to its internal 12-bit digital output bus. This bus directly feeds DDS with tuning word, proportional to the ADC input voltage. In result, DDS output frequency is directly proportional to ADC input voltage. The VCO transfer coefficient can be adjusted from approx. 5 kHz/V to 1.5 MHz/V by selecting ADC input scale, DDS clock frequency and by shifting DDS control bits. As shown:

$$K_{VCO} = \frac{4095}{2.048\ V} * \frac{48\ MHz}{2^{24}} = 5.72\ kHz/V$$

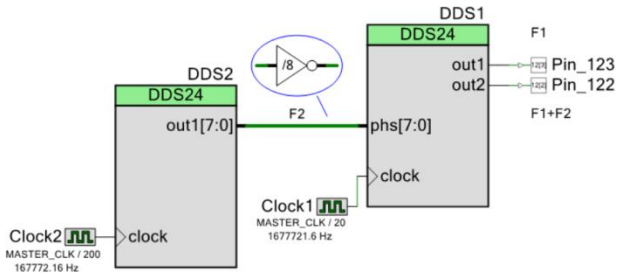

Figure 6. Frequency upconverter.

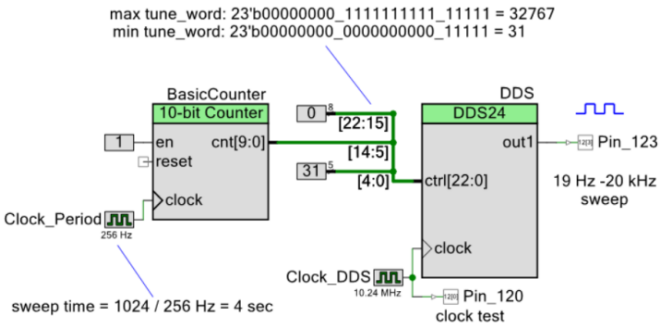

Figure 7. Hardware controlled sweep generator.

Frequency shifter (upconverter).

Associated project: DDS24_upconv

Frequency upconverter demo using two DDS modules. Output frequency F_1 on Pin_123 is set by DDS1 (the carrier frequency). DDS2 provides modulation frequency (F_2). The output frequency on Pin_122 is a sum of the F_1 and F_2. Such arrangement can be used for producing frequency modulated (FM) output. In this example the modulation frequency F2=0.02 Hz is deliberately set below DDS1 step resolution (0.1 Hz), while still producing correct output: F_1=10000 Hz, F_2 = 0.02 Hz, F_out2 = 10000.02 Hz.

Frequency downconvertion (F_1-F_2) can be achieved by flipping control bus bits using NOT8 element.

Sweep generator with hardware control.

Associated project: DDS24_sweep_hw

This design idea demonstrates all-hardware controlled frequency sweep generator using DDS digital control bus. DDS output frequency is swept in 1024 steps from 19 Hz to 20 kHz. The number of steps and sweep period are defined by the bit width of the BasicCounter and counter's sampling clock. DDS starting and ending frequencies are defined by the MSBs and LSBs constants of the control bus and DDS sampling clock (10.24 MHz):

$$tw_{min} = 23'b00000000\_0000000000\_11111 = 31$$

$$tw_{max} = 23'b00000000\_1111111111\_11111 = 32767$$

$$F_{min} = 31/2^{24} * 10.24\ MHz = 19\ Hz$$

$$F_{max} = 332767/2^{24} * 10.24\ MHz = 20\ kHz$$

The tuning range is not quite flexible, but it conveniently covers spectrum from 19 Hz to 20 kHz, which may come handy for audio applications. This sweep generator does not consume CPU resources.

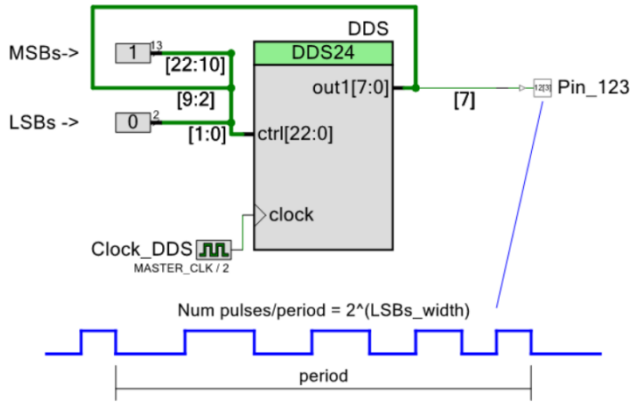

Figure 9. Frequency chirp generator.

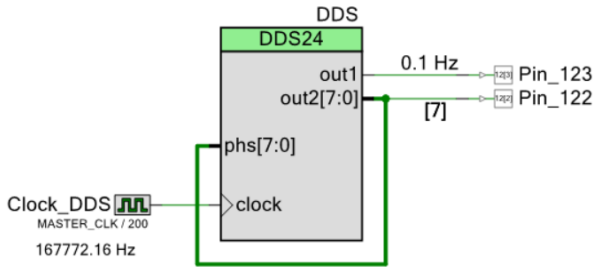

Figure 10. Hardware controlled sweep generator.

Frequency chirp generator.

Associated project: DDS24_chirp

Frequency chirp demo using digital bus control with feedback. Digital feedback loop ramps up tuning word, producing frequency chirp. MSBs and LSBs control starting and ending frequencies, pattern period and number of pulses per period ($N = 2^{LSB\_width}$), see project for details. Output spectrum observed for LSBs = [5:0] is flattop from 1 MHz to 2 MHz (Figure 10).

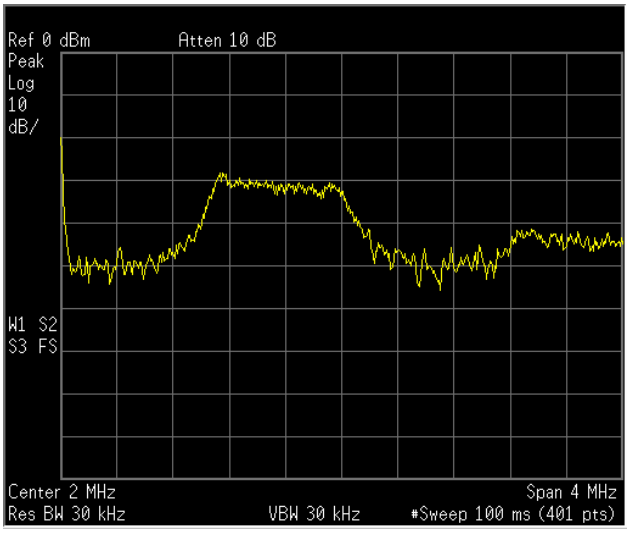

Figure 11. Observed spectrum for LSBs = [5:0].

Frequency sweep oscillator.

Associated project: DDS24_sweep_osc

Curious case of DDS with phase feedback loop, resulting in oscillating frequency sweeps (Figure 12). DDS out2 frequency oscillates between 0 to Clock/2 with step size Clock/256. The pattern period is defined by DDS set frequency (0.1 Hz): T = $(F_{set})^{-1}$ = 10 sec.

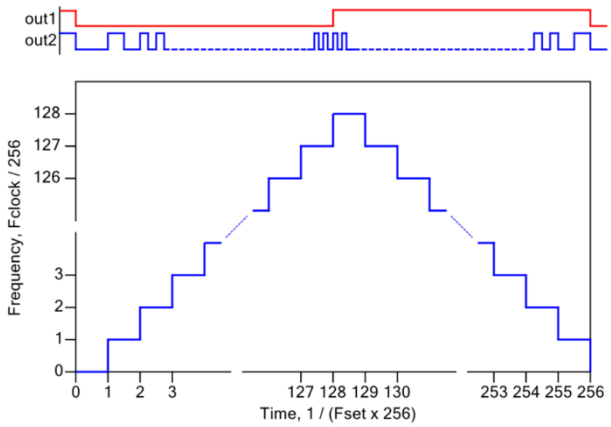

Figure 12. Top: Time diagram of out1 and out2. Bottom: out2 frequency vs. time (within single period).

Summary.

This application note provides overview of possibilities and gives several basic examples of DDS24 component utilization.