Signal Rectifier Using PSoC® 1

CE52251

Code Example Name: Example_Signal_Rectifier
Programming Language: Assembly
Associated Part Families: CY8C24x23, CY8C27x43, CY8C29x66, CY8C24x94
Software Version: PSoC® Designer 5.1 (FCS)
Related Hardware: CY3210 PSoC Eval1
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Objective

CE52251 builds a full wave signal rectifier using PSoC® analog resources.

Overview

Analog signal is fed to a unity gain PGA and to a Comparator which is configured as a Zero Crossing Detector, and a SC Block, which is configured as a modulator. The output of the comparator is used to modulate the sign of the SC Block that converts the AC input signal to full wave rectified output.

User Module List and Placement

The following table lists user modules used in this code example and the hardware resources occupied by each user module.

User Module	Placement
PGA_1	ACB00
CMPPRG_1	ACB01
RefMux_1	ACB02
SCBLOCK_1	ASC10
DigBuf_1	DBB00

User Module Parameter Settings

The following tables show the user module parameter settings for each of the user modules used in the code example.

PGA_1		
Parameter	**Value**	**Comments**
Gain	1.000	The PGA is configured as unity gain amplifier.
Input	AnalogColumn_InputMUX_0	Input from P0[1] is connected from AnalogColumn_InputMux0
Reference	AGND	The PGA is referenced to Analog Ground
AnalogBus	Disable	The analog output is not used. The output of the PGA is internally connected to the SC Block

Note Amplification and rectification can be performed for small signals by setting the gain of the PGA to more than 1.

SCBLOCK_1		
Parameter	**Value**	**Comments**
FCap	16	Feedback capacitor
ClockPhase	Norm	
ASign	Neg	This value is XOR'ed with the hardware modulator signal from the CMPPRG to decide the sign of the SC Block
ACap	16	Gain is ACap / Fcap = 1
ACMux	ACB00	Output of PGA (Buffer) is routed to SCBLOCK's I/P
BCap	0	
AnalogBus	AnalogOutBus_0	SCBLOCK (Rectifier) O/P is routed to P0.3
CompBus	Disable	
AutoZero	On	Auto Zero is enabled
CCap	0	
ARefMux	AGND	The input is referenced to AGND
FSW1	On	Phase-2 switch in Fcap is enabled
FSW0	On	Phase-1 switch in Fcap is enabled
BMux		Bmux is not used
Power	High	SCBLOCK set for full power

Notes

- The column clock decides the over sampling ratio of the SC block. The data clock to the SC Block is a quarter of the column clock. For a column clock of 2 MHz, the data clock is 500 KHz. For a 1 KHz input signal and 500 KHz of data clock, the over sampling ratio is 500. When the input frequency increases, the over sampling ratio reduces. These are seen as discreet steps on the output. For a smoother output, higher oversampling ratio should be used. However, the column clock should not exceed the maximum column clock limit for the operating power as specified in the SC Block data sheet
- Setting the Sign parameter to positive results in a full wave rectified signal with negative polarity.
- AN2041 – Understanding Switched Capacitor Blocks explains in detail the principles of an SC Block and the meaning of the above parameters.

RefMux_1		
Parameter	**Value**	**Comments**
Reference Selection	AGND	Used to route AGND to P0[4]

CMPPRG_1		
Parameter	**Value**	**Comments**
AnalogBus	Disable	
CompBus	ComparatorBus_1	
Input	ACB00	Input to the Comparator comes from the PGA
LowLimit	VSS	
RefValue	0.500	The Low Limit and RefValue set the threshold of CMPPRG to VDD/2

DigBuf_1		
Parameter	**Value**	**Comments**
DefaultLoadStatus	Enable	The DigBuf is enabled by default and does not require a DigBuf_1_Start function call
Input1	ComparatorBus_1	The output of the ZCD is the input to DigBuf
Input2		Not used
Input2ClockSync		Not used
Output1	Row_0_Output_0	Output is taken to P1[4] through Row_0_Output_0
Output2		Not used
InvertInput1	Normal	Input1 is not inverted

Note
The DigBuf is used only to bring out the Comparator Bus signal to an output pin. This is only for debugging purpose and is not required for normal operation of the rectifier.

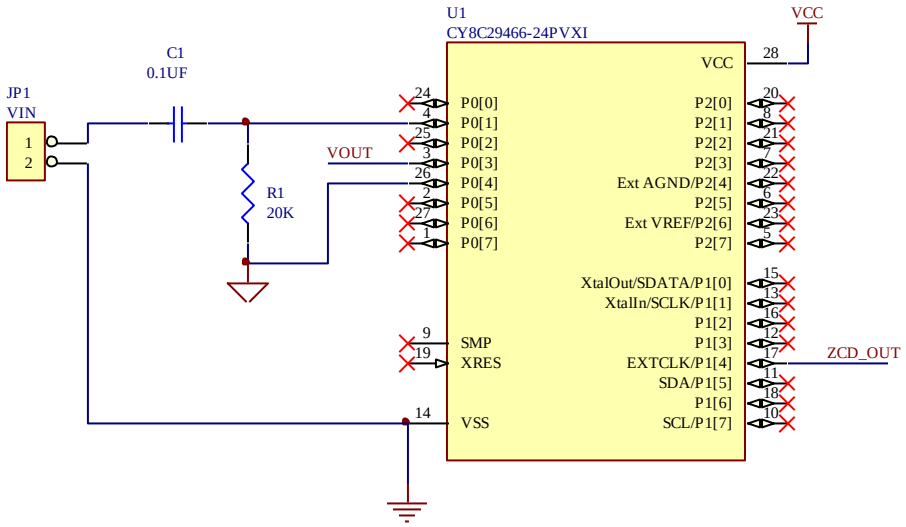
Global Resources

Important Global Resources		
Parameter	**Value**	**Comments**
Analog Power	SC On / Ref High	Switched Capacitor blocks On, Reference at High Power
VC1	12	VC1 generates 2 MHz column clock to the SC Block

Hardware Connections

The hardware is shown in the following schematic diagram.

Figure 1. Example Schematic Diagram



The Analog Ground (AGND) is brought out on P0[4] and the input signal which is referenced to VSS is biased to AGND using C1-R1. The rectified output signal is available on P0[3]. The comparator bus output from the CMPPRG is brought out on P1[4]. This output is only for debugging and is not required for the normal operation of the example.

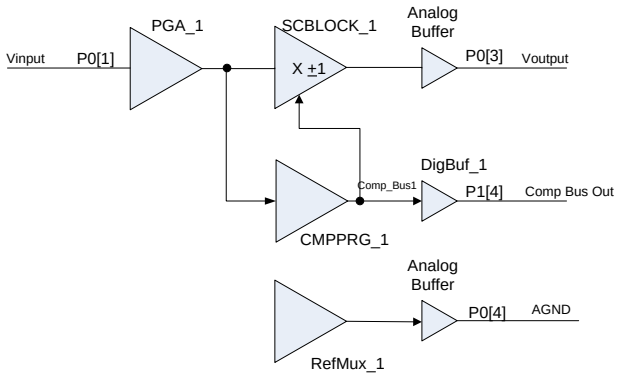
The example can be tested using the CY3210 – PsoC Eval1 board. The following connections may be made on the CY3210 board:

- Use the bread board area of the CY3210 to assemble R1 and C1.
- Connect the input signal after the RC network to P0[1] on J6.
- The rectified output is available on P0[3] on J6.
- The AGND is available on P0[4] on J6.
- Observe the comparator bus output on P1[4] on J7.

Operation

The block diagram of the PSoC device configuration is shown in the following figure.

Figure 2. PSoC Device Configurations



The rectifier works in the following manner:

- A RefMux user module placed in ACB02 is used to bring the AGND to P0[4].
- The input signal referenced to AGND is fed to a PGA placed in ACB00, configured as a unity gain amplifier.
- The output of the PGA feeds a CMPPRG placed in ACB01 and an SCBLOCK placed in ASC10.
- The CMPPRG is configured as a Zero crossing detector with its threshold set at AGND, which is 2.5V. The output of the CMPPRG is high when input signal is positive and low when the input signal is negative.
- The SCBLOCK is configured as a unity gain amplifier by selecting Fcap = Acap = 16.
- The modulation source of the Rectifier is set to Comparator_Bus_1.
- The “Sign” parameter of the SCBLOCK and the Comparator Bus output are XOR’ed and the result sets the sign of the SCBLOCK. As the “Sign” parameter of the SC Block is set to “Negative”, a HIGH from the CMPPRG results in a positive sign and LOW results in a negative sign.
- When the input signal is positive, the output of CMPPRG is HIGH; the sign is positive and hence the output is also positive.
- When the input signal goes negative, the output of the CMPPRG is LOW; the sign is negative and the negative signal multiplied by negative sign results in a positive output.
- Therefore, the sign modulation of the SCBLOCK produces a full wave rectified output which is available at P0[3].
- For debugging, the Comparator_Bus_1 is brought out on P1[4] using a DigBuf user module.

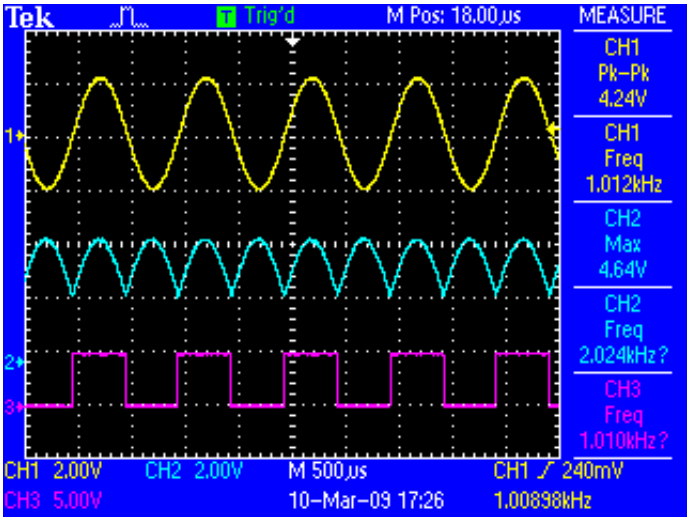
Firmware

The firmware of the example is simple. The following operations are done in main.asm:

- The PGA is started at high power.
- The CMPPRG is started at high power.
- The RefMux is started at high power.
- The modulation source of SCBLOCK is set to Comp_Bus_1 by writing to the AMD_CR register.
- The DigBuf user module is started by default and does not need any function call.
- The hardware takes care of the rest of the operation.

For an input signal of 1 KHz, the screen capture of the input, output, and comparator bus signals is shown in the following figure. The yellow trace is the input, the blue trace is the rectified output, and the pink trace is the output of the comparator.

Figure 3. Input, Output, and Comparator Bus Signals



Note The firmware in the code example is written in assembly. It is very straightforward to write a C program for the example.

```
void main(void)
{
    // M8C_EnableGInt;      // Uncomment this line to enable Global interrupts
    PGA_1_Start(PGA_1_HIGHPOWER);
    SCBLOCK_1_Start(SCBLOCK_1_HIGHPOWER); // Start the SC Block modulator
    CMPPRG_1_Start(CMPPRG_1_HIGHPOWER); // Start the Zero crossing detector
    DigBuf_1_Start(); // Start the Digital buffer
    RefMux_1_Start(RefMux_1_HIGHPOWER); // Start the Refmux
    AMD_CR0 |= 0x05; // Set Comparator_Bus_1 as the modulator source to ASC10

    // Nothing more to do.
    while(1)
    {

    }
}
```

Document History

Document Title: Signal Rectifier Using PSoC® 1

Document Number: 001-52251

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2696891	ABHU	04/22/2009	New example project: Signal Rectifier.
*A	3252432	GRAA	05/09/2011	1. Changed heading from “Signal Rectifier” to “Signal 2. Rectifier using PSoC® 1”. 3. Changed the header to include CE number, Related hardware and author details. 4. Removed the reference to AN2044 as this app note could not be found on the web. 5. Added code snippet for C. 6. Upgraded project to PSoC Designer 5.1 FCS. 7. Changed all “project” to “example”.

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