PSoC 3/5 Design Contest

Component Design Preliminary

Sorry that I could not get to post the specification on Friday. The deadline for the submission of the component is next Monday, that is 17th of December 12:00PM (PDT).

The Specification given below is for the preliminary level of component design.

SPECIFICATION:

Design a 4 bit synchronous counter. Following, are the expected features of the component.

1. The Counter should be capable of counting UP/DOWN, based on the user selection. This should be made as a configuration label.
2. The counter should count with respect to the positive edge of the clock.
3. The counter is expected to reset to the value 4b'0, on the negative edge of the reset. Reset is asynchronous to the clock.
4. The counter, should output the value present in the load_val signal on the next positive edge of the clock, for every rising edge of the load signal.
5. The counter should roll over from 4'd15 to 4'd0 or from 4'd0 to 4'd15 only if the roll_enable signal is high. Else, it should stop at the max/min value appropriately. Reset should release the counter from this lock state if roll_enable is low.
6. The counter should indicate the maximum value, by asserting a max signal high.
7. The counter should indicate the minimum value, by asserting a min signal high.
8. The Max and Min signals are asserted high, only based on the count values and not based on the mode /any other external signal(Irrespective of counting UP or DOWN, the max and min signals are asserted when that value is reached).