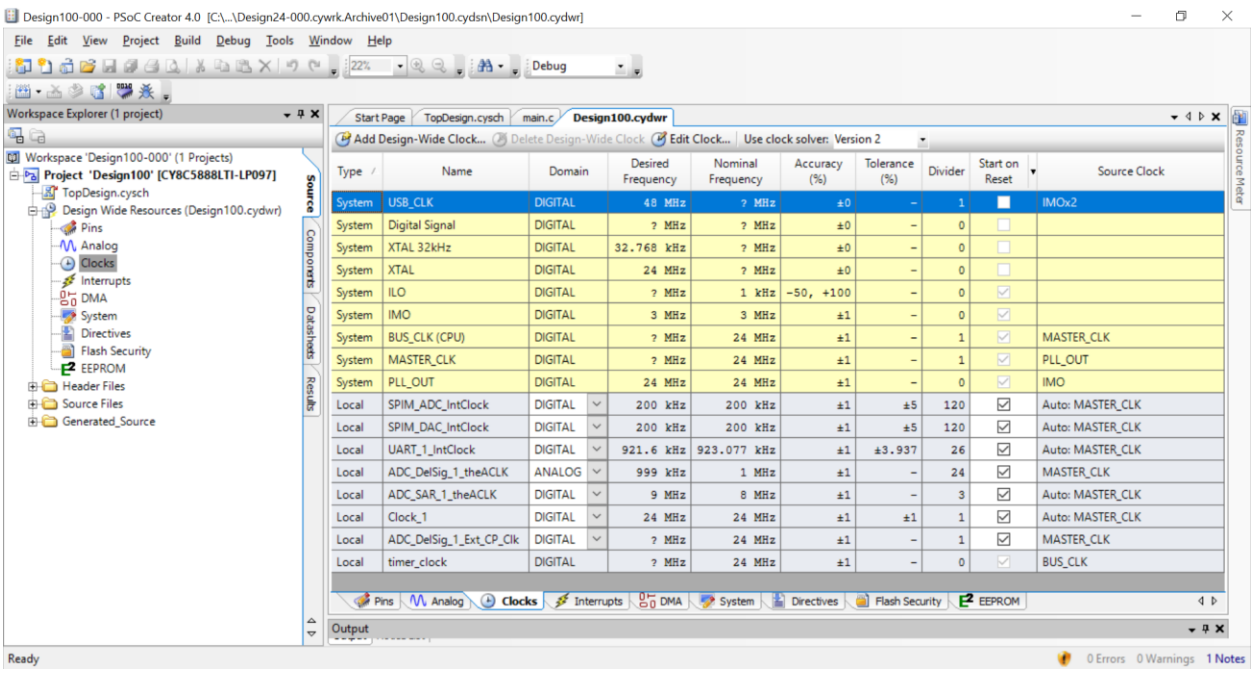
v


Design100-000 - PSoC Creator 4.0 [C:\...\Design24-000.cywrk.Archive01\Design100.cydsn\Design100.cydwr]
File Edit View Project Build Debug Tools Window Help
Debug
Workspace Explorer (1 project)
Workspace 'Design100-000' (1 Projects)
Project 'Design100' [CY8C5888LTI-LP097]
TopDesign.cysch
Design Wide Resources (Design100.cydwr)
Pins
Analog
Clocks
Interrupts
DMA
System
Directives
Flash Security
EEPROM
Header Files
Source Files
Generated_Source
Start Page
TopDesign.cysch
main.c
Design100.cydwr
Add Design-Wide Clock...
Delete Design-Wide Clock
Edit Clock...
Use clock solver: Version 2
Type
Name
Domain
Desired Frequency
Nominal Frequency
Accuracy (%)
Tolerance (%)
Divider
Start on Reset
Source Clock
System USB_CLK DIGITAL 48 MHz ? MHz ±0 – 1 IMOx2
System Digital Signal DIGITAL ? MHz ? MHz ±0 – 0
System XTAL 32kHz DIGITAL 32.768 kHz ? MHz ±0 – 0
System XTAL DIGITAL 24 MHz ? MHz ±0 – 0
System ILO DIGITAL ? MHz 1 kHz -50, +100 – 0
System IMO DIGITAL 3 MHz 3 MHz ±1 – 0
System BUS_CLK (CPU) DIGITAL ? MHz 24 MHz ±1 – 1 MASTER_CLK
System MASTER_CLK DIGITAL ? MHz 24 MHz ±1 – 1 PLL_OUT
System PLL_OUT DIGITAL 24 MHz 24 MHz ±1 – 0 IMO
Local SPIM_ADC_IntClock DIGITAL 200 kHz 200 kHz ±1 ±5 120 Auto: MASTER_CLK
Local SPIM_DAC_IntClock DIGITAL 200 kHz 200 kHz ±1 ±5 120 Auto: MASTER_CLK
Local UART_1_IntClock DIGITAL 921.6 kHz 923.077 kHz ±1 ±3.937 26 Auto: MASTER_CLK
Local ADC_DelSig_1_theACLK ANALOG 999 kHz 1 MHz ±1 – 24 MASTER_CLK
Local ADC_SAR_1_theACLK DIGITAL 9 MHz 8 MHz ±1 – 3 Auto: MASTER_CLK
Local Clock_1 DIGITAL 24 MHz 24 MHz ±1 ±1 1 Auto: MASTER_CLK
Local ADC_DelSig_1_Ext_CP_Clk DIGITAL ? MHz 24 MHz ±1 – 1 MASTER_CLK
Local timer_clock DIGITAL ? MHz 24 MHz ±1 – 0 BUS_CLK
Pins Analog Clocks Interrupts DMA System Directives Flash Security EEPROM
Output
Ready
0 Errors 0 Warnings 1 Notes