Ex0

R_3 10K

Ex1

Ex2

AMux

ADC_DelSig
ADC_DelSig
0
2
ΔΣ
eoc
12-bit

Vbat

Vssa (GND) Vref

RTD
RTD
Rw1 Rw2
RTD Rw3
Rw4

1K

1.5K R_1

Timer_1
Timer
capture_out
capture tc
interrupt
BUS_CLK clock
24 MH 0 reset
32-bit (UDB)

INT_TMR

PGA_2
PGA
0.256V Vref Vin
Ex4

q s
r
SRFF
clk

IDAC8_1
IDAC8
i
ipolarity

pol:
0= SOURCE
1 = SINK

EC_Cell 10K

PGA_1
PGA_Inv
Vin
Vref
EX3

TP2

Comp_3
Comp

q s
r
SRFF
clk

Comp_1
Comp

WaveDAC8_1
WaveDAC8
ws
DAC
wc1
wc2

GlitchFilter_1
Glitch Filter
q d
reset
clock

Clock_2 1000 kHz

Clock_1 100 kHz

Control_Reg_1
Control Reg
control_0
control_1
control_2
control_3

[0:0]
[1:1]

Comp_2
Comp

q s
r
SRFF
clk

TP4

UART_SP

UART

Rx_1 rx tx Tx_1

tx_interrupt

rx_interrupt INT_SP_RX

0 reset

TEL_Stdby