PSoC® 3 and PSoC 5 – Pin Selection for Analog Designs

AN58304

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Associated Project: No
Associated Part Family: CY8C38xxx/CY8C55xxx
Software Version: PSoC® Creator™ 1.0
Associated Application Notes: None

Application Note Abstract

The PSoC® 3 and PSoC 5 families are the most flexible mixed signal microcontrollers on the market today. Almost any analog or digital signal can be routed to any of the many GPIOs. There are, however, some routes to and from analog blocks to GPIO pins that are more optimal than others. For applications that do not use all the analog resources or that require less than 16 bits of resolution, PSoC Creator™ does a good job routing your design and selecting pins. For applications that use a large percentage of analog resources or require 16 bits or more accuracy, this application note helps the designer make the best choices for the highest performance possible and best resource utilization.

PSoC 3 and PSoC 5 Internal Analog Routing

Prior to discussing which pins are better than others for a particular operation or application, it is best to understand the underlying analog structure of the PSoC 3 and PSoC 5 parts.

This application note focuses on connections between the analog blocks and GPIO pins. The SIO, USB, or pins used for connecting the external crystals are not discussed.

The PSoC 3 and PSoC 5 can be divided into an analog and digital section. The top section of the silicon is mostly analog and the bottom section is digital. The analog section consists of several analog blocks such as Delta-Sigma ADC (DSM), comparators, DACs, and SC/CT blocks. The digital section contains the CPU, RAM, ROM, DMA, UDBs, Clocks, and so on. The entire chip is surrounded by pins. Most of these pins are general purpose I/O or GPIO pins. The GPIO pins can be configured for eight different modes: seven digital and one analog input/output mode. This application note concentrates only on the analog mode for these pins.

Analog globals (AGs) and analog mux buses (AMUXBUS) provide analog connectivity between GPIOs and the various analog blocks. As shown in Figure 1, there are 16 AGs that are divided between four quadrants. Each quadrant contains four analog globals: (AGR[7:4], AGR[3:0], AGL[7:4], and AGL[3:0]). The analog mux bus may be connected to any of the GPIO pins and most of the analog block inputs and outputs. It can be divided between the left and right half of the chip or configured as a single bus that wraps around the entire chip. Together, the analog mux bus and analog globals provide up to 18 paths between the analog blocks and GPIO pins. Additionally, there are about 20 dedicated paths between GPIOs and analog blocks. The dedicated routes provide low resistive paths between GPIOs and devices such as current DACs and uncommitted op-amps (operational amplifier).

PSoC Creator routes signals for the user. However, the designer can dictate a preferred route to select the proper GPIOs for a given signal. In a future release of PSoC Creator, the user will be able to add signal properties to force a particular path. The Analog Diagram on the following page shows a more detailed view of the analog section. All analog blocks, signal paths, and switches are shown.

Figure 1. PSoC 3 and PSoC 5 Analog/Digital Layout

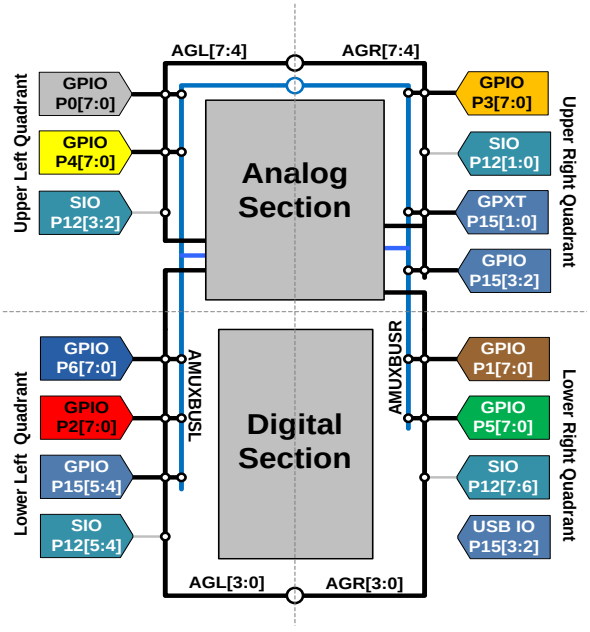
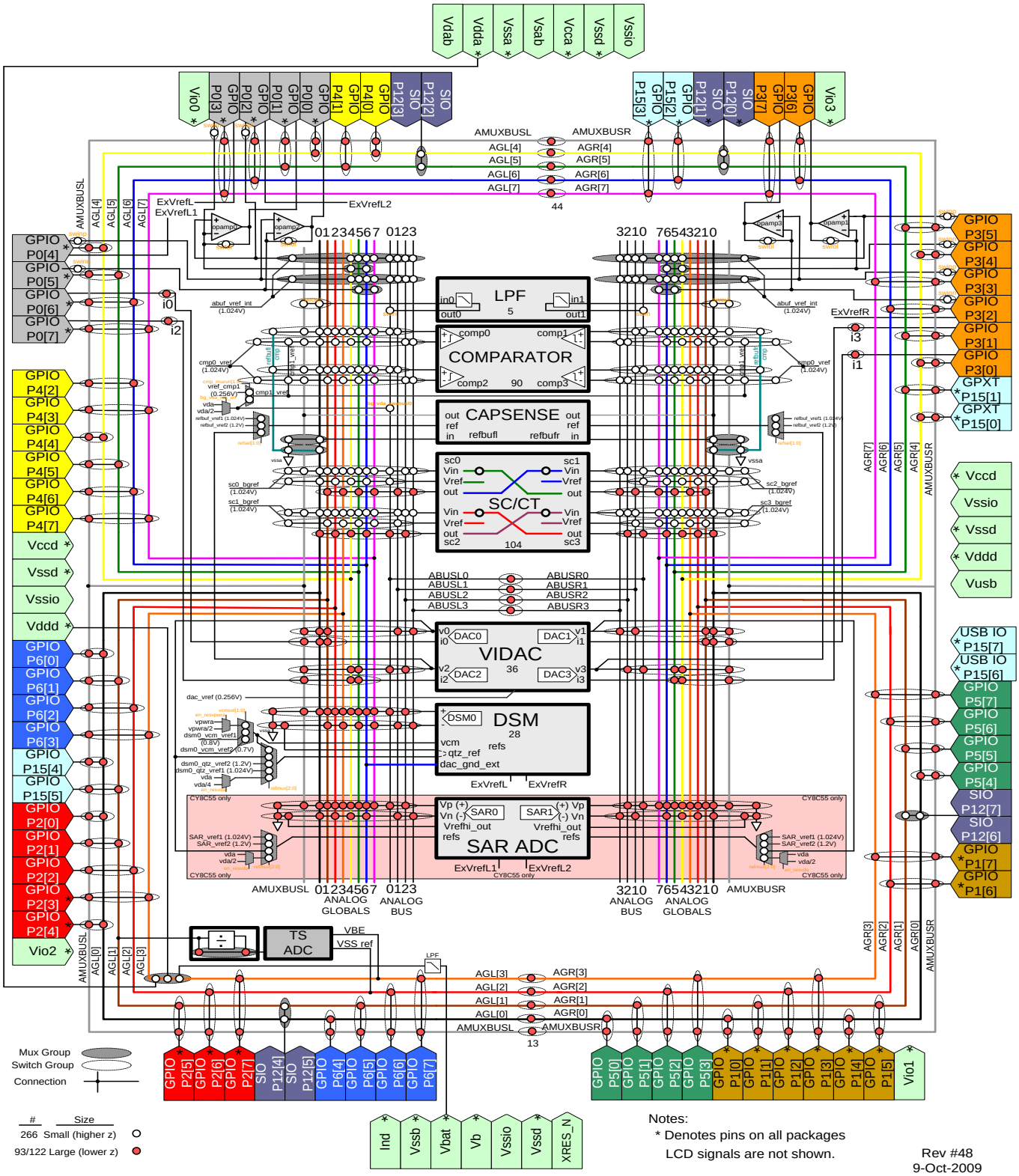


Figure 2. PSoC 3 and PSoC 5 Analog Diagram



To fully understand the analog routing in PSoC 3 and PSoC 5, it is important to understand the Analog Diagram that shows all possible analog routes and switches between analog blocks and GPIOs.

Analog Mux Bus (AMUXBUS)

There are two AMUXBUS routes in PSoC 3 and PSoC 5 devices. The AMUXBUSL may be connected to any of the GPIOs on the left side. The AMUXBUSR can connect to all GPIOs on the right side of the device. The left and right AMUXBUS may be shorted together with an analog switch to create a single bus that can be connected to all GPIO pins. It is possible to use the AMUXBUS to connect all GPIOs to a single analog block such as the Delta-Sigma ADC.

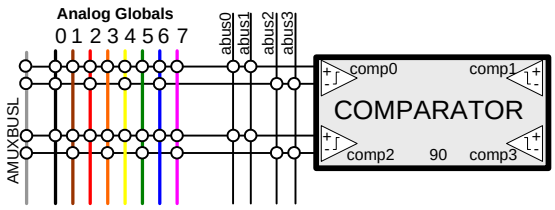
Analog Globals (AGs)

The PSoC 3 and PSoC 5 device is divided into four quadrants as shown in Figure 1 on page 1. The analog global bus has eight routes on each side: AGL[7:0] on the left and AGR[7:0] on the right. Within each side, the bus is divided into two groups: AGR[3:0] and AGR[7:4] for the right side and AGL[3:0] and AGL[7:4] for the left side. The lower four globals on each side are routed to the GPIO in the lower half of the part and the upper four globals on each side are routed to the GPIO in the upper half of the device. All eight analog globals on each side get routed to analog blocks on the same side. Analog globals can be used as single ended or differential signal paths.

The globals on the left and right half may operate independently or they may be joined through the switches that are shown at the top and bottom. The analog globals AGL[3:0] and AGR[3:0] are routed down and around the digital blocks. The other busses AGL[7:4] and AGR[7:0] stay up in the analog section where there is likely to be less digital switching noise and the paths are shorter (less resistive). In the Analog Diagram, each analog block is capable of connecting to various analog busses. These connections form an analog connection matrix between analog blocks and GPIO pins. Analog blocks may be interconnected to each other or to GPIOs. The small circles indicate switches that connect the paths that intersect. The On resistance of the switches colored red is about 200 ohms. The On resistance of the white switches is about 870 ohms. Note that the connection between the pins and analog globals or AMUXBUS is with the lower resistance switches.

Most of the switches can be addressed individually, which means that any combination of switches can be connected at any time. Some analog block I/Os may connect to a different combination of analog busses than other analog blocks. This enables maximum flexibility and, at the same time, keeps size and bus capacitance to a minimum. For example, in Figure 3, the negative input to the two comparators connects to a different set of analog globals. The negative input to comparator 0 connects to the odd analog globals and comparator 2 connects to the even analog globals.

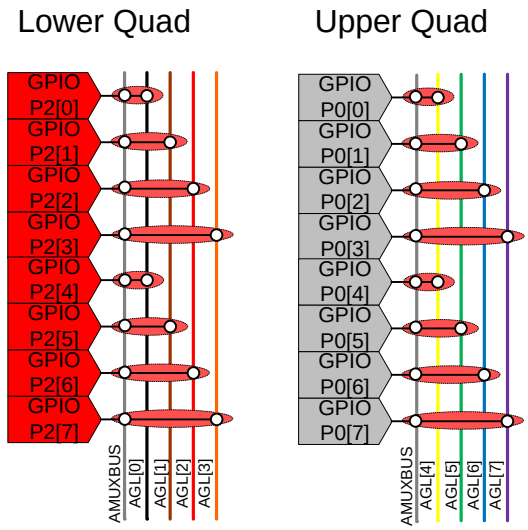
Figure 3. Comparator Connections



GPIO Connection to Analog Busses

Each GPIO pin may be connected to analog globals or the AMUXBUS or both simultaneously. Two pins of each port share the same analog global connection. Figure 4 illustrates in two examples how the GPIOs are actually connected to the analog global busses. PSoC Creator makes these connections for the user when analog wires and muxes are placed between analog blocks and GPIOs.

Figure 4. GPIO Connection to AG[n] and AMUXBUS



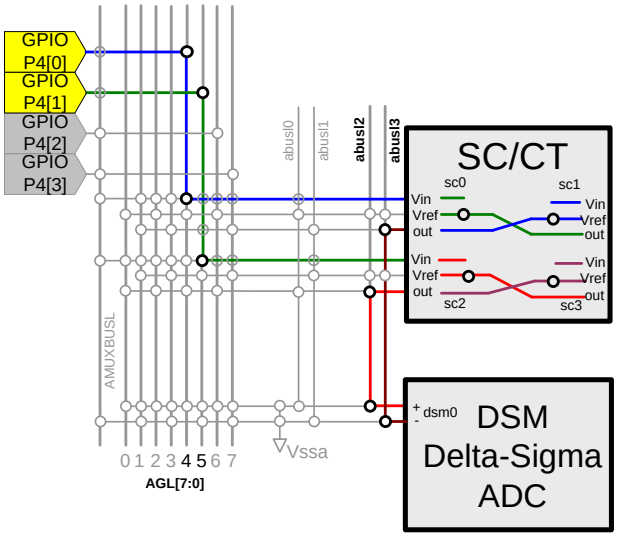
Analog Local Bus (abus)

Internal to the analog section, there are eight additional analog local bus (abus) routes, four in the left half abusl[3:0] and four in the right half abusr[3:0] as shown in the Analog Diagram. These are local routes for interconnecting analog blocks but not to GPIOs. They help to save the analog globals to route to GPIOs. The left and right sides may be shorted together with four analog switches.

Routing Example

Figure 5 illustrates a signal route making use of both the Analog Globals AGL[4] and AGL[5] to make a connection between the GPIOs P4[0] and P4[1] to the SC/CT blocks. The route between the output of the SC/CT blocks to the Delta-Sigma ADC makes use of abusl2 and abusl3. This saves the more valuable routing resources of the analog globals and the AMUXBUS for other routes.

Figure 5. Example of Signal Path



Direct Routes

Several direct routes bypass the analog muxbus, analog globals, and the analog local bus to connect analog blocks directly to GPIOs. For each VIDAC, there is a dedicated route from the current output to a specific GPIO. This dedicated route is only active when the VIDAC is configured as a current sink or source (IDAC). Table 1 shows the corresponding connection between each DAC and the GPIO pin.

Table 1. Dedicated IDAC Connections

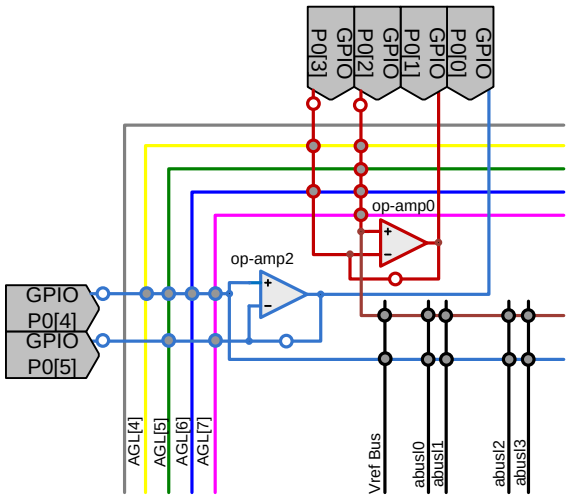
IDAC	GPIO Pin
DAC0	P0[6]
DAC1	P3[0]
DAC2	P0[7]
DAC3	P3[1]

The op-amps also have direct connections between their terminals and dedicated GPIOs. Figure 6 shows these connections graphically. Table 2 lists the GPIOs that are connected directly to the op-amp input and output terminals.

Table 2. Dedicated Op-amp Connections

OPAMP	GPIO Pin (Non-inverting)	GPIO Pin (Inverting)	GPIO Pin (Output)
Opamp0	P0[2]	P0[3]	P0[1]
Opamp1	P3[5]	P3[4]	P3[6]
Opamp2	P0[4]	P0[5]	P0[0]
Opamp3	P3[3]	P3[2]	P3[7]

Figure 6. Dedicated GPIO Connections for Op-amp 0 and 2



Pin Selection Optimization

This brief overview of PSoC 3 and PSoC 5 routing resources makes it easier to understand how selecting a specific pin can assist PSoC Creator make the best route for your application. There are two reasons for routing optimization: resource usage and performance. Although the PSoC 3 and PSoC 5 contain much more analog routing resources than previous families, there is still a finite set of analog routes. Making the right pin assignments can mean the difference between a design fitting into a particular part and not having sufficient routing resources.

Direct Routes to GPIO Pins

As mentioned previously, there are several internal analog signals that have direct routes between an analog block and a specific GPIO pin. These direct routes are limited to Port0 and Port3. They are used for routing IDAC outputs, op-amp connections, external references, or internal reference bypass capacitors. Table 3 on page 5 is a summary of these signals and the GPIO connections.

Table 3. GPIO Direct Routes

Port	Description
P0[0]	Op-amp2 output
P0[1]	Op-amp0 output
P0[2]	Op-amp0 non-inverting input ExVrefL2 SAR ADC reference input
P0[3]	Op-amp0 inverting input ExVrefL DCM (DelSig ADC) reference input Internal Reference bypass capacitor
P0[4]	Op-amp2 non-inverting input ExVrefL1 SAR ADC reference input
P0[5]	Op-amp2 inverting input
P0[6]	VIDAC0 current sink/source connection
P0[7]	VIDAC2 current sink/source connection
P3[0]	VIDAC1 current sink/source connection
P3[1]	VIDAC3 current sink/source connection
P3[2]	Op-amp3 inverting input ExVrefL DCM (DelSig ADC) reference input Internal Reference bypass capacitor
P3[3]	Op-amp3 non-inverting input
P3[4]	Op-amp1 inverting input
P3[5]	Op-amp1 non-inverting input
P3[6]	Op-amp1 output
P3[7]	Op-amp3 output

IDAC Pin Selection

Each IDAC (current DAC) output may be routed to a GPIO in many ways. Using the analog globals or the analog mux bus works fine as long as the maximum current is limited to the two lower ranges of 32 uA or 255 uA. When using the high current range of 2 mA, the resistance in the path and analog switches may cause an excessive voltage drop and limit the compliance voltage of the current source at the pin. A path through the analog globals can be 500 ohms or more. To minimize the voltage drop, make sure that one of the pins listed in Table 1 on page 4 is used to connect the output of the IDAC. This dedicated route is less than 200 ohms from IDAC to GPIO. PSoC Creator selects the appropriate IDAC to make sure that connection is made. Using these dedicated pins also frees up routing resources that can be used for other parts of the design. These dedicated pins can be used irrespective of the current range you use with the IDAC. Therefore, you can use the dedicated pins any time an IDAC is used to maximize routing resources.

Op-amp Pin Selection

The op-amps are connected to the GPIOs in such a way that they can be used without any internal analog global busses, See Figure 6 on page 4. If all connections to the op-amp are external through the GPIOs, it is a good idea to use the dedicated pins. In many cases, the op-amp may be used as a buffer to an internally generated signal, such as a buffer to a VDAC output. After the op-amp is enabled, the dedicated output GPIO will always be driven by the output of the op-amp. This GPIO is now dedicated to the op-amp output. If you must use a different pin for the output, the dedicated output pin still outputs the signal. If the op-amp is not used, it has no affect on the GPIOs directly connected to it. These GPIO pins operate as any of the other GPIOs when the op-amp is disabled.

Reference Voltage Pins

External references can be used to enhance the accuracy or change the range of the ADCs. There are connections for external references for both the Delta-Sigma and SAR ADCs. The SAR ADC is only available in the CY8C55 family. The internal reference is accurate up to 0.1% over the operating temperature range depending on the device selected. An external reference can increase the accuracy beyond 0.1%. For the Delta-Sigma ADC, either pins P0[3] or P3[2] may be used for an external reference. Pins P0[2] or P0[4] are used for the SAR ADC external reference.

Pins P0[3] and P3[2] can also be used to bypass the reference voltage used for the Delta-Sigma ADC with a filter capacitor. A capacitor in the range of 1 uF to 10 uF is used to filter out low frequency noise on the internal reference voltage.

Separating Analog and Digital Signals

Most analog input signals have relative high impedance and digital signals usually have low output impedance. Analog input signals can have an impedance of several MΩ. However, digital signals can have output impedance of 10 to 50 ohms or less. When these two signals are placed in close proximity, or are on adjacent pins, the fast rise and fall times of the digital signal can easily be capacitively coupled to the analog signal. Therefore, when selecting pins for analog and digital functions, it is recommended that analog and high speed digital signals be kept away from each other when possible. Similar to laying out a circuit board, signals near each other have some amount of capacitive coupling. This coupling can occur both internal to the chip at the I/O pads and on the circuit board traces. Isolating these signals by at least one pin reduces this coupling both internally and externally.

Best Analog Ports

The largest pin count parts of the PSoC 3 and PSoC 5 families have more than seven full 8-pin ports or 56 GPIOs that can be used for analog input and output. Of these seven ports, three can have a slight analog performance advantage. Ports 0, 3, and 4 reside in the analog upper portion of the chip. The analog globals, AGL[7:4] and AGR[7:4] that connect to these ports, also remain in the upper analog section of the part. For designs that require less than 16 bits of analog performance, any port works equally as well. For higher performance, low noise designs, it is better to use ports 0, 3, and 4 for analog signals.

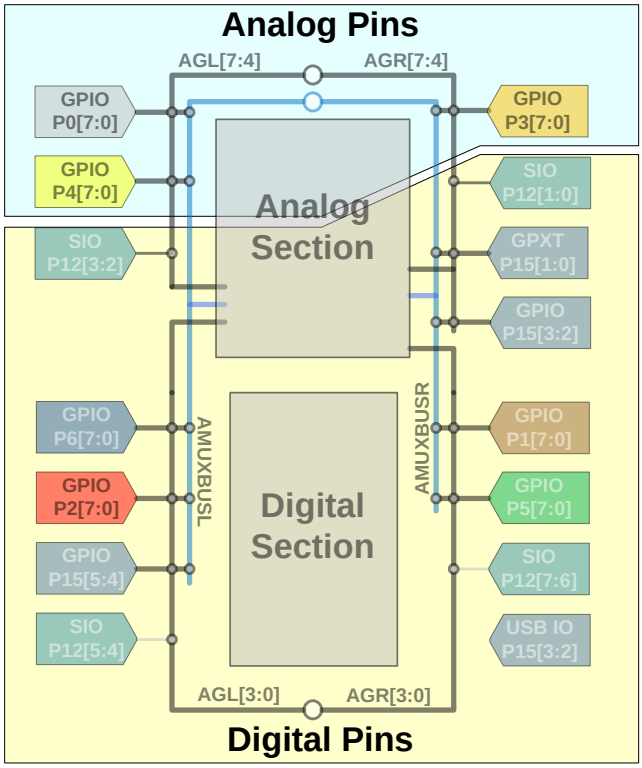
To take separating analog and digital signals further, it is good design practice to keep analog and digital signals on opposite sides of the chip. This also helps when it is time to lay out the circuit board. A few easy steps can be used to plan a pinout for optimal analog performance.

Design Steps

1. Determine how many analog pins/ports are required for a given design.
2. Determine which signals can or should use the dedicated routes between the analog block and the GPIO pin. Make these pin assignments first.
3. Start with port 0 and work out in both directions to port 4 and port 3 and select the analog GPIO pins needed for the design.
4. Draw a line between the analog GPIO pins selected and the rest of the pins required for the design.
5. Keep all analog GPIOs on one side of the line and all digital GPIOs on the other.

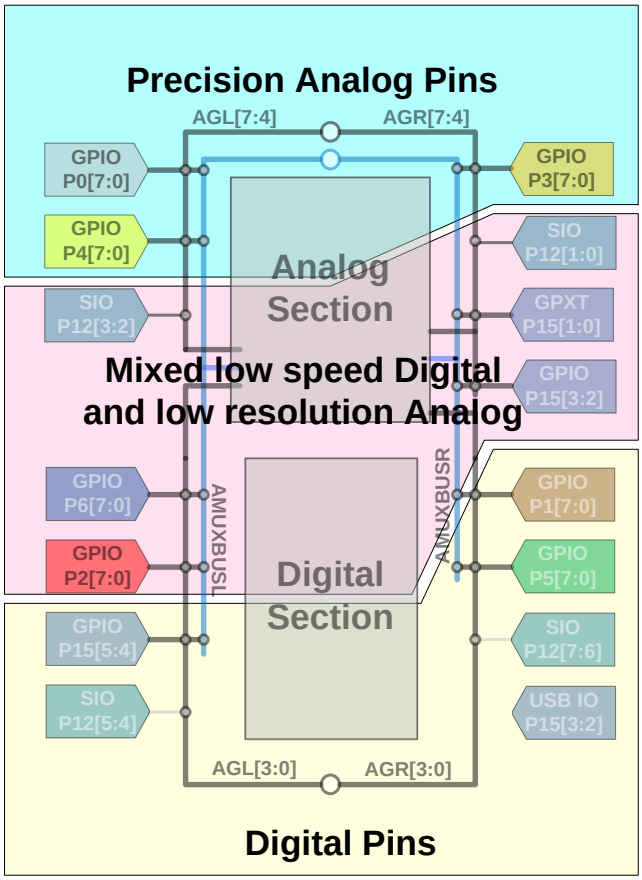
Follow these simple steps to isolate the analog and digital signals on both the chip and your circuit board. Figure 7 shows an ideal separation between analog and digital ports.

Figure 7. Ideal Analog and Digital Separation



Sometimes a design may have a mix of precision analog, low resolution analog, low speed digital, and high speed digital. The low precision and low speed digital can be used to isolate the precision analog and high speed digital. See Figure 8 for an example.

Figure 8. Three Signal Sections



Other Resource Optimizations

Muxing Pins

Refer to the GPIO connection pattern to the Analog Global Bus in Figure 4 on page 3. The sequence is always 0,1,2,3,0,1,2,3 or 4,5,6,7,4,5,6,7. Each quadrant has four analog globals; therefore, make sure you make the best use of them. If your design includes a 4-input analog mux, connecting pins P0[0], P0[1], P0[2], and P0[3], it requires all four Analog Globals in that quadrant AGL[7:4]. It may not be possible to route more signals in that area. Instead, an alternative solution is to connect pins P0[0], P0[1], P0[4], and P0[5] to the analog mux. This time only globals AGL[5:4] are used and AGL[7:6] are left to route other signals. See Figure 9 and Figure 10 on page 7 for a graphical representation of these examples.

Figure 9. Inefficient Use of Globals

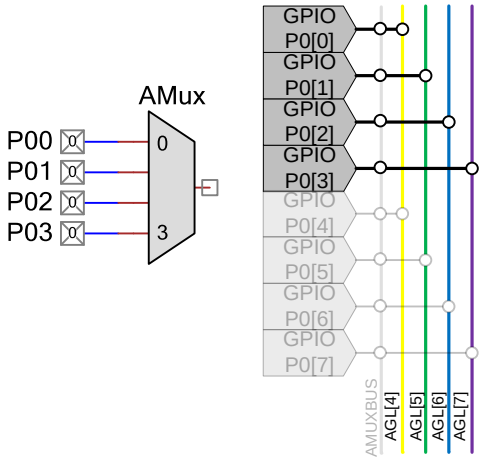
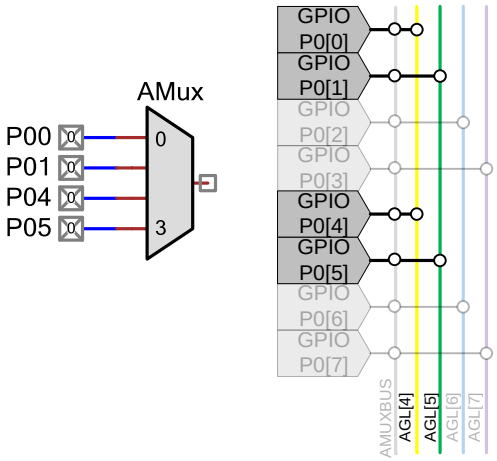


Figure 10. Efficient Use of Analog Globals



Both these examples use four pins with a 4-input analog mux (AMux). The example in Figure 9 uses all four Analog Globals AGL[7:4], whereas the example in Figure 10 uses just two Analog Globals, AG[5:4]. This small change in pin selection helps to double the available routing resources.

Connecting to the Sigma_Delta ADC

The analog blocks are equally distributed between the left and right sides of the chip. Currently, there is just one Delta-Sigma ADC, which is placed on the left side and only has direct connections to the routing resources on the left side. Signals may be routed from the right side of the part, but only by connecting the left and right analog globals together. When pins from the right side of the part must connect to the ADC, the analog globals on the right side must be connected to the corresponding analog globals on the left side. For example, if pin P3[7] needs to be routed to the ADC, the pin is first connected to AGR[7]. Then AGL[7] must then be connected to AGR[7] to route to the ADC. However, if pin P0[7] is selected, then only analog global AGL[7] is used instead of both AGR[7] and AGL[7]. (See the top section Analog Diagram for clarity). All of the left analog globals (AGL[7:0]) may be connected to the corresponding right analog globals (AGR[7:0]).

Summary

Because there are sufficient analog routing resources, most engineers need not be concerned with getting the most efficient hardware usage. For those cases where most analog resources are used, routing may become tight. This application note and a better understanding of analog routing can aid in fitting even the most complicated design in the desired part.

As discussed, most applications do not need to make an effort to get maximum analog performance. The topics discussed in this application note take little effort to implement and can provide a better signal to noise ratio and less offset.

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Document History

Document Title: PSoC® 3 and PSoC 5 Pin Selection for Analog Designs

Document Number: 001-58304

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2828695	MEH	12/15/2009	New application note.
*A	2991540	SRIH	07/22/2010	Fixed branding discrepancies

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