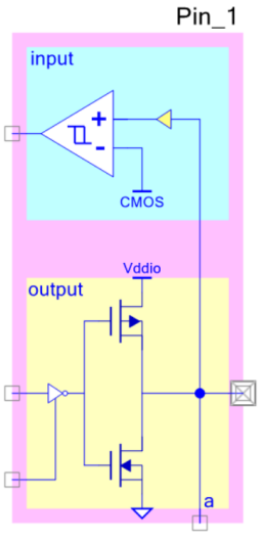
Pins Annotation Component
0.0



Features

- Shows pins configuration and hardware connections
- Facilitates PSoC pins configuration
- Doesn't consume system resources
- Doesn't affect run-time performance

General description

PSoC Pins component offers variety of configurations, which are not intuitive to navigate [1, 2]. Pins Annotation component facilitates this task by visualizing the Pins internal structure. It identifies terminals with direct access to PSoC's internal hardware and graphically displays pins configuration. Component was designed with PSoC5 in mind, but it may be useful for PSoC4 as well due to similarities of their pins structures. Component covers many, but not all configuration options available to PSoC pins. Current release shows only true hardware connections, and does not cover registers, Capsense, Mux, interrupts or clocks. Component doesn't consume system resources, or affects the run-time performance of the project.

When to use Pins Annotation

The component was developed to simplify pins configuration on PSoC4 and PSoC5 projects. It is also useful for documenting projects and making schematics using of-chip components and complimentary PSoC Annotation Library(*) [3].

* PSoC Annotation Library is a collection of the off-chip annotation components

Functional Appearance

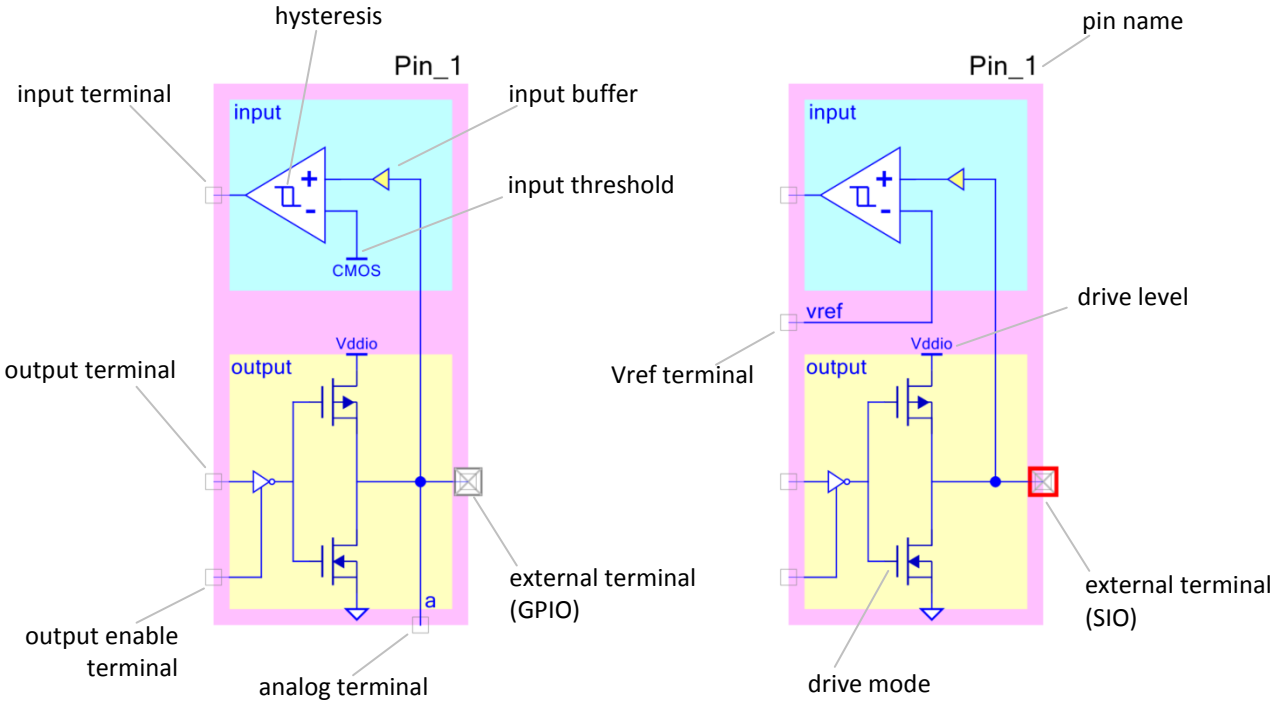


Figure 1. Component appearance with options enabled (top-to-bottom): Digital Input terminal, Digital Output terminal, Output Enable terminal, Analog terminal, Digital Input Hysteresis, Input Buffer, Input Threshold, Vref terminal, external Pin terminal (GPIO), Drive Mode, Display Name, Output Drive Level, external Pin terminal (SIO). Pins with SIO features enabled have red outline.

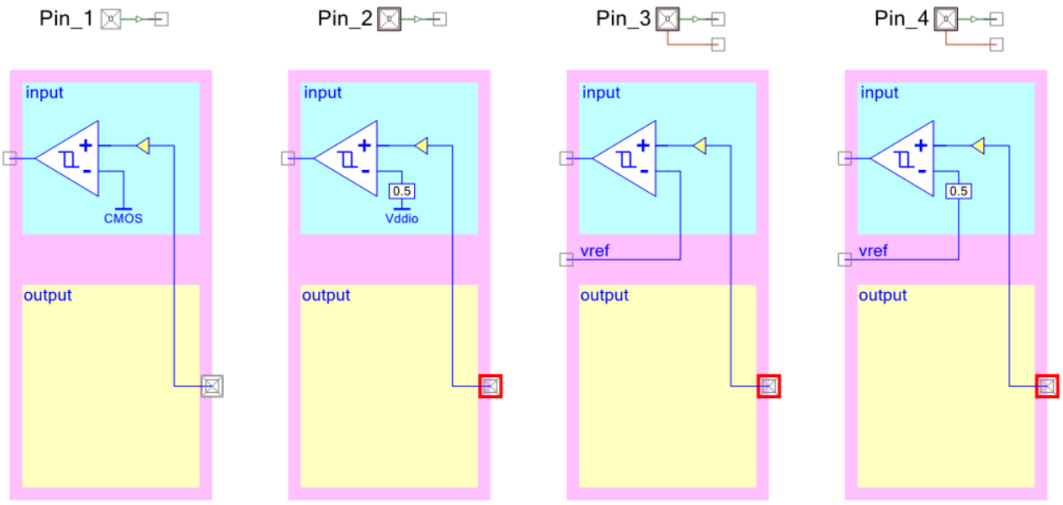


Figure 2. Pin and annotation appearances in Digital Input mode: (1) default, (2) Threshold = 0.5×Vddio, (3) Threshold = Vref, (4) Threshold = 0.5×Vref. Pins with SIO features enabled have red outline.

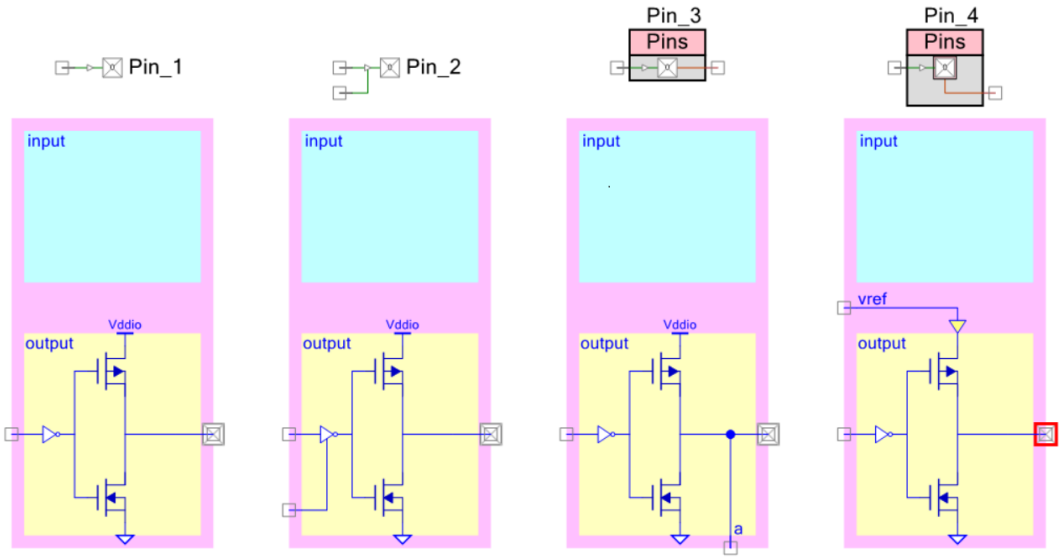


Figure 3. Pin and annotation appearances in DigitalOutput, StrongDrive mode: (1) default view; (2) OutputEnable = true; (3) Analog = true; (4) DriveLevel = Vref. Pins with SIO features enabled have red outline.

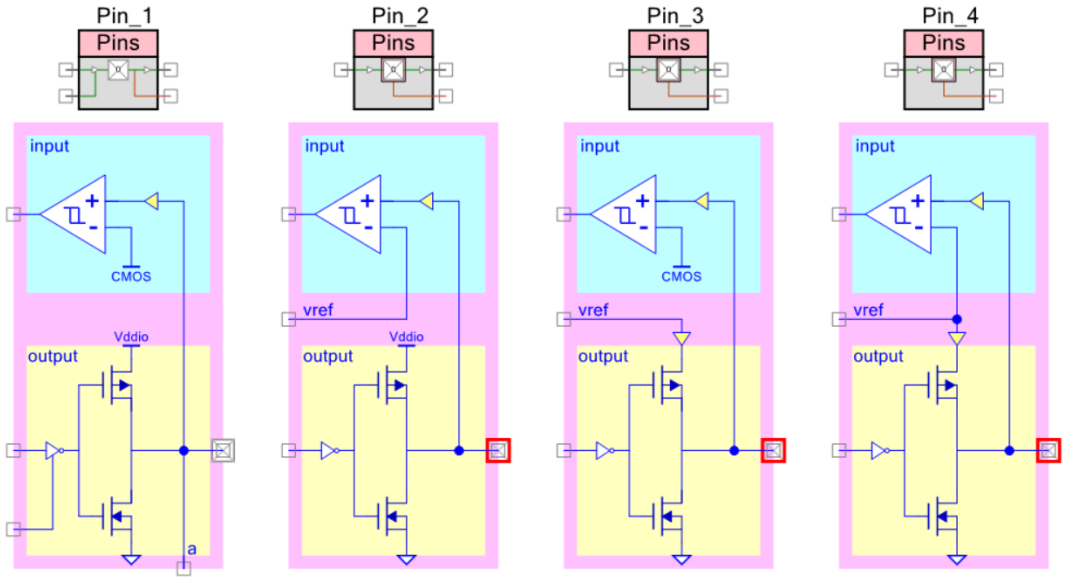


Figure 4. Pin and annotation appearances in multi-mode configurations: (1) Analog + Digital Input + Digital Output; (2) Digital Input (Threshold = Vref) + Digital Output; (3) Digital Input + Digital Output (Drive Level = Vref); (4) Digital Input (Threshold = Vref) + Digital Output (Drive Level = Vref). Pin Drive mode is set to Strong Drive in all cases. Pins with SIO features have red outline.

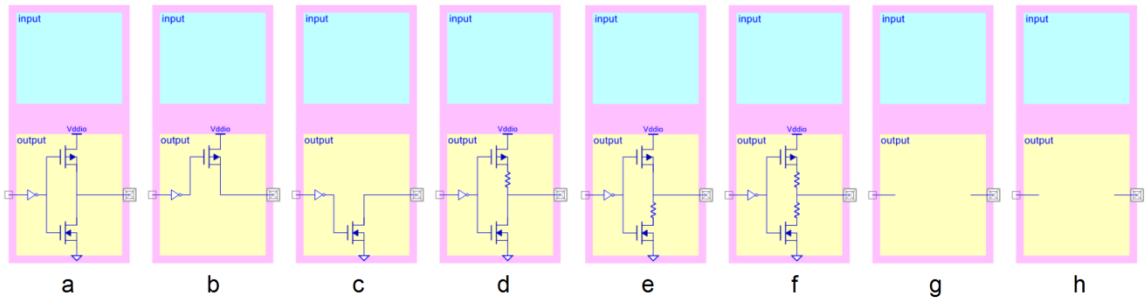
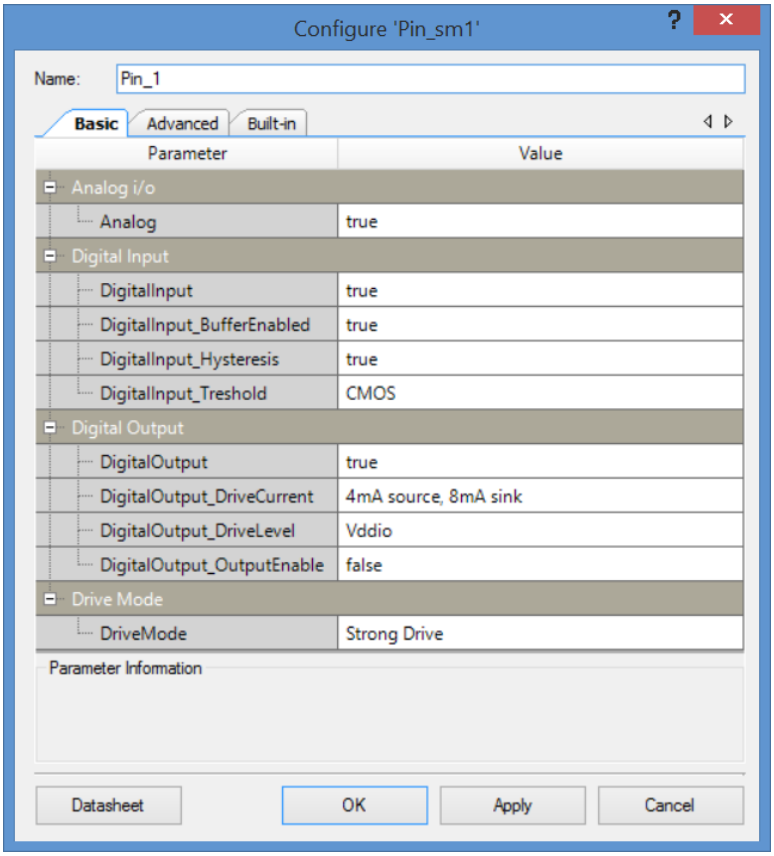


Figure 5. Component appearance for various DriveMode setting: (a) Strong Drive, (b) Open Drain, Drive Up, (c) Open Drain, Drive Down, (d) Resistive Pull Up, (e) Resistive Pull Down, (f) Resistive Pull Up/Down, (g) High Impedance Digital, (h) High Impedance Analog. Pin configured for Digital Output.

Parameters and Settings

Typical Basic dialog provides following parameters:



Analog (bool)

Enables the analog terminal to allow analog signal routing to other components. Default setting is True. When this option is selected, analog terminal is displayed.

DigitalInput (bool)

Enables Digital Input terminal. Default setting is True. When this option is selected, the digital input terminal is displayed.

DigitalInput_BufferEnabled (bool)

Enables digital input buffer. Default setting is True. When this option is selected, the digital input buffer is displayed.

DigitalInput_Hysteresis (bool)

Enables digital input differential hysteresis. Default setting is True. When this option is selected, the hysteresis symbol is displayed. This option available only for SIO pins. For GPIO pins the hysteresis is always enabled.

DigitalInput_Threshold [CMOS / CMOS or LVTTL / LVTTL / 0.5×Vddio / 0.4×Vddio / 0.5×Vref / Vref]

Specifies the digital input logic level threshold. Default setting is CMOS. When 0.5×Vref or Vref option is selected, the Vref terminal is displayed (Figure 3). When any of the 0.5×Vddio, 0.4×Vddio, 0.5×Vref or Vref option is selected, the Pin becomes marked as SIO pin.

DigitalOutput (bool)

Enables Digital Output terminal. Default setting is True. When this option is selected, the digital output terminal is displayed.

DigitalOutput_DriveCurrent [4mA source, 8mA sink / 4mA source, 25mA sink]

Specifies the nominal pin drive currents. Default setting is “4mA source, 8mA sink”. When 25mA sink option is selected, the Pin is marked as SIO pin.

DigitalOutput_DriveLevel [Vddio / Vref]

Selects the output drive voltage supply sourced by the pin. Default setting is Vddio. When Vref option is selected, the Vref terminal is displayed and the Pin is marked as SIO pin.

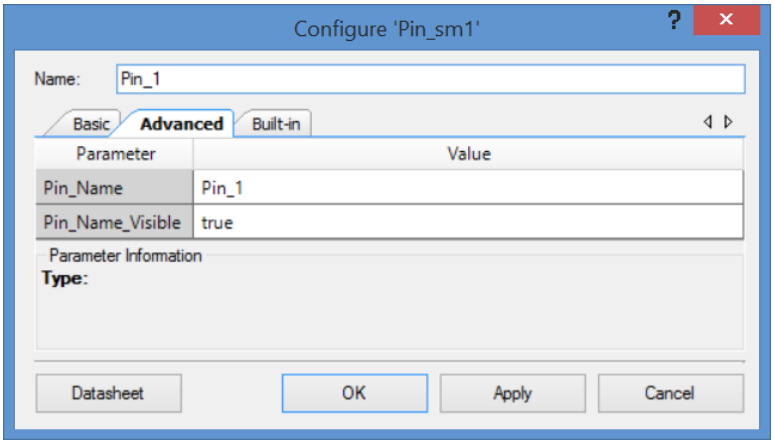
DigitalOutput_OutputEnable (bool)

Sets visibility of the output enable terminal. Default setting is False. The output enable feature allows a hardware signal to control the pin's output drivers. A high logic level configures the output drivers according to the Drive Mode parameter. A low logic level disables the output drivers and places the pin into the HI-Z drive mode.

DriveMode [Strong Drive / Open Drain, Drives High / Open Drain, Drives Low / Resistive Pull Up / Resistive Pull Down / Resistive Pull Up/Down / High Impedance Digital / High Impedance Analog]

Sets pin drive mode (Figure 5). Default setting is Strong Drive.

Advanced dialog provides following parameters:



Pin_Name (string)

Component display name (Net Name). Displays user-defined name of the component, which can be any string of characters. It is not auto-enumerated and may differ from the Instance Name. The Net names are not automatically checked for duplicate instances, it is user responsibility to keep track of them. The Net Name may coincide with the Instance Name of the component, for example a Pin with Instance Name “Pin_1” can also be given a Net Name “Pin_1”. Visibility of this parameter is controlled by Pin_Name_Visible option.

Pin_Name_Visible (bool)

Sets visibility of the Pin_Name. Default value is True.

Application Programming Interface

The component does not have associated API.

Resources

The component doesn’t consume any hardware resources.

Performance

The component doesn’t affect project run-time performance.

Application examples

See **Appendices 1-2** for component application examples.

Component Changes

Version	Description of changes	Reason for changes/impact
0.0	First beta release.	

References

1. AN60580 - SIO Tips and Tricks in PSoC® 3 / PSoC 5LP
   https://www.cypress.com/documentation/application-notes/an60580-sio-tips-and-tricks-psoc-3-psoc-5lp
2. Using PSoC3 and PSoC 5LP GPIO Pins.
   https://www.cypress.com/documentation/application-notes/an72382-using-psoc-3-and-psoc-5lp-gpio-pins
3. PSoC Annotation Library v1.0,
   https://community.cypress.com/thread/48049
4. Jordan Dimitrov, EDN, Dec 1, 2011
   https://www.edn.com/inexpensive-vfc-features-good-linearity-and-dynamic-range/

Appendix 1

1-Shot timer

Basic 1-shot timer schematic using pins hardware is shown on Figure 6. It requires only a single pin and a capacitor to produce a pulse of fixed duration in response to the triggering pulse. The triggering pulse can be as short as a single bus clock. The pin should be configured for both digital input and output; the Driving Mode set to Resistive Pull Up. The trigger sets SRFF, charging capacitor through the pin's internal pull-up resistor. Once capacitor voltage reaches the input threshold level the SRFF resets, generating output pulse of fixed length. The length of the pulse is defined by the values of the capacitor and pull-up resistor[(*)], the input threshold level and comparator delay, $\tau \approx 0.7 \times R_u C_2$.

Table 1. Pin_1 configuration and observed output pulse length as function of the capacitor value.

Pin configuration	C_2(nF)	τ (us)
DigitalInput: enabled, Buffer= enabled, Hysteresis=true, Threshold=CMOS. **DigitalOutput:** enabled, Drive Current= 4ma src/ 8mA sink, DriveLevel= Vddio; OutputEnable=false. **DriveMode:** Resistive Pull Up	0.1	0.64
	1	3.3
	10	31

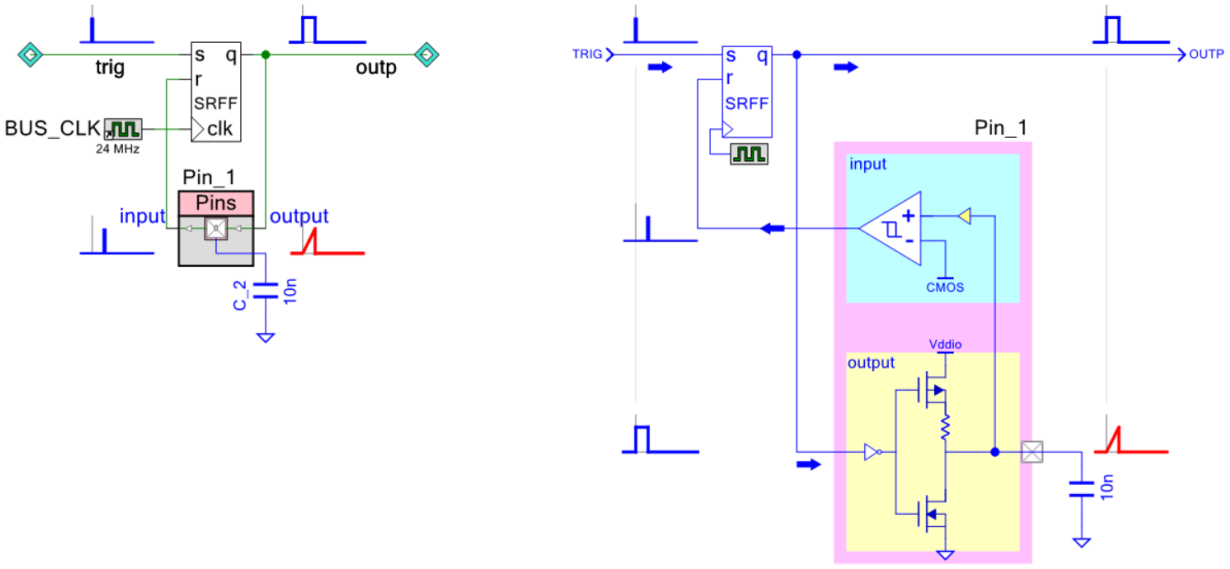


Figure 6. Example of the 1-shot timer with fixed output pulse length using a GPIO pin and external capacitor. Pin Annotation shows internal functionality of the Pin_1.

[*] Pull-up/down resistor values are ≈4.4k, but due to low precision they are not even.

Appendix 2

Voltage-controlled oscillator (VCO)

Pins' hardware can be utilized to create a Voltage Controlled Oscillator based on 1-shot architecture[(*)] [4], consuming minimal hardware resources (Figure 7). The control voltage is supplied to the high-impedance positive input of the Opamp, which causes linear charge of the feedback capacitor C1 during low-phase of "outp" signal. The Pin_34 is configured for Analog and Pin_36 configured for Analog and Digital Input. Once capacitor voltage reaches the input threshold, Pin_36 fires a short pulse triggering 1-shot timer, described in Appendix 1. The 1-shot timer produces digital pulse of the fixed width, discharging the feedback capacitor C1 during high-phase of the "outp" signal. Then cycle repeats.

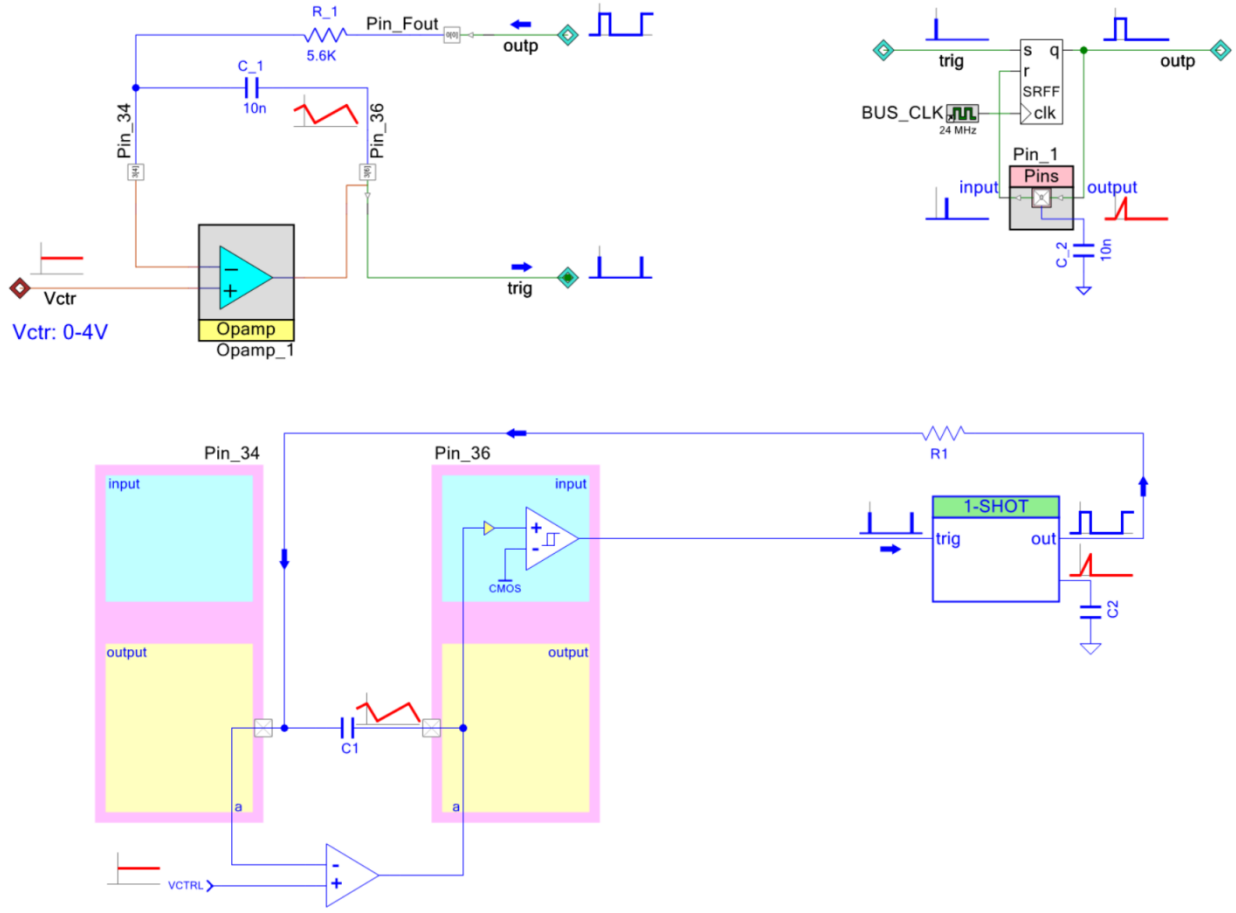


Figure 7. Example of the VCO using 1-shot architecture. Top – PSoC schematic, Bottom – project annotation using Pins Annotation component. Pin_34 is configured for Analog, Pin_36 is configured for Analog and Digital Input. Analog 1-shot timer described in Appendix 1.

[*] Original idea of this type of VCO is attributed to Bob Pease.

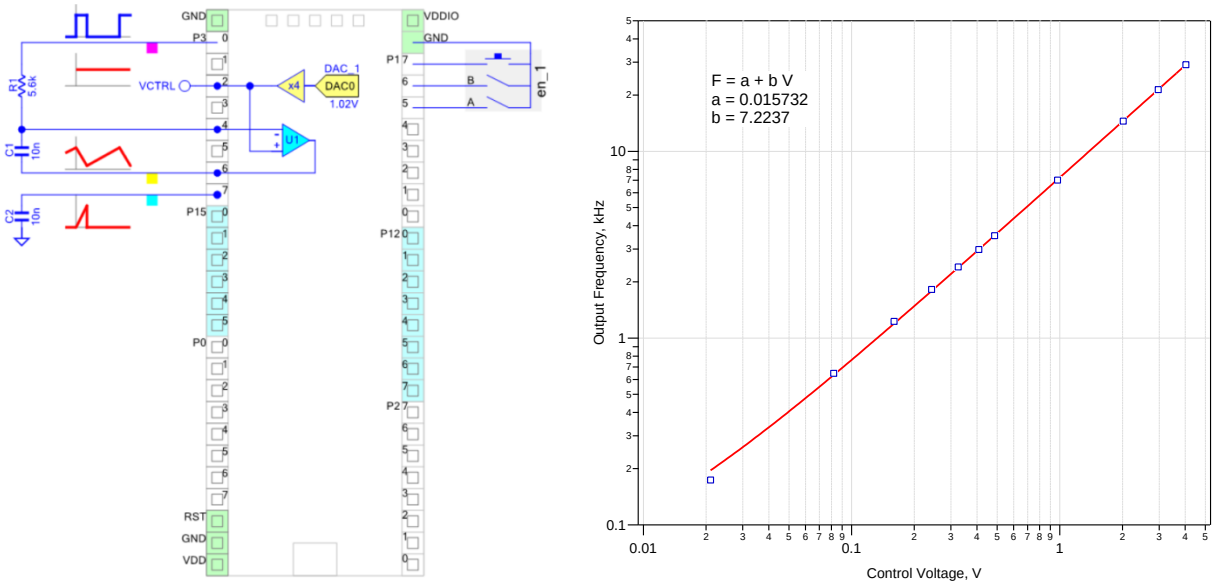


Figure 8. Project annotation created with PSoC Annotation Library [3]. Project uses only three external parts (two capacitors and resistor). A rotary encoder and VDAC form optional voltage generator for VCO testing. Right: VCO output frequency vs. control voltage.

The VCO output frequency response is linear(*) and directly proportional to the control voltage: $F \sim (V_{CTRL}/V_{DD}) \times (1/\tau)$, where τ – is the duration of the 1-shot pulse. Components R1 and C1 do not participate in equation, but their values should be optimized to prevent Opamp output falling into the ground during discharge). For example, using R1=5.6k, C1=C2=10n the output frequency varies from 170 Hz to 29 kHz for control voltage 20mV to 4 V.

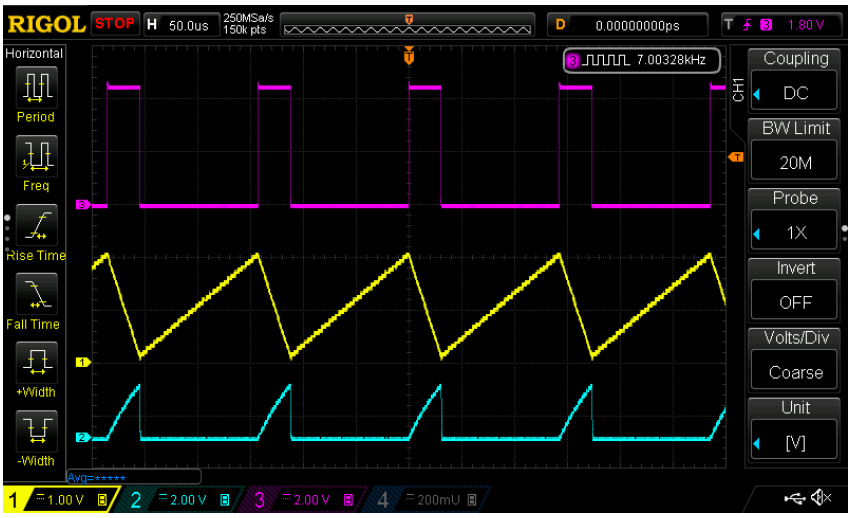


Figure 9. VCO traces at V_{CTRL}=1V. Fuchsia – VCO output; Yellow – Opamp output; Cyan – 1-shot timer output.

* Deviation from linearity is caused by the Opamp bias offset and restricted non-rail-to-rail operation.