Space-and-Cost-Efficient Neuron Model Implementation Using an Analog FPGA

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***Abstract*—As an electronic analog neuron model, small and inexpensive circuit using an analog FPGA is proposed. By making full use of chip property and maximum circuit packing through placement search, it surpasses the previous implementation by factors of 4 for space and 15 for cost.**

Keywords—FitzHugh-Nagumo model, Cypress PSoC

I. Introduction

FitzHugh-Nagumo model is a simplified model of neuron, based on the Hodgkin-Huxley formulation. It was suggested by FitzHugh [1], and realized by Nagumo et al. [2] using a tunnel diode for nonlinear operation. Since then, various types of analog implementations have been proposed .

From the viewpoint of practical applications, standard LSIs are preferred to circuits with special elements like tunnel diodes or memristers [3]. In addition, commercial LSIs attract attention, compared to custom LSIs [4, and have already been proposed by Zhao et al. [5].

They used dpASP [6] as analog FPGA and had problem with its circuit size and price. If some large model is to construct, these factors will impede usage. Standing on this viewpoint, this article proposes the use of PSoC [7] and features performance by factors of 4 for space and 15 for cost.

II. Model and its Implementation

A. FitzHugh-Nagumo model

It can be formulated as:

$$dv/dt = v - v^3/b - w + I \quad (1a)$$

$$dw/dt = w - v + a \quad (1b),$$

where v denotes *membrane potential* and w does *recovery variable,* with a and b as constants.

B. Circuit to implement FitzHugh-Nagumo model

By applying the standard method of solving differential equations on an analog computer, Eqs. (1a) and (1b) can be programmed as in Fig. 1 in the bock diagram format (boxes with "1/s" inside denote integrator).

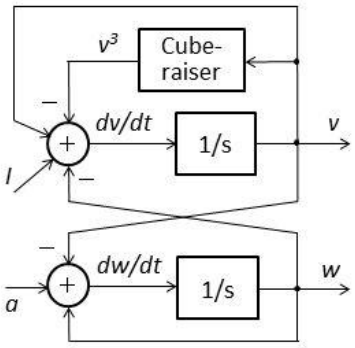

Fig. 1 Circuit to solve FitzHugh-Nagumo model

III. Implementation by PSoC

A. Implementation Outline

Fig.2 shows the outline of implementation. Two integrators ("integ") directly correspond to two "1/s" in Fig. 1, while three blocks at top take the operation "$v - v^3/b$", to be detailed in the next subsection.

PSoC integrators, configured on the switched-capacitor (SC) technique, have two inputs, A and B, where polarity of A can be set either positive or negative (B has fixed negative polarity). By making full use of this property, Fig. 2 does not include summing points shown in Fig. 1.

B. Multiplication by ADC and DAC

Implementation of (1a) and (1b), multiplier to provide v^3 from v is necessary other than integrators to solve differential equations.

dpASP Zhao et al. used looks to have analog multiplier, but actually that is not the case, and multiplication is implemented by a multiplying DAC and an ADC is used to get multiplier value in digital.

Though PSoC does not have analog multiplier, the same principle can be applied. The three blocks at top of Fig. 2 implements this, where the ADC get v and DAC generates v-v^3, after cubic and subtract operations (in the dashed box) by software.

C. Maximum packing into one PSoC chip

Each of the four blocks in bold rectangles in Fig. 2 can be put into one SC block inside PSoC. Largest PSoC, type I chip, has eight SC blocks, then two neuron models seem to be accommodated in one PSoC chip, other than ADCs and DACs. However, connectivity of PSoC blocks has strong "neighboring" restriction, and simple placement may result in "blocks cannot be connected".

In order to cope with this problem, search for placement under the connectivity constraint is coded in C language. Fig. 3 shows the result of the *only* solution for two neurons packed in one chip[1].

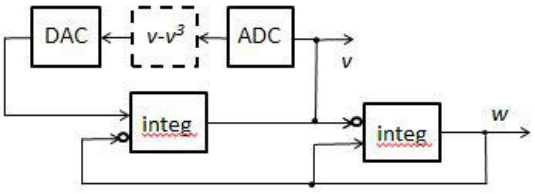

Fig. 2 PSoC circuit to solve FitzHugh-Nagumo model

[1] Resolutions of ADC and DAC are 8- and 6- bits, respectively, for minimum implementation. If higher resolution is necessary, they need two SC blocks, meaning one neuron in one chip.

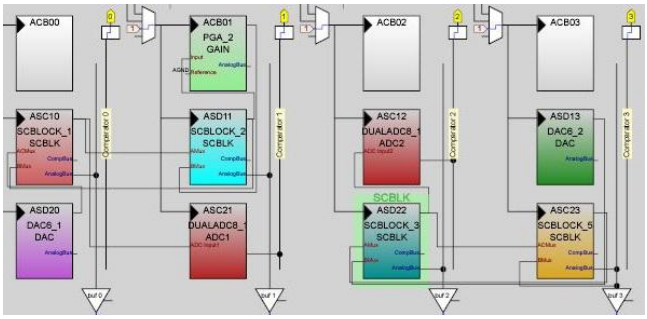

Fig. 3 Optimal Placement on a 4-column PSoC

D. *Additional techniques to realize maximum packing*

- Detour routing
  Though integrator marked by white arrow in Fig. 3 needs feedback around it, such connectivity is not provided by PSoC. Then, amp. marked by black arrow, effectively a wire, provides the feedback path, instead. This technique, possible if row 1 of Fig. 3 has vacancy, is sometimes effective.
- Proper clock phase selection
  Among two phases of SC operation, usually only ϕ 2 is considered. However, if a block has non-inverting input, its clocking should be set to "swapped". This changes input sampling phase to ϕ 1, resulting in proper operation. ADC may need additional "normal" setting, contrary to ordinary "swap".

IV. Experimental Results and Evaluation

A. *Waveforms*

Fig. 4 show an example of *v* (upper, red) and *w* (lower, blue) waveforms, where the time axis is 10ms /div.

B. *X-Y Plots*

Usually, behavior of FitzHugh-Nagumo model is investigated with the X-Y plot of *v* and *w*. Subfigures of Fig. 5 show some cases for different values of *a* and *b*. These correspond well to the well-known FitzHugh-Nagumo operation modes.

C. *Evaluation from the Viewpoint of Space and Cost*

The dpASP implementation [4] needs two dpASP chips to emulate one neuron. In contrast, our proposal can pack two neurons into one PSoC, as just described. PSoC is cheaper than dpASP, as well. Table 1 compares the two implementations, revealing our advantage over dpASP case.

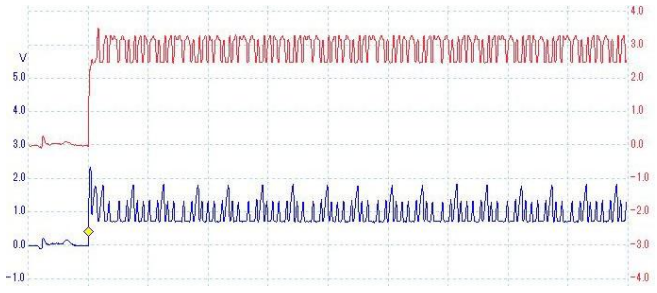

Fig. 4 Sample *v* and *w* waveforms

(a) b = 100

(b) b = 10

(c) a = 10

(d) a = 20

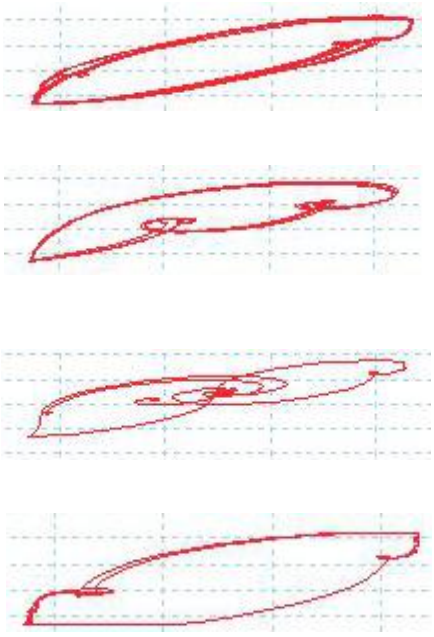

Fig. 5 X-Y Plots for some values of *a* and *b*

TABLE I. dpASP vs PSoC

LSI type	# of chip per model	Cost (USD) per model
dpASP	2	24
PSoC	0.5	1.7

V. Conclusion

As an analog electronic implementation of the FitzHugh-Nagumo neuron model, PSoC analog FPGA from Cypress is made use of. With optimal circuit configuration, it features advantage by factors of 4 for space and 15 for cost. These effectiveness will benefit cases where many neurons are used to form some complicated system for AI.

References

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