Application Report
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PWM DAC Using MSP430 High-Resolution Timer

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ABSTRACT

The digital-to-analog converter (DAC) generates an analog output that is proportional to the digital input it receives. The pulse width modulation (PWM) DAC is one of the popular techniques to implement DAC functionality in MCUs that don't have an integrated DAC module. The PWM DAC approach is not new, but performance limitations have historically confined its use to low-resolution, low-bandwidth applications. This application report focuses on achieving increased DAC performance by using the MSP430™ Timer_D high-resolution mode. It also discusses PWM DAC design considerations, duty-cycle limitations of the Timer_D high-resolution mode and its effects on the PWM DAC performance, and supply-voltage drift compensation in PWM DAC applications.

Project collateral and associated source discussed in this application report can be downloaded from the following URL: http://www-s.ti.com/sc/techlit/slaa497.zip.

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1 What is PWM DAC?

PWM or Pulse Width Modulation is a form of signal modulation where data is represented by the ratio of the ON time to the period (also known as the duty cycle). A given ON time corresponds to an average DC voltage, which is linearly proportional to the duty cycle (see Figure 1).

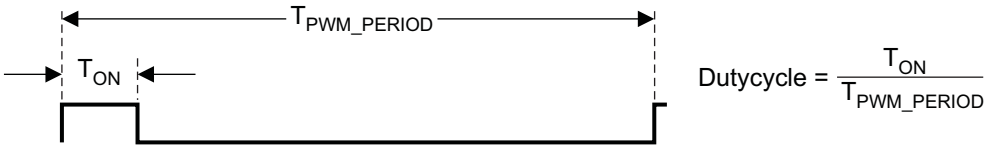


Figure 1. PWM Signal With Variable Duty Cycle

Where,

T_{ON} is the ON period

T_{PWM_PERIOD} = PWM period

MSP430 timer compare blocks in conjunction with the various output modes can be used to generate these variable duty cycle PWM signals. For more details on how to generate these PWM signals using MPS430, see the Timer section in the *MSP430x5xx/MSP430x6xx Family User's Guide* (SLAU208).

For implementing the PWM DAC, either the PWM period is fixed and the duty cycle is varied or vice versa. In some cases, both parameters must vary to achieve the required DAC output. In this application, the PWM DAC implementation with fixed PWM period and variable duty cycles are considered.

On passing the PWM signal through a low-pass filter (LPF), a dc voltage with reasonable ripple is generated. The ripple is caused by the charging (during PWM ON time) and discharging (during PWM OFF time) of the filter capacitors (see Figure 2). This ripple represents the first harmonic of the filter and is of the same frequency of the PWM signal. Integer multiples of this PWM frequency form the higher order harmonics in the system.

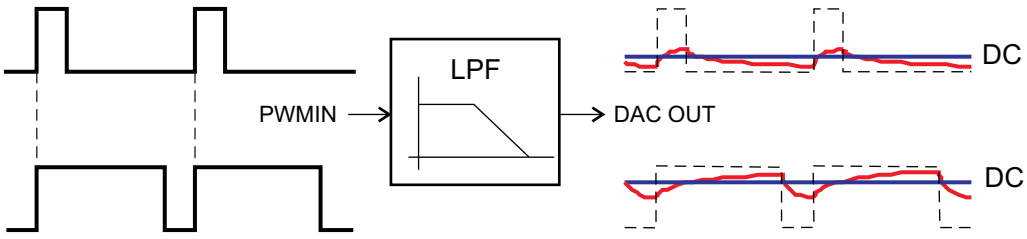


Figure 2. PWM DAC Implementation

The PWM DAC resolution is dependent on this harmonic ripple generated by the LPF and the duty-cycle resolution. These PWM DAC parameters are discussed in detail in Section 2.

2 PWM DAC Performance Parameters

This section discusses the PWM DAC parameters that affect the PWM DAC resolution and the tradeoffs between these parameters to achieve the best PWM DAC resolution.

2.1 Duty-Cycle Resolution

DAC resolution is the smallest increment in the analog output voltage that corresponds to an increment in the DAC digital count. In the case of the PWM DAC, the smallest increment in the output voltage level is achieved by incrementing the PWM duty-cycle value. Therefore, in the case of PWM DAC, PWM duty-cycle resolution directly represents the DAC resolution.

Consider,

- f_{PWM} = frequency of the PWM signal that is input to the LPF. This f_{PWM} signal is generated using a timer module in an MCU.
- f_{CLOCK} = frequency of the timer clock source that is used as a timer tick to increment the timer counter.

Then, the relation between f_{PWM}, f_{CLOCK} and PWM DAC duty-cycle resolution is:

$$2^N = \frac{f_{CLOCK}}{f_{PWM}} = \text{\#PWM Duty cycle Steps} = \text{\#DAC Output Levels} \quad (1)$$

where, N = duty-cycle resolution of PWM DAC in bits

NOTE: For a detailed discussion regarding the frequency selection design considerations of PWM DAC applications, see Appendix A.

In Figure 3, f_{CLOCK} = 8 x f_{PWM}. There are eight f_{CLOCK} periods within one f_{PWM} period. Therefore, the PWM duty cycle and the DAC output can be varied in eight levels = 2^3, which corresponds to 3 bits of resolution.

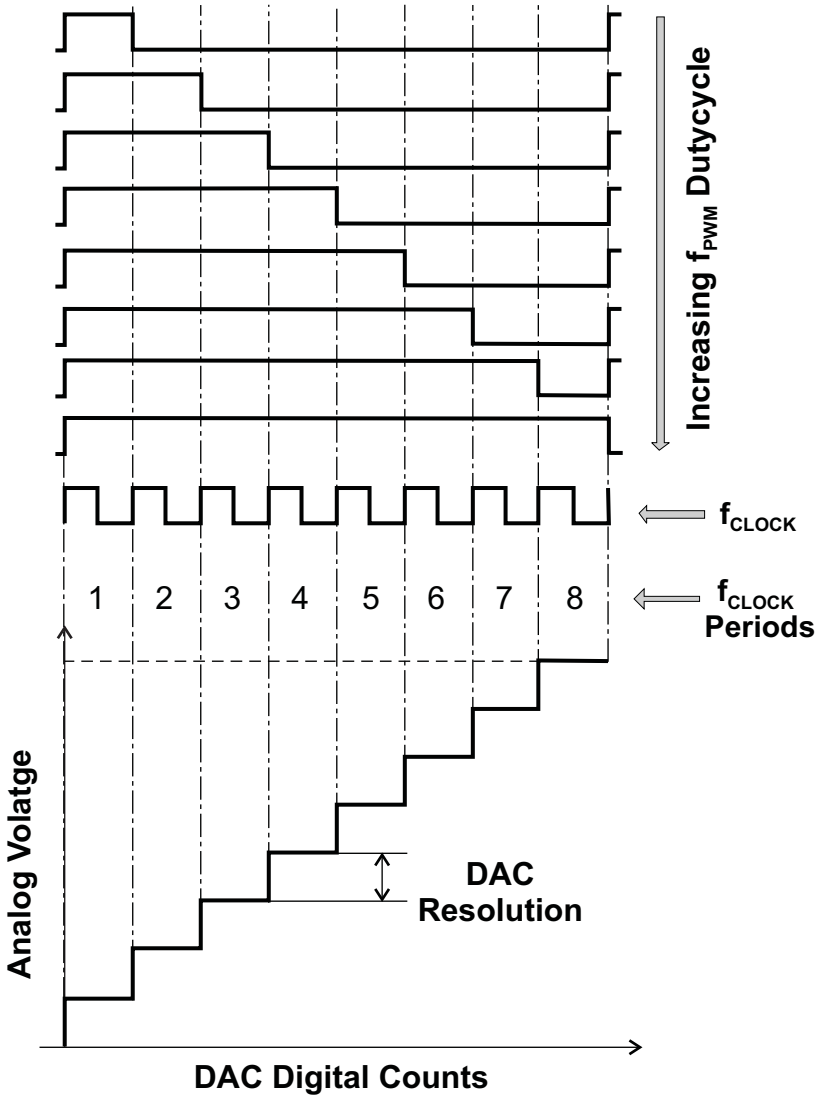


Figure 3. PWM DAC - Duty-Cycle Resolution

According to Equation 1, in order to increase the PWM DAC resolution, either the f_{CLOCK} should be increased or f_{PWM} should be decreased. However, higher f_{PWM} frequencies are required to lower the complexity of the external low-pass filter circuitry. Higher order filters require more external components, which in turn increases system cost and space. And, reducing the order of the low-pass filter affects the DAC bandwidth. This is discussed in more detail in Section 2.3. So the limiting factor for achieving higher duty-cycle resolution with higher f_{PWM} frequency is the PWM timer clock source, f_{CLOCK}.

MSP430 devices with regular timers (Timer_A/Timer_B) can be clocked by the maximum clock frequency that equals the device clock frequency (16 MHz on F2xx devices and 25 MHz on F5xx/F6xx devices). However, with the high-resolution timer generator present on the Timer_D module, timer clock frequencies up to 256 MHz can be generated and this helps achieve higher duty-cycle resolution for a given f_{PWM} frequency.

Figure 4 shows the PWM DAC duty-cycle resolution (in bits) vs f_{PWM} for various f_{CLOCK} frequencies (16 MHz, 25 MHz, 128 MHz and 256 MHz).

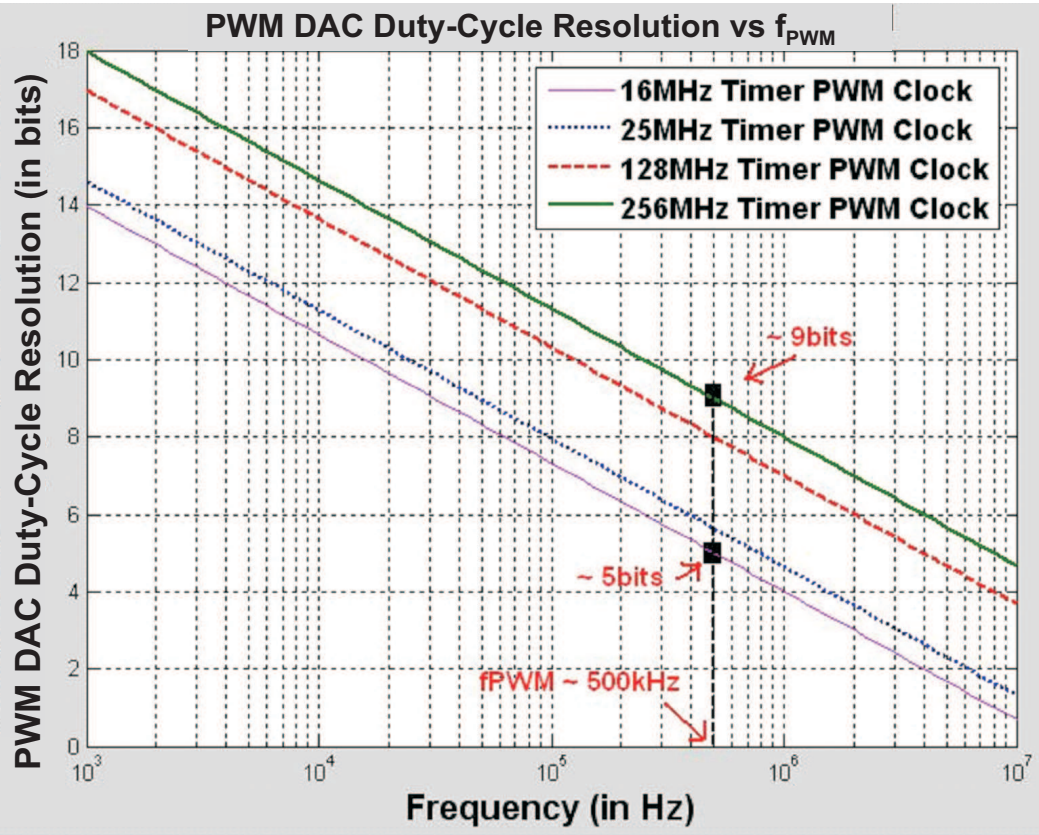


Figure 4. PWM DAC Duty-Cycle Resolution vs f_{PWM} Frequency

In Figure 4, it can be seen that there is a clear tradeoff between the PWM DAC duty-cycle resolution and the f_{PWM} frequency. That is, the higher the f_{PWM} frequency, the lower the DAC resolution achieved for a given f_{PWM} frequency; it can be seen that the higher duty-cycle resolution can be achieved by increasing the timer clock or f_{CLOCK} frequency.

On MSP430 devices with the Timer_D module, f_{CLOCK} frequencies of up to 256 MHz can be generated using the high-resolution generator, and in Figure 4 it can be seen that for a given PWM frequency, f_{PWM} = 500 kHz, f_{CLOCK} = 16 MHz yields ~5-bits of DAC duty-cycle resolution and f_{CLOCK} = 256 MHz yields higher DAC duty-cycle resolution, which is ~9-bits of resolution.

2.2 Harmonic Ripple and Total Uncertainty of the DAC Output:

As discussed in Section 2.1, duty-cycle resolution of the PWM signal is one of the main factors that affect the DAC resolution. The other important factor is the harmonic distortion that is caused by the harmonics (not filtered by the low-pass filter) that are used in the PWM DAC application.

Harmonics are the integer multiples of the fundamental frequency and insert, in the case of the PWM DAC application, harmonics are the integer multiples of the f_{PWM} frequency. For frequency analysis of the PWM signal and its high frequency harmonic components, see *Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller* (SPRAA88).

In the case of PWM DACs, the unfiltered harmonics can be measured as the peak-to-peak ripple at the filter output. The harmonic ripple amplitude on the filter output gets higher as the fundamental frequency gets closer to the filter cutoff frequency.

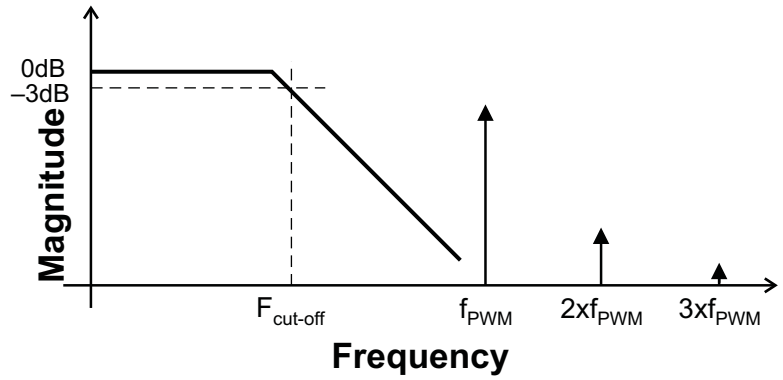


Figure 5. Filter Frequency Response and Harmonics

Figure 5 shows that the harmonic ripple can be reduced by either increasing the stop band roll-off rate or decreasing the filter cut-off frequency of the analog low-pass filter or by increasing the f_{PWM} frequency. Increasing the stop band roll-off rate is achieved by the complex higher-order filter circuitry, which impacts the system cost. Decreasing the filter cut-off frequency implies decreasing the DAC bandwidth or the signal bandwidth. And, increasing the f_{PWM} frequency affects the PWM DAC duty-cycle resolution, which encompasses the existing PWM DAC limitations.

The sum of the duty-cycle resolution and harmonic ripple at the filter output yields the total uncertainty of the PWM DAC output. Figure 6 shows the graphical representation of the same.

Total uncertainty of DAC output = harmonic ripple + PWM duty-cycle resolution

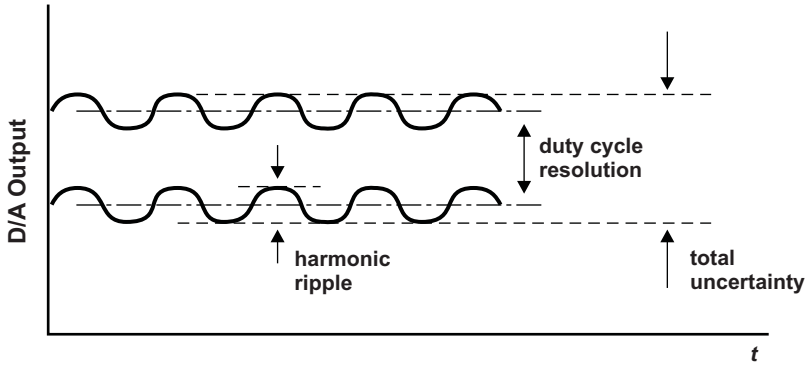


Figure 6. PWM DAC Output – Total Uncertainty

So far, the effects of increasing/decreasing f_{PWM} frequency on PWM DAC resolution parameters have been discussed: harmonics ripple and duty-cycle resolution. In conclusion, the optimal f_{PWM} frequency is the one where the total uncertainty of the DAC output is smallest. Section 3 shows simulation and experimental curves that indicate optimum f_{PWM} frequency for a given f_{CLOCK} frequency.

2.3 Analog Filter Design

The PWM DAC performance, where the f_{PWM} carrier frequency is required to be filtered off by the analog low-pass filter to output a steady analog voltage, is heavily dependent on the design and selection of the analog low-pass filter.

In this application report, passive filters that offer low cost, reduced complexity, and assured stability compared to active filters are considered for generating simulation and experimental data.

The first and second order low-pass filter transfer function equations are:

Transfer function of first order filter: $\frac{Vout(s)}{Vin(s)} = \frac{1}{\tau s + 1}$

where, T = time constant in seconds

And, the transfer function of the second order filter is: $\frac{Vout(s)}{Vin(s)} = \frac{\omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}$

where, ω_n = un-damped natural frequency and ζ = damping ratio

Table 1 shows the first and second order RC/RLC filter responses that are chosen to compare the PWM DAC performances using the normal and high-resolution timer modes.

Table 1. First and Second Order Passive Low-Pass Filter Designs

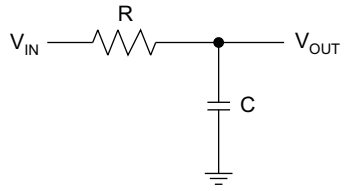
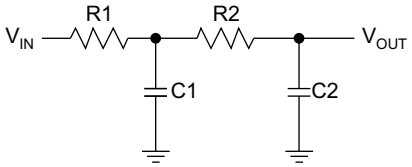
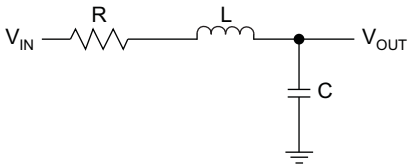
Filter Order	Low Pass Filter Circuit	Stop Band Roll-Off Rate (in dB/ decade)	Filter Bandwidth (in rad/s)	Damping Ratio (ζ)
1st		-20	$BW = \frac{1}{\tau}$ $where, \tau = RC$	-
2nd		-40	$BW = \omega_n\left(\left(1-2\xi^2\right)+\sqrt{4\xi^4-4\xi^2+2}\right)^{1/2}$ $\omega_n = \frac{1}{\sqrt{R_1R_2C_1C_2}}$	$\xi = \frac{(R_1C_1 + R_1C_2 + R_2C_2)}{2\sqrt{R_1C_1R_2C_2}}$
2nd		-40	$BW = \omega_n\left(\left(1-2\xi^2\right)+\sqrt{4\xi^4-4\xi^2+2}\right)^{1/2}$ $\omega_n = \frac{1}{\sqrt{LC}}$	$\xi = \frac{R}{2}\cdot\sqrt{\frac{C}{L}}$

Table 2 shows the filter designs used in the simulation analysis of the effective PWM DAC resolution vs. f_{PWM} frequency at various f_{CLOCK} frequencies.

Table 2. Low-Pass Filters Used in Simulation Analysis

Filter #	Filter Order	BW (in kHz)	Damping Ratio (ζ)	$\tau = \frac{1}{(2\pi \times BW)}$	Transfer Function Coefficient b = Numerator coefficient a = Denominator coefficient
1	1st	10	-	0.0000159	b = [1] a = [0.0000159 1]
2	1st	20	-	0.000008	b = [1] a = [0.000008 1]

Filter #	Filter Order	BW (in kHz)	Damping Ratio (ζ)	$\omega_n = (2\pi \times BW)$ (in rad/sec)	Transfer Function Coefficient b = Numerator Coefficient a = Denominator Coefficient
3	2nd	10	0.707	62830	b = [62830*62830] a = [1 2*0.707*62830 62830*62830]
4	2nd	20	0.707	125663	b = [125663*125663] a = [1 2*0.707*125663 125663*125663]

Filter #	Filter Order	BW (in kHz)	Damping Ratio (ζ)	$\omega_n = (2\pi \times BW)$ (in rad/sec)	Transfer Function Coefficient b = Numerator Coefficient a = Denominator Coefficient
5	2nd	50	0.707	314159	b = [314159*314159] a = [1 2*0.707*314159 314159 *314159]
6	2nd	100	0.707	628318	b = [628318*628318] a = [1 2*0.707*628318 628318*628318]

Figure 7 shows the MATLAB simulations of the magnitude and phase response of all the filter designs listed in Table 2. From the first order (filter #1,2) and second order (filter #3,4,5,6) filter responses, it can be seen that higher order filters have better faster stop band roll-off rates, but longer phase delays.

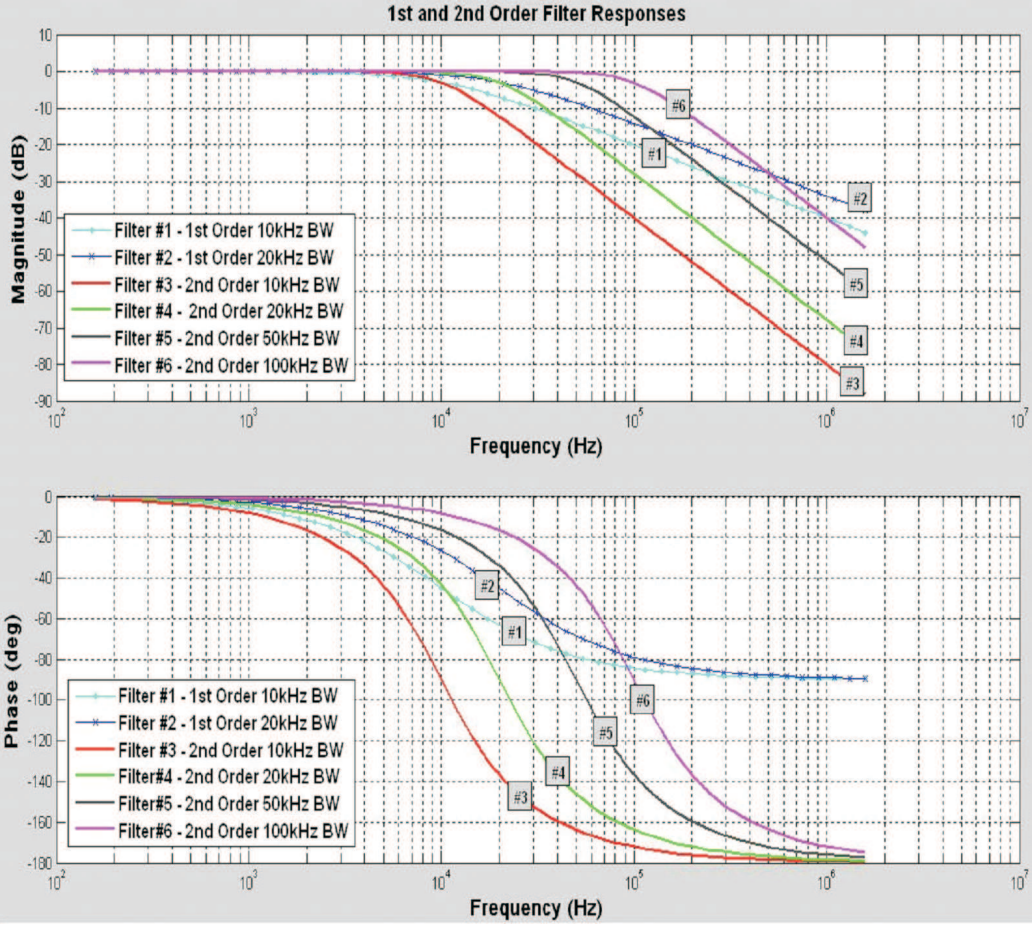
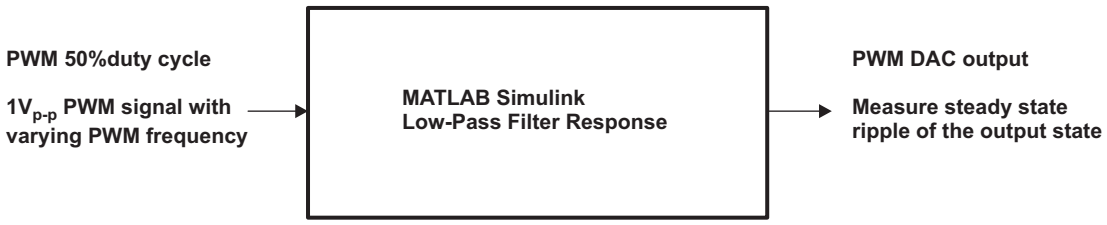


Figure 7. Magnitude and Phase Response of Analog Filters Listed in Table 2

3 PWM DAC Resolution – Simulation Analysis

This section discusses the PWM DAC effective resolution (which includes ripple uncertainty due to harmonic distortion plus duty-cycle resolution) simulation analysis with and without the high-resolution timer mode.

Harmonic distortion includes infinite summation of integer multiples of the fundamental frequency, and is theoretically challenging to compute. Therefore, in this case MATLAB/Simulink was used to determine the steady state ripple of the low-pass filter outputs and, then, applied towards the effective PWM DAC resolution analysis.



The PWM signal of $1V_{p-p}$ amplitude and 50% duty cycle (1) is input to the MATLAB/Simulink low-pass filter block, and the ripple voltage on the steady state PWM DAC output is measured. Ripple uncertainty of the DAC output for a given is:

$$f_{PWM}\ \text{frequency} = \frac{\text{PWM DAC Steady State Output Ripple}}{1V_{p\text{-}p}\ \text{PWM Amplitude}} = \frac{V_{ripple}}{V_{p-p}} \quad (2)$$

And, the duty cycle uncertainty of PWM DAC for a given f_{PWM} frequency = $\frac{f_{PWM}}{f_{CLOCK}}$

Summing ripple uncertainty and duty-cycle uncertainty gives the total uncertainty.

Total uncertainty = ripple uncertainty + duty-cycle uncertainty

$$\text{Total uncertainty} = \frac{V_{ripple}}{V_{p-p}} + \frac{f_{PWM}}{f_{CLOCK}}$$

The effective DAC resolution is given by:

$$\text{Effective DAC resolution (in bits)} = \log_2\left(\frac{1}{\text{Total Uncertainty}}\right) = \log_2\left(\frac{1}{\left(\frac{V_{ripple}}{V_{p-p}} + \frac{f_{PWM}}{f_{CLOCK}}\right)}\right) \quad (3)$$

Figure 8 to Figure 13 show the effective PWM DAC resolution vs. f_{PWM} frequency at different f_{CLOCK} frequencies for various low-pass filter responses listed in Table 2.

It can be seen that DAC resolution at lower f_{PWM} frequencies is affected by the ripple uncertainty. And, at higher f_{PWM} frequencies it is evident that the duty-cycle resolution affects the effective PWM DAC resolution. At f_{PWM} frequencies lower than the filter cut-off frequency, the ripple magnitude is very high (as the first harmonic goes completely unfiltered), therefore, the effective PWM DAC resolution converges to zero. For a given f_{CLOCK} frequency, the optimum f_{PWM} frequency is where the DAC resolution curve peaks.

On comparing the high-resolution f_{CLOCK} curves (f_{CLOCK} = 128 MHz and 256 MHz) with the normal timer f_{CLOCK} curves (f_{CLOCK} = 16 MHz and 25 MHz), it is evident that using the high-resolution clock as the PWM timer clock source yields more resolution compared to the regular clock source. For example, using Filter#4 in Figure 11 (second order LPF with 20 kHz bandwidth), the maximum effective PWM DAC resolution using normal timer mode (with f_{CLOCK} = 16 MHz) is ~6 bits and when f_{CLOCK} = 256 MHz in high-resolution mode is used, the effective DAC resolution that can be achieved is ~9 bits. In this case, the high-resolution timer mode helps achieve ~3 additional bits of DAC resolution when compared to normal-timer mode.

(1) 50% duty cycle of the PWM input signal maximizes the energy of the n=1 harmonic. Refer to the *Appendix* section in *Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller* (SPRAA88), which shows the worst case duty-cycle derivation.

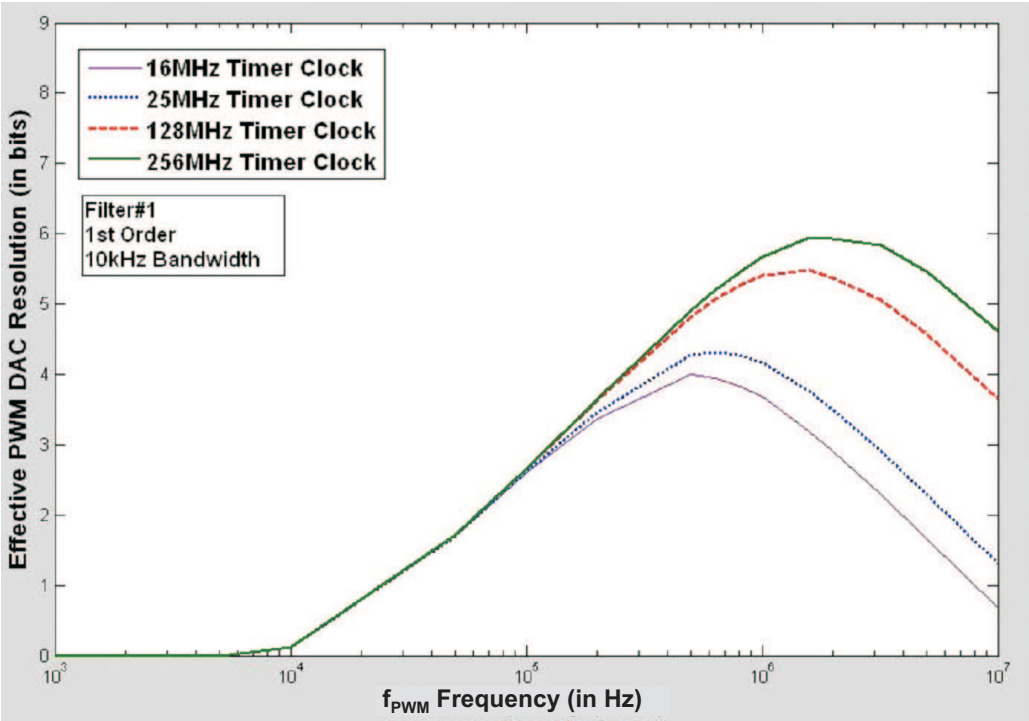


Figure 8. Effective PWM DAC Resolution vs. f_{PWM}, Filter #1 (Simulation)

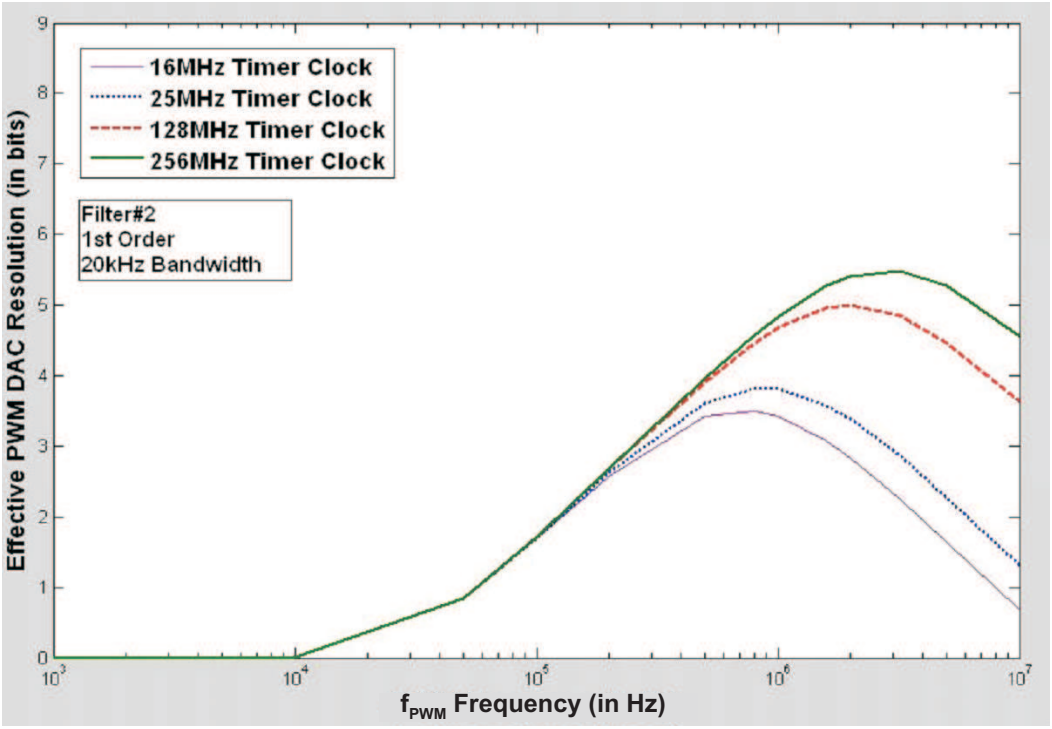


Figure 9. Effective PWM DAC Resolution vs. f_{PWM}, Filter #2 (Simulation)

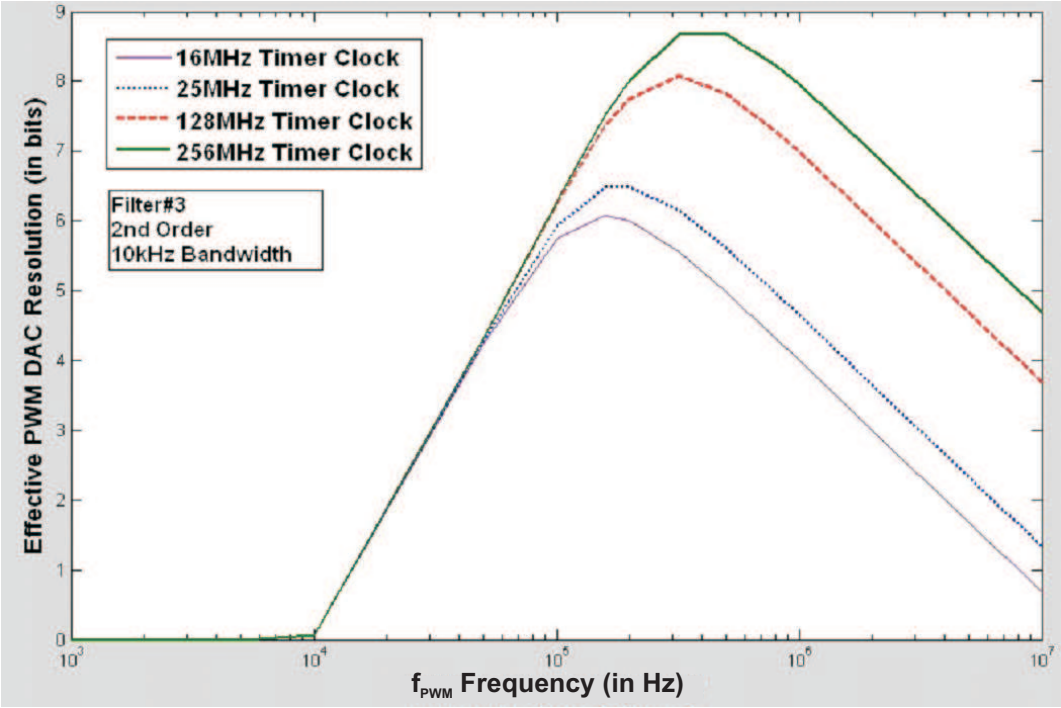


Figure 10. Effective PWM DAC Resolution vs. f_{PWM}, Filter #3 (Simulation)

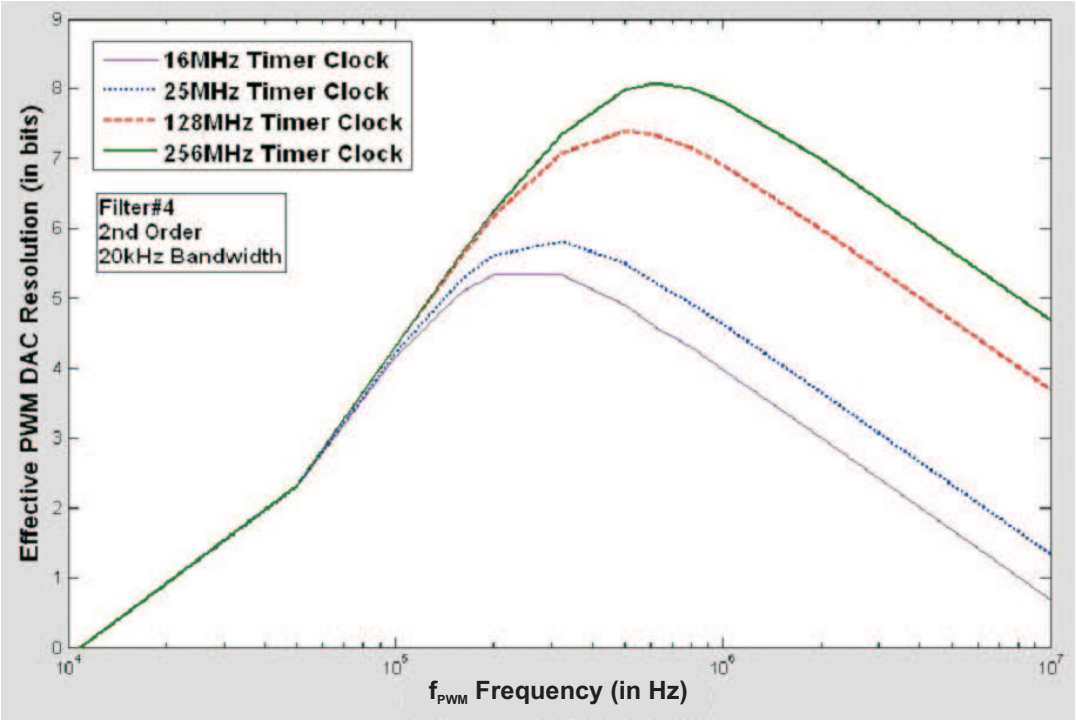


Figure 11. Effective PWM DAC Resolution vs. f_{PWM}, Filter #4 (Simulation)

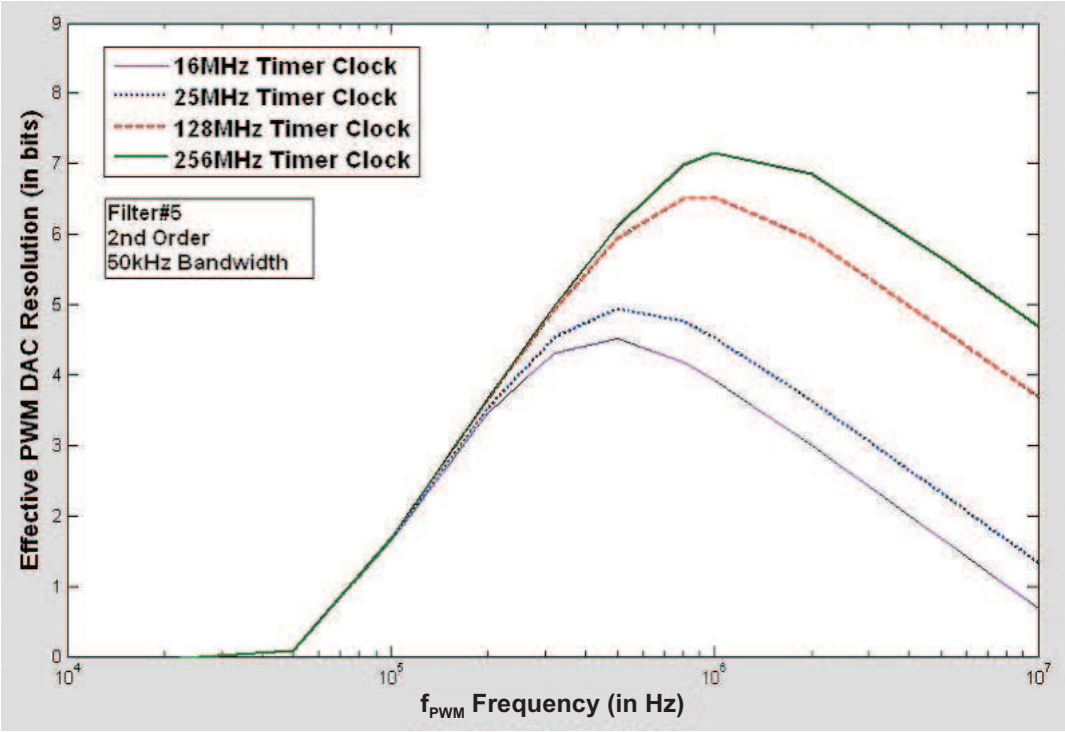


Figure 12. Effective PWM DAC Resolution vs. f_{PWM}, Filter #5 (Simulation)

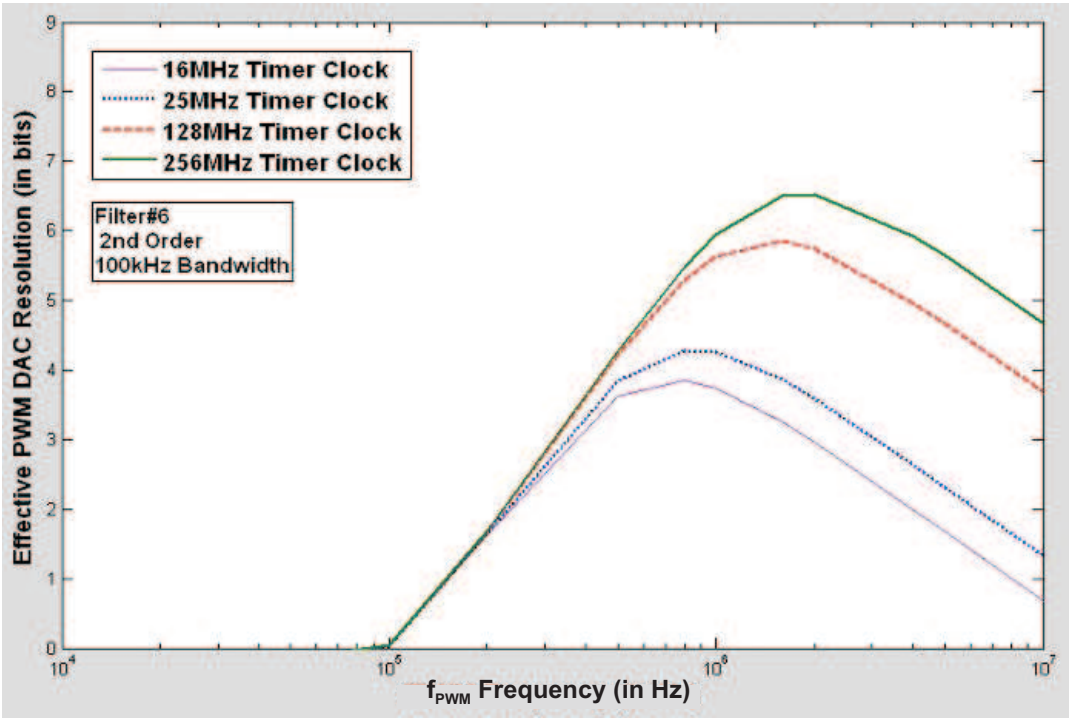


Figure 13. Effective PWM DAC Resolution vs. f_{PWM}, Filter #6 (Simulation)

4 PWM DAC – Experimental Test Set-up and Analysis

Tests were conducted to ensure the experimental data matches the simulation results obtained in Section 3. Table 3 lists the filter designs that were implemented for the experimental test analysis.

Table 3. Low Pass Filter Designs Used in Experimental Test Set-Up

Filter #	Filter Order	RC Component Values	t = RC	$BW = \frac{1}{\tau}$ $where, \tau = RC$ (in rad/s and Hz)
2	1st	R = 1.69kΩ C = 4.7 nF	7.94 µs	125.9k rad/s 20.037 kHz

Filter #	Filter Order	RC Component Values	Damping Ratio $\xi = \frac{(R_1C_1 + R_1C_2 + R_2C_2)}{2\sqrt{R_1C_1R_2C_2}}$	$\omega n = \frac{1}{\sqrt{R_1R_2C_1C_2}}$ (in rad/s)	$BW = \omega_n\left(\left(1-2\xi^2\right) + \sqrt{4\xi^4 - 4\xi^2 + 2}\right)^{1/2}$ (in rad/s and Hz)
4	2nd	R1 = 51 Ω R2 = 5.11 kΩ C1 = 10 0nF C2 = 1 nF	1.005	195.88k	126.07 krad/s 20.06 kHz

Filter #	Filter Order	RLC Component Values	Damping Ratio $\xi = \frac{R}{2}\cdot\sqrt{\frac{C}{L}}$	$\omega n = \frac{1}{\sqrt{LC}}$ (in rad/s)	$BW = \omega_n\left(\left(1-2\xi^2\right) + \sqrt{4\xi^4 - 4\xi^2 + 2}\right)^{1/2}$ With ζ = 0.707, BW = ωn (in rad/s and Hz)
6	2nd	R = 45.3 Ω L = 100 µH C = 100 nF	~0.707	316.22k	316.22k rad/s 50.3 kHz

4.1 Effective PWM DAC Resolution

In the experimental set-up, PWM signal of $3V_{p-p}$ and 50% duty cycle was generated from the MSP430 and input to filters listed in Table 3. The ripple on the PWM DAC output voltage was measured to calculate the ripple uncertainty. The f_{PWM} frequency was varied from 10 kHz to 5 MHz to generate the effective DAC resolution curves for both the normal and high-resolution timer clocks used as PWM timer clock source (f_{CLOCK}).

Figure 14 to Figure 16 show the experimental data of the effective PWM DAC resolution vs. f_{PWM} frequency at different f_{CLOCK} frequencies for various low-pass filter responses listed in Table 3. From the experimental analysis, it is evident that the experimental and simulation data match very closely.

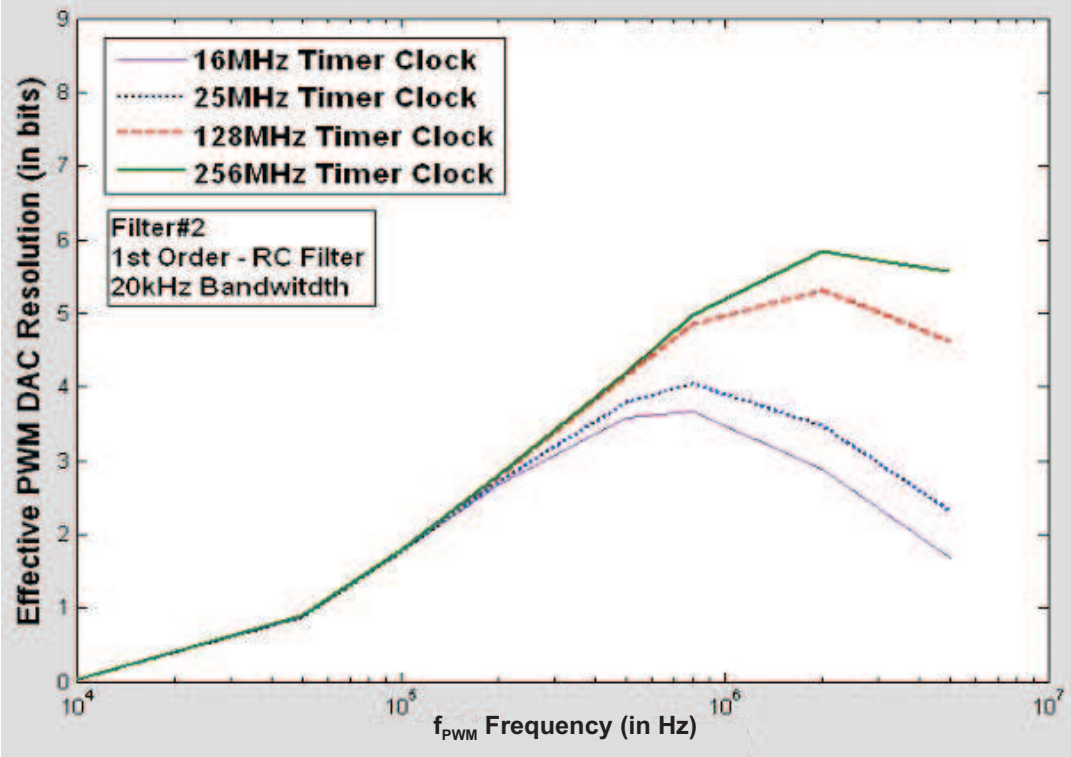


Figure 14. Effective PWM DAC Resolution vs. f_{PWM}, Filter #2

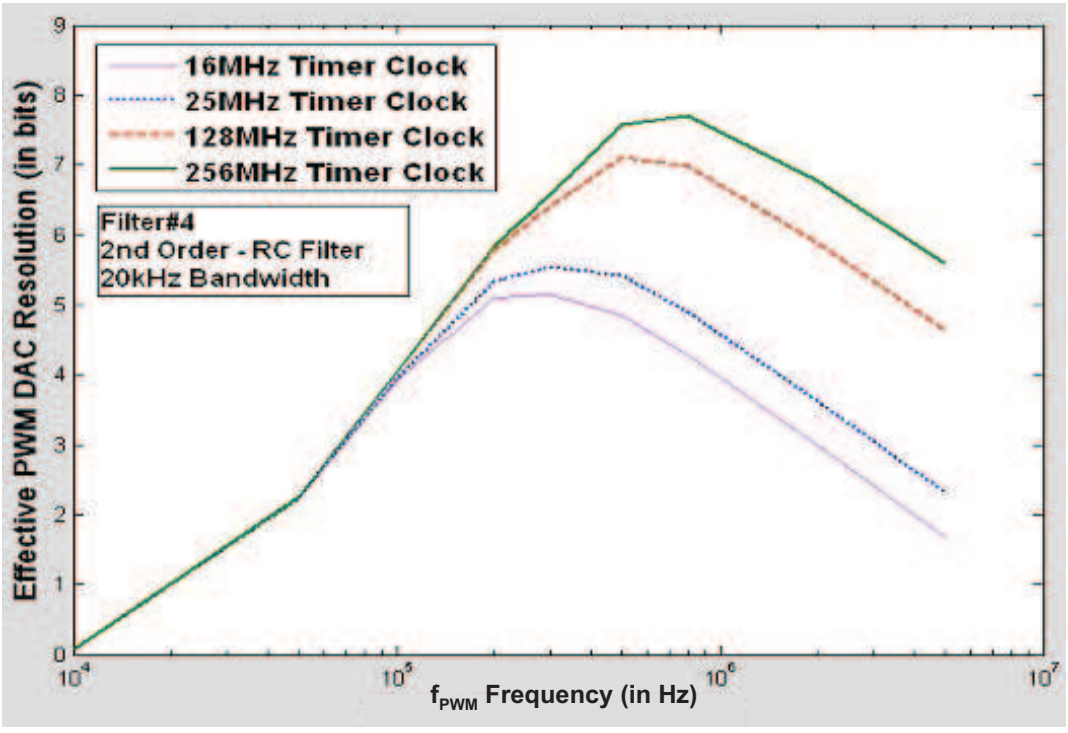


Figure 15. Effective PWM DAC Resolution vs. f_{PWM}, Filter #4

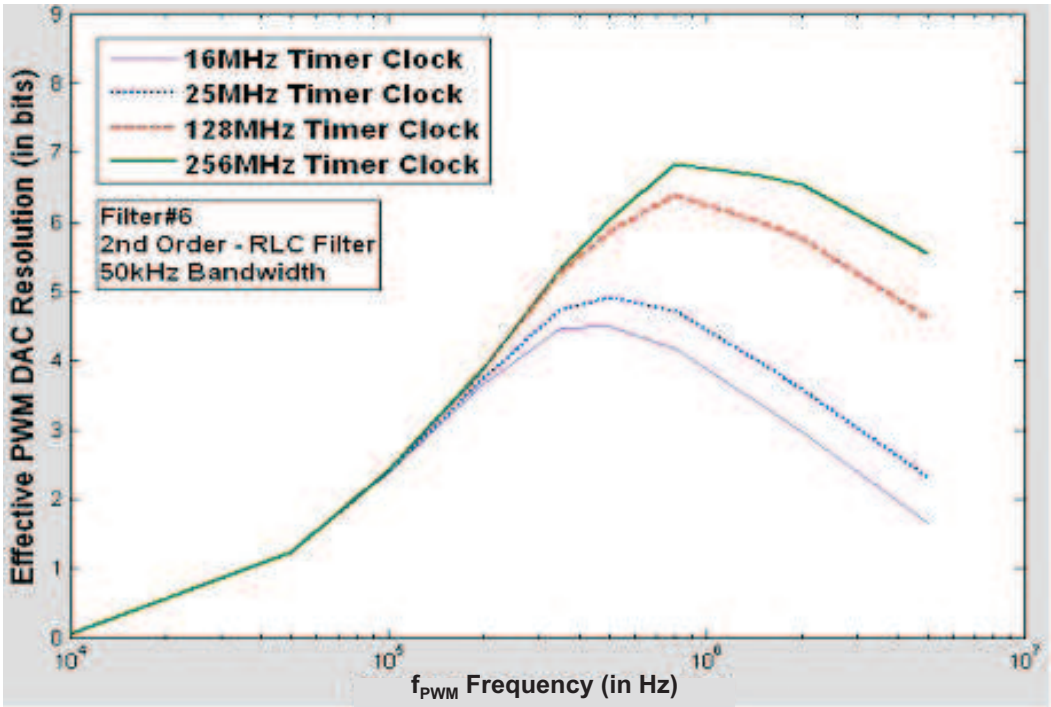


Figure 16. Effective PWM DAC Resolution vs. f_{PWM}, Filter #6

4.2 Monotonicity

Monotonicity refers to the ability of DAC analog output to move only in the same direction as the digital input code – that is, increase analog output voltage level with increase in input code and decrease analog output voltage level with decrease in input code. Figure 17 (a) and (b) show PWM DAC monotonicity curves where the PWM duty cycle was varied from 0 to maximum duty cycle value and vice versa. The DAC output voltage changes in only one direction. For this test case, Filter #4 with f_{PWM} = 512 kHz, f_{CLOCK}= 256 MHz and f_{update} = 8 kHz is used.

It can be seen that at PWM minimum and maximum duty cycles, the high-resolution timer reverts back to the default state of the timer PWM output mode. This is a known limitation of the Timer_D high-resolution mode and is discussed in more detail in Section 5.

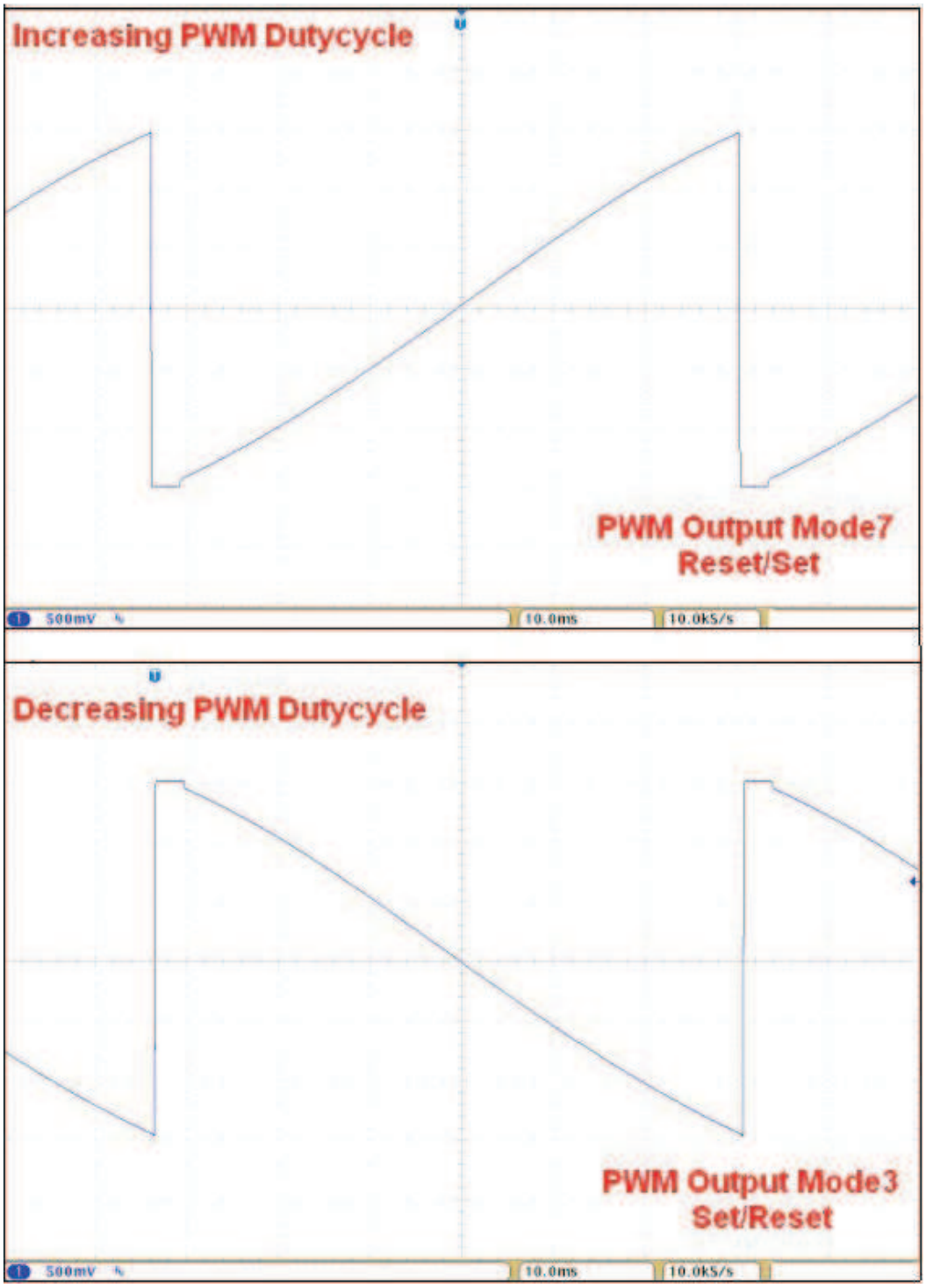


Figure 17. PWM DAC Monotonicity (a) Increasing PWM Duty Cycle (b) Decreasing PWM Duty Cycle

4.3 Settling Time

Settling time is the time taken for the DAC output voltage to settle, starting from when the input code changes. The DAC settling time should be less than the DAC update rate.

Figure 18 shows the worst case settling time of the PWM DAC when the PWM duty cycle was changed from 0 to maximum duty cycle count (256 MHz/500 kHz = 512 counts) using Filter #4.

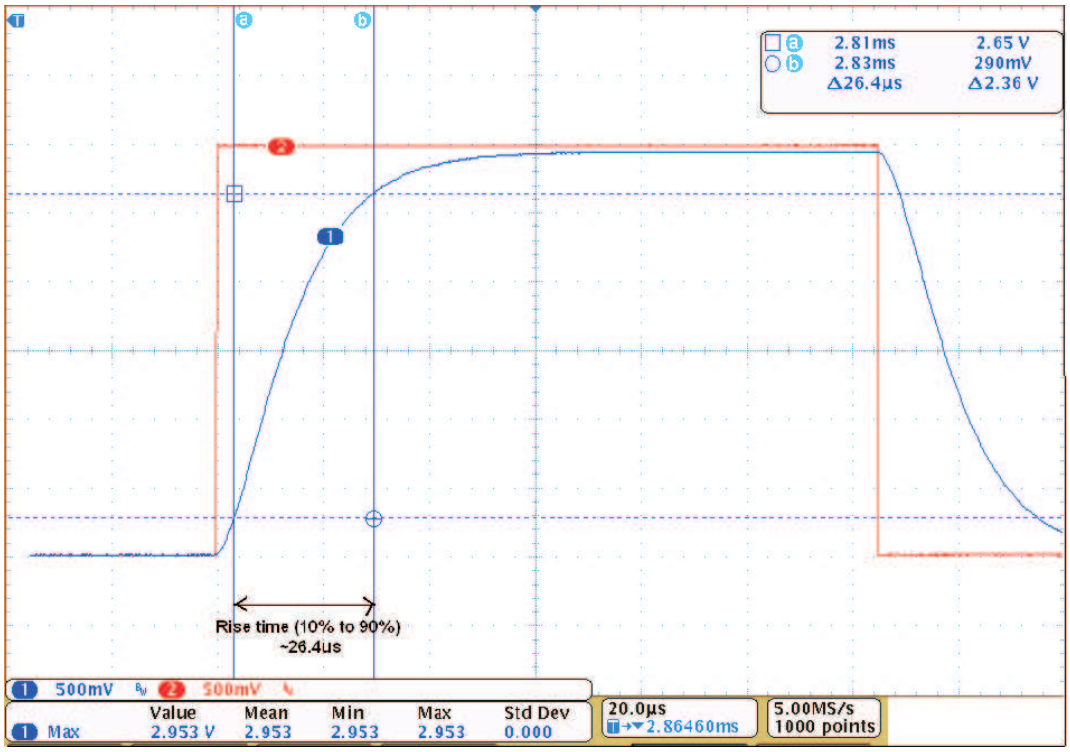


Figure 18. PWM DAC Settling Time

In Figure 18, channel 1 represents the PWM DAC output and channel 2 represents PWM duty cycle count change from 0-100%, which is equivalent to 0 V-3 V PWM DAC change. It can be seen that the maximum DAC output level reached is not equivalent to 100% duty cycle of the PWM signal. This is due to the high-resolution timer generator limitation (discussed in Section 5). Accounting for the high-resolution Timer_D limitation, the maximum voltage level in this case would be [3 V – (8/512) x 3 V] ~ 2.95 V and the rise time of the PWM DAC output (10% to 90% of the final DAC output value) is 0.1*2.95 V = 0.295 V to 0.9*2.95 V = 2.655 V measured is ~26.4 µs.

The settling time for a given filter also represents the maximum updated duty-cycle frequency that can be applied to the PWM signal to ensure the PWM DAC output settles properly every time.

5 Limitations of Timer_D High-Resolution Mode

The Timer_D high-resolution clock is generated by the high-resolution clock generator, which can be operated in either the regulated mode or the free-running calibrated mode. In the regulated mode, a reference input clock is multiplied by the factor of either 8 or 16 (depending on the frequency of the reference clock). For example, 16 MHz reference clock (on-chip DCO clock or externally available clock) multiplied by a factor of 16 generates a 256 MHz high-resolution timer clock. And, in the free-running calibrated mode, the high-resolution clock calibration data (available for 64 MHz, 128 MHz, 200 MHz and 256 MHz) is applied to the high-resolution clock generator to generate the high-resolution timer clock. The multiplication factor of 8 or 16 is also required for the high-resolution clock-generator mode in free-running mode to configure the generator in the right frequency range.

The limitation associated with the Timer_D high-resolution clock generator is that the first 8 or 16 PWM duty cycle counts (depending on whether the multiplication factor of 8 or 16 is used to generate the high-resolution timer clock) and the last 8 PWM duty cycle counts (regardless of the multiplication factor) use the default PWM-output mode state selected for the PWM signal. Figure 19 shows this high-resolution timer limitation at the output of the PWM DAC using Filter #4 (second order RC filter with 20 kHz bandwidth) with f_{PWM} = 512 kHz and f_{CLOCK} = 16 MHz x 16 = 256 MHz. The duty cycle is increased from 0x0 to 0x1FF and then decremented from 0x1FF to 0x0. In this case, the PWM OUTMOD 7 ($\overline{\text{RESET}}$/set) is used, therefore, at minimum and maximum duty cycle counts, the PWM output defaults to the $\overline{\text{RESET}}$ state. Because the high-resolution clock generator is configured using a multiplication factor of 16, the first 16 high-resolution duty cycle counts default to the reset state.

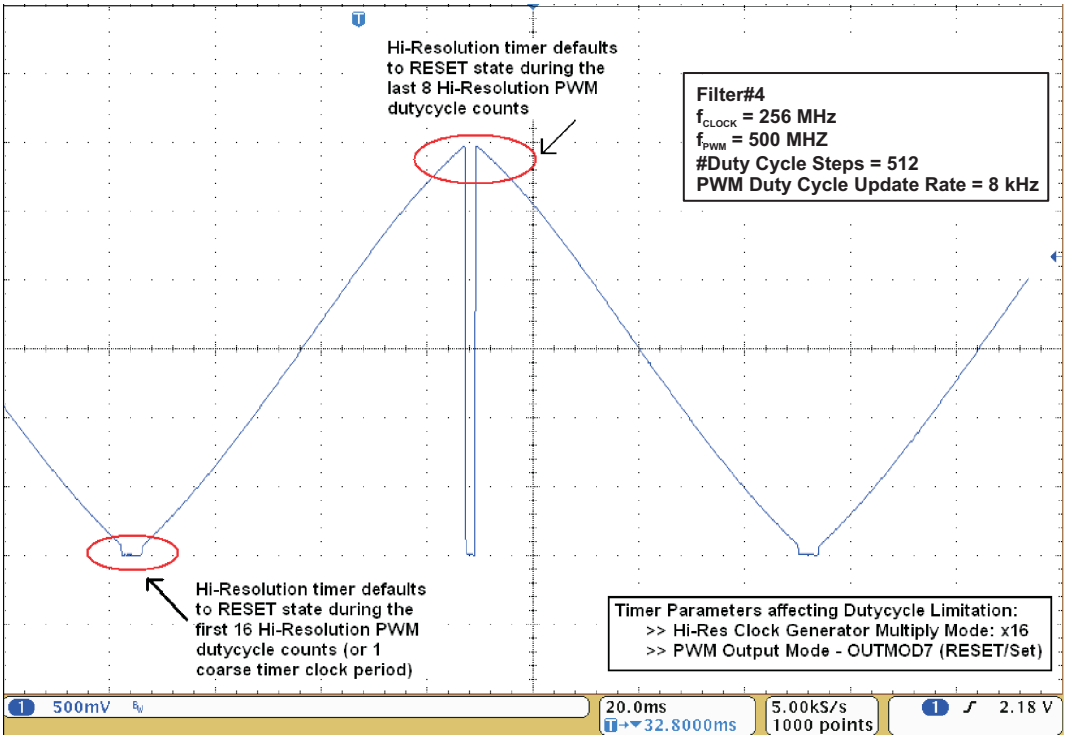


Figure 19. High-Resolution PWM Duty-Cycle Range Limitation Using OUTMOD7

With timer PWM-output mode set to OUTMOD3 (SET/reset), the PWM output defaults to the SET state at the minimum and maximum PWM duty cycle counts (see Figure 20).

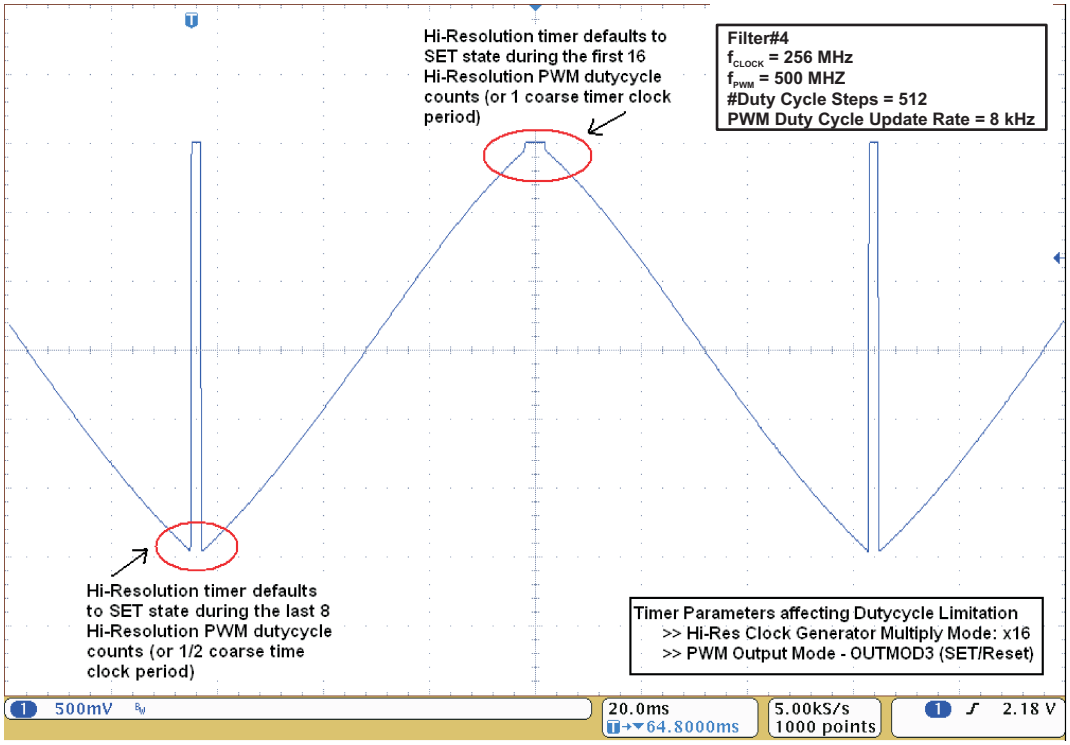


Figure 20. High-Resolution PWM Duty-Cycle Range Limitation Using OUTMOD3

This means there is a loss of resolution at the upper and lower ends of the DAC output range. This reduces the effective full-scale range of the DAC depending on the f_{PWM} frequency used. For example, with f_{CLOCK} = 16 MHz x 16 = 256 MHz, 16 high-resolution duty cycle counts are lost at the upper and lower end of the DAC output range due to this limitation. Table 4 shows that the %FSR of DAC lost due to this limitation increases with increasing f_{PWM} frequencies.

Table 4. Timer_D High-Resolution Limitation: DAC Output FSR vs. f_{PWM}

f_{PWM}	# DAC Output Steps = f_{CLOCK}/f_{PWM}	% FSR of DAC Lost at Lower End of the Range = (16/#DAC Output Steps) x 100	% FSR of DAC Lost at Higher End of the Range = (8/#DAC Output Steps) x 100
100 kHz	2560	0.625%	0.3125%
500 kHz	512	3.125%	1.5625%
1 MHz	256	6.25%	3.125%

This limitation can be accounted for by limiting the digital code and, in turn, the PWM duty cycle range at the minimum and maximum values. In most PWM DAC applications, the entire full scale range of the DAC is not used; in such cases, this limitation would not pose any restriction to the application. For example, in audio applications, most of the digital information is concentrated in the mid range and usually does not have digital information close to minimum/maximum duty-cycle values.

6 Supply-Voltage Drift Compensation

In battery powered applications, the battery charge decays over time. For PWM DAC operations, a steady supply voltage and PWM V_{p-p} signal (that represents a particular DAC output full-scale range) is required.

With the decaying battery charge, the supply voltage drops and, in turn, the V_{p-p} of the PWM signal also drops. In this case, the digital code that is output by the D/A converter will no longer represent the equivalent analog voltage at the PWM DAC output.

This issue can be overcome by either:

- Applying a steady supply voltage to the MSP430, which means an extra regulator is used in the system (adds to system cost) or replace the battery as soon as the battery voltage starts dropping below its nominal value (short battery life)
- Extending the battery life by compensating for the varying supply voltage during runtime

The supply-voltage drift can be compensated for by measuring the supply voltage on occasion and applying an equivalent offset to the digital code in the software if the battery voltage has decayed. In PWM DAC applications, the supply-voltage drift compensation is measured as a factor of the nominal battery voltage and needs to be applied to the digital code runtime. However, with decreasing battery voltage and equivalent drift compensation being applied, the effective full-scale range of the DAC also decreases. For example, if the nominal battery voltage = 3 V (which represents 100% effective FSR of DAC) and if the supply voltage drops to 2.8 V, then the effective %FSR is now 2.8 V/3 V *100 = 93.3% total DAC FSR. As long as this reduced effective full-scale range is still acceptable by the PWM DAC application, the supply-voltage drift compensation can be applied to extend the battery life.

Consider,

$V_{nominal\_supply}$ = nominal battery voltage

V_{supply} = battery voltage at any given instant

Then, the supply-voltage drift compensation ratio is calculated as:

$$\text{Compensation ratio} = \frac{V_{nominal\_supply}}{V_{supply}} \quad (4)$$

Figure 21 shows the effective full-scale range of the PWM DAC for different supply voltage levels with supply-voltage drift compensation applied. Depending on the effective DAC full-scale range acceptable by the PWM DAC application, the supply voltage level to which the battery can decay can be calculated.

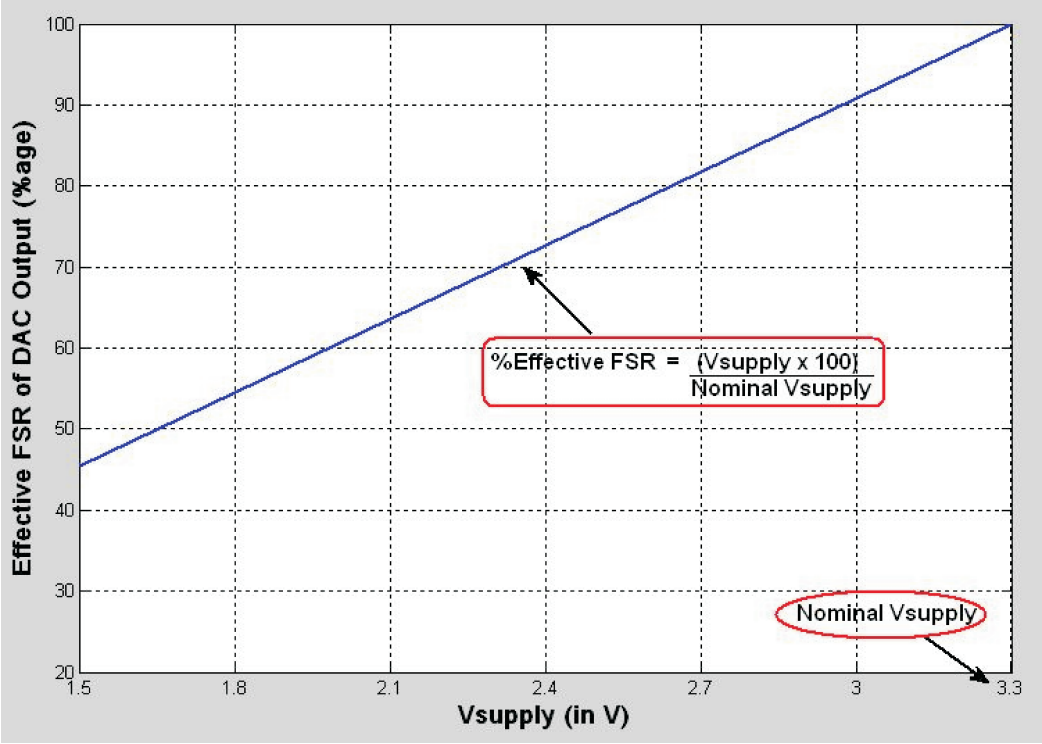


Figure 21. Effective DAC Output Range With Supply-Voltage Drift Compensation

For example, if $V_{nominal\_supply}$ = 3 V and PWM max duty cycle counts = 512, PWM duty cycle count of 256 represents 1.5 V analog. When battery voltage drops to V_{supply} = 2.8 V, PWM duty cycle counts of 256 no longer represents 1.5 V, but is equivalent to (2.8 x 256)/512 = 1.4V. And, in order to compensate for this supply-voltage drift, the digital code of 256 should be multiplied with the compensation ratio = ($V_{nominal\_supply}$/V_{supply}) = 3 V/2.8 V = 1.07. After applying the correction ratio to the digital code, the update digital code is 1.07*256 = 273. Now, the duty cycle count of 273 with V_{supply} = 2.8 V yields a PWM DAC output of (2.8*273)/512 ~ 1.5 V.

Because the MSP430 does not support floating-point numbers, the compensation ratio has to be represented as a fixed-point number multiplied by 10^3 or higher; depending on the number of bits required to represent the mantissa part of the floating-point number.

The supply-voltage drift compensation is applied by multiplying every PWM duty cycle digital code with the compensation ratio. This means a 16x16 unsigned multiply operation is required before every PWM duty cycle update. In order to reduce the number of computation cycles required to apply compensation, the hardware multiplier on MSP430 devices can be used to perform this operation.

Depending on the decay rate of the batteries used in the application, the supply voltage sampling rate can be determined.

7 References

- *MSP430x5xx/MSP430x6xx Family User's Guide* (SLAU208)
- *MSP430F51x1, MSP430F51x2 Mixed Signal Microcontroller Data Sheet* (SLAS619)
- *Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller* (SPRAA88)
- *Using PWM Timer_B as a DAC* (SLAA116)

Appendix A Design Considerations of PWM DAC Frequency Parameters

This section discusses the various frequency parameters that should be considered while designing a PWM DAC application. Figure A-1 below shows the entire A/D to D/A signal path.

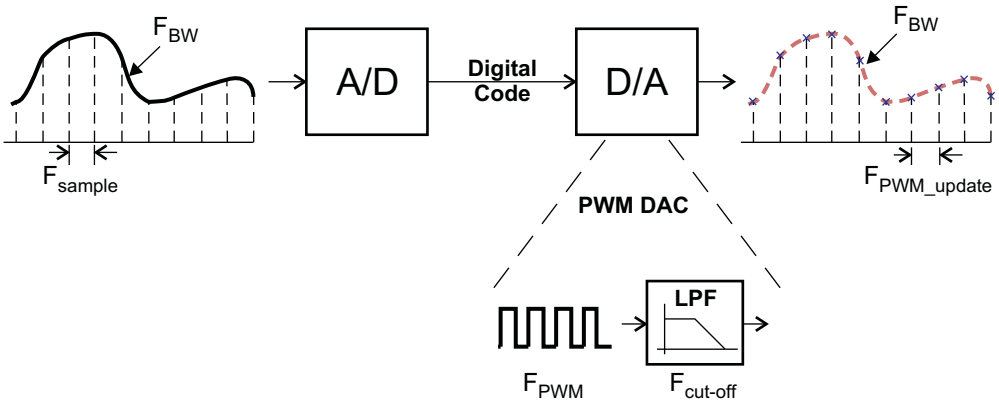


Figure 22. PWM DAC Implementation in A/D and D/A Signal Chain

In the figure above,

f_{BW} = Analog signal bandwidth

f_{sample} = Sampling frequency of the A/D converter

f_{update} = f_{sample} = PWM duty cycle update frequency

f_{PWM} ¬¬ = Frequency of PWM signal input to the low pass filter

$f_{cut\text{-}off}$ = Low pass Filter Cut-off frequency

According to Nyquist criterion, $f_{sample} \geq 2 \times f_{BW}$ **(a)**

And for the PWM DAC operation, relation between f_{PWM} and f_{update} is:

$f_{PWM} \geq f_{update}$ **(b)**

Combining the (a) and (b): $2 \times f_{BW} \leq f_{update}$ OR $f_{sample} \leq f_{PWM}$

And, in order to reproduce the signal at the D/A output, the cutoff frequency of the low pass filter should be atleast the signal bandwidth. That is, $f_{cut\text{-}off} \geq f_{BW}$.

Appendix B Associated Files

Table 5 lists the associated PWM DAC C source files used in this application report. The header files contain the PWM DAC-based frequency configuration values used in the respective .c files.

Table 5. Associated Files – C Source

C Source Files/Folders	Comments
Experimental Ripple Data	Filter2_Ripple.c, Filter4_Ripple.c, Filter6_Ripple.c and Ripple.h. Filter2_Ripple.c, Filter4_Ripple.c, Filter6_Ripple.c and Ripple.h. Ripple.h header file included in all FilterX_Ripple.c files. f_{PWM} value in Ripple.h is varied in order to measure ripple amplitude at output for Figure 14 through Figure 16.
Monotonicity	Monotonicity.c and Monotonicity.h files – Figure 17
Settling Time	Settling.c and Settling.h files – Figure 18
High-Resolution Mode Limitation	Limitation.c and Limitation.h files – Figure 19 and Figure 20

In Monotonicty, settling time and high-resolution mode limitation codes, Timer_A0 is used as an interval timer used to update the duty-cycle value of the PWM signal used for PWM DAC operation. Respective Timer_D PWM duty-cycle values are updated within the Timer_A0 ISR. The high-resolution timer clock is generated by using Timer_D high-resolution generator in the regulated mode using the DCO clock as the reference clock input.

The timer PWM signals that have been used in the C source files for various filters have been selected per the schematic file *PWM DAC Board.pdf* (also included in the zip folder).

Table 6 lists the MATLAB source files used in the simulation analysis.

Table 6. Associated Files – MATLAB Source

MATLAB Files/Folder	Comments
Filter_Responses.m	First and second order filter response curves (magnitude and phase responses) - Figure 7
Duty cycle_Resolution.m	PWM DAC duty-cycle resolution with high-resolution and normal timer modes – Figure 4
Effective PWM DAC Resolution Folder: • d2a_order2.mdl • minmax.m • xOrder RC - ykHz BW.txt • xOrder RC - ykHz BW.xls • x_Order_RC_ykHz_BW.m	This folder contains the MATLAB Simulink file d2a_order2.mdl file and subfolders for each of the filter listed in Table 2. Frequency of the PWM block in the .mdl file is a variable. The ripple amplitude of the filter output is measured using the minmax.m function. The ripple amplitudes measured for various f_{PWM} have been recorded in the respective excel sheets. The .txt files in the respective folders have the respective filter coeffifcients and instructions to follow before executing the .mdl file. The x_Order_RC_ykHz_BW.m file in the respective filter sub-folders plot the effective PWM DAC resolution vs. f_{PWM} numbers (in Figure 8 through Figure 13) recorded in the excel spreadsheet.

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