Migration from GL064N to GL064S

About this document

Scope and purpose

AN220470 describes the differences and potential issues when migrating from Cypress GL064N to the GL064S NOR flash. It discusses affected device features, timing parameters as well as packages.

Table of contents

1 Introduction

Cypress continues to extend the MirrorBit® GL family of 3-V NOR flash with the introduction of the GL064S parallel NOR family based on 65-nm process technology. Cypress developed the GL064S flash with migration in mind; most of the existing applications developed for GL064N flash can also use the GL064S flash. This document outlines the product differences that require attention when migrating from GL064N to GL064S flash.

Feature comparisons are shown is Section **2**. Feature differences are mentioned in Section **3**. Differences in Power-On-Reset (POR) timing are discussed in Section **4**. Differences in DC and AC specifications are detailed in Section **5**. Differences in footprint and packaging are discussed in Section **6**.

2 GL064N and GL064S Flash Feature Comparison

The 65-nm MirrorBit® GL064S flash provides significantly improved program and erase performance for 3-V parallel NOR applications, while maintaining basic hardware and software compatibility to allow use in existing designs that use GL064N. **Table 1** compares the features between GL064N and GL064S.

Table 1 GL064N and GL064S Feature Comparison

	GL064N	GL064S	Migration Issues
Process Node	110 nm	65 nm	No
Access Time	90 ns	70 ns	No
Temperature Range			
Industrial (−40 to +85°C)	√	√	No
Industrial Plus (−40 to +105°C)	x	√	No
Automotive, AEC-Q100 Grade 3 (−40 to +85°C)	x	√	No
Automotive, AEC-Q100 Grade 2 (−40 to +105°C)	x	√	No
Endurance			
100,000 Erase Cycles Typical Per Sector Minimum	√	√	No
Sector Architecture			
Uniform 64 KB	√	√	No
Hybrid one hundred twenty-seven 64-KB and eight 8-KB	√	√	No
Data Retention			
Twenty-year Data Retention Typical	√	√	No
Access			
Data Bus Width	x8/x16	x8/x16	No
Asynchronous	√	√	No
Read Page Mode	√	√	No
Read Page Size	16 bytes	16 bytes	No
Write Buffer Size	32 bytes	256 bytes	No
Security			
Individual Sector Write Protection	√	√	No
Secure Silicon OTP Area	256 bytes	256 bytes	No
Additional Features			
Status via Status Register	X	√	No
Evaluate Erase Status	X	√	No
Continuity Check	X	√	No
Automatic ECC	X	√	No
Packaging and Ordering Options			
48 -pin TSOP (TS048)	√	√	No
56-pinTSOP (TS056)	√	√	No
48-ball Fine-pitch BGA (VBK048, 8.15 mm x 6.15 mm)	√	√	No
64-Ball Fortified Ball Grid Array (LAA064, 13 mm x 11 mm)	√	√	No
64-Ball Fortified Ball Grid Array (LAE064, 9 mm x 9 mm)	√	√	No

3 Feature Difference Discussion

3.1 Write Buffer

The Write Buffer is designed to reduce the overall system programming time when programming the device. The host system issues a Write to Buffer command, fills the Write Buffer with data, and then issues the programming command. Depending on the device design, a Write Buffer can store up to a maximum Write Buffer size of data.

GL064N has a 32-byte (16 words) Write Buffer while GL064S has a 256-byte (128 words) Write Buffer. The Write Buffer in GL064S is eight times bigger than the one in GL064N. The larger Write Buffer facilitates higher programming throughput and better data alignment with most of the file systems. No software modifications are required to operate with a 32-byte maximum Write Buffer fill supported by GL064N flash in GL064S. Software can be modified to take advantage of the larger GL064S Write Buffer by querying the CFI Programming Buffer Size register at CFI word offset 2Ah and configuring the software to perform larger buffer fills.

3.2 Device ID

The GL064S flash has the same Device ID as the GL064N flash.

3.3 Status Register

The Status register contains the status and control bits that can be read or set by specific commands. The GL064S flash supports Status register reads as an alternative method to data polling determine the embedded operation status. The Status register feature is not supported on the GL064N flash.

The 16-bit Status register is accessed via a two-cycle operation consisting of a Read Status Register command write cycle followed immediately by a read cycle to the same targeted sector address. Utilization of the Status register is advantageous because unlike legacy data polling, the software does not need to track active address regions or compare sequential polling read values to determine the embedded algorithm status.

One Status register access provides all the information necessary to determine the flash state. A Clear Status Register command is available to reset the last completed embedded operation portion of the Status register. Status register usage is optional; existing designs using the GL064N flash do not have to accommodate this feature. If desired, software can be modified to take advantage of this feature. Similar to GL064N, GL064S also has the data polling option. Therefore, you have the option to choose the best method for your application to check the operation status.

For more details on Status register implementation and bit definition, see the **GL064S datasheet**.

3.4 Evaluate Erase Status

The Evaluate Erase Status (EES) command verifies that the last erase operation on the addressed sector was completed successfully. The EES command can be used to detect those erase operations that failed due to loss of power, reset, or failure during the erase operation.

The GL064S flash supports the Evaluate Erase Status feature that enables system software to minimize delay associated with erasures prior to code updates. Use of this feature is optional and is not supported in the GL064N flash. The addition of the Evaluate Erase Status feature is transparent to existing designs. See the **GL064S datasheet** for implementation details of this feature.

3.5 Continuity Check

The Continuity Check feature provides a basic test of connectivity from package connectors to each die pad. The GL064S flash supports the Continuity Check feature; using this feature is optional. The GL064N flash does not support Continuity Check. The addition of this feature is transparent to existing designs. See the GL064S datasheet for implementation details.

3.6 Automatic ECC

The GL064S flash supports the Automatic ECC feature that has internal hardware ECC with single-bit error correction. This feature can help improve user data integrity stored in flash. This feature is executed by flash internally and no change needs to be done when migrating from GL064N. This feature is transparent to the user.

See the GL064S datasheets for Automatic ECC feature details.

3.7 CFI Register

Table 2 provides a listing of all the Common Flash File (CFI) register values that are different for the GL064N and GL064S flash families. Software can access the CFI register to determine device-specific features such as array size, command set, page size, and programming time; and use these values to self-configure for optimal performance.

Table 2 CFI Register Differences

CFI Register	Word Offset	Byte Offset	GL064S	GL064N
Typical timeout per single write 2^N µs	1Fh	3Eh	0008h	0007h
Typical timeout for Min. size buffer write 2^N µs (00h = not supported)	20h	40h	0008h	0007h
Typical timeout per individual block erase 2^N ms	21h	42h	0009h	000Ah
Typical timeout for full chip erase 2^N ms (00h = not supported)	22h	44h	0010h	0000h
Max. timeout for buffer write 2^N times typical	24h	48h	0003h	0005h
Max. timeout per individual block erase 2^N times typical	25h	4Ah	0001h	0004h
Max. number of bytes in multi-byte write = 2^N (00h = not supported)	2Ah 2Bh	54h 56h	0008h 0000h	0005h 0000h

4 Power-On Reset (POR) and Warm Reset Timing

At power on, the flash requires more time in the reset state to self-configure than it does during a warm reset.

Table 3, **Figure 1**, and **Figure 2** detail the power-on reset and warm reset timing requirements for the GL064N and GL064S flash.

Table 3 Power On and Warm Reset Timing Requirements

Parameter	Description	Type	GL064N	GL064S
t_{VCS}	V_{CC} Setup Time to first access	min	50 µs	50 µs
t_{VIOS}	V_{IO} Setup Time to first access	min	N/A	50 µs
t_{RPH}	RESET# LOW to CE# LOW	min	N/A	50 µs
t_{RP}	RESET# LOW to RESET# HIGH	min	500 ns	200 ns
t_{RH}	RESET# HIGH to CE# LOW	min	50 ns	50 ns
t_{CEH}	CE# HIGH to CE# LOW	min	N/A	20 ns

Note:

1. *N/A = Not Applicable.*
2. *For GL064S, Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.*
3. *For GL064N, t_{RP} = 20 µs during embedded operation and t_{RP} = 500 ns.*

The durations to the first memory access after power-on, t_{VCS}, are identical in both GL064N and GL064S devices and should not present a migration challenge. However, the GL064S devices do require CE# to remain HIGH for at least t_{CEH} prior to CE# falling edge which initiates the first access. This t_{CEH} was not a requirement for GL064N devices.

The warm reset durations are different in GL064N and GL064S devices and can pose migration issues. GL064N devices need 550 ns (t_{RP} +t_{RH}) to complete a warm reset whereas GL064S devices require 50.2 µs (t_{RP} +t_{RH}) to complete the same warm reset. t_{CEH} is again a requirement for GL064S devices which was not needed for GL064N devices. In applications which may access the NOR Flash within 50.2 µs of a warm reset, some circuit modification will be required to accommodate migration to GL064S devices.

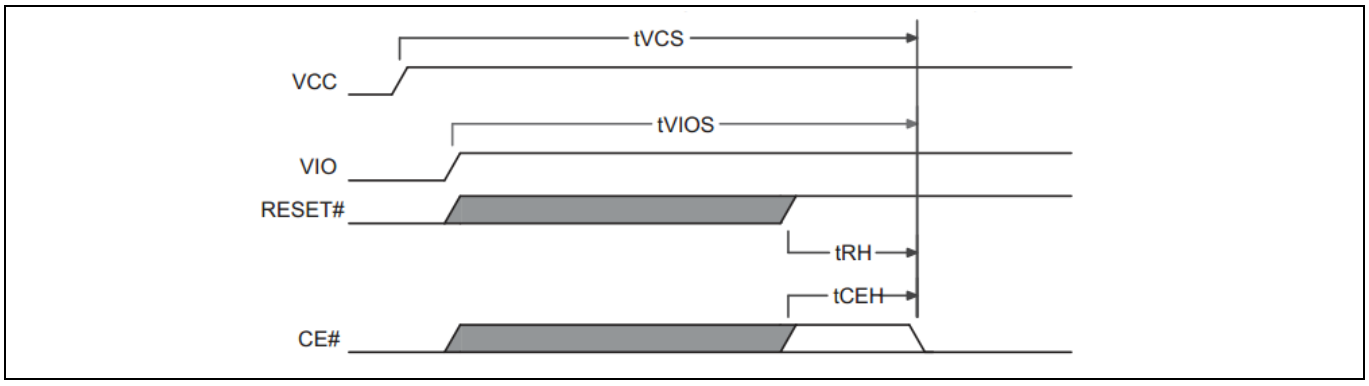

Figure 1 Power-Up Reset Timing

Power-On Reset (POR) and Warm Reset Timing

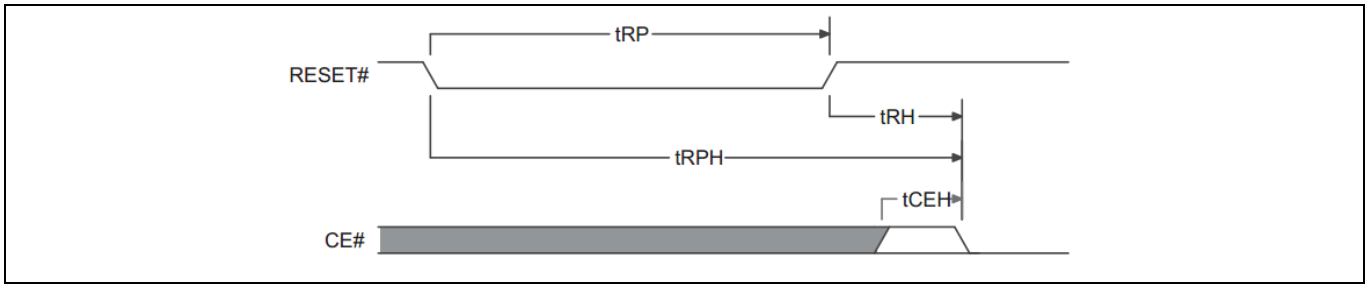

Figure 2 Warm Reset Timing

5 DC and AC Parameter Differences

The differences in DC parameters will not cause any issue during migration.

Table 4 DC Specification Differences

Parameter	Description	Type	GL064N	GL064S
Power Usage				
I_{CC2}	V_{CC} Intra-Page Read Current	Typ	5 mA	7.5 mA
I_{CC4}	V_{CC} Standby Current	Typ	1 µA	40 µA
		Max	5 µA	100 µA
I_{CC5}	V_{CC} Reset Current	Typ	1 µA	10 mA
		Max	5 µA	20 mA
I_{CC6}	Automatic Sleep Mode	Typ	1 µA	40 µA
		Max	5 µA	100 µA
Logic Levels				
V_{IL}	Input LOW Voltage	Min	-0.1	-0.5
V_{IH}	Input HIGH Voltage	Max	V_{IO} + 0.3	V_{IO} + 0.4

Table 5 provides side-by-side comparisons of AC parameter specification differences between the GL064S and the GL064N (less the reset timing parameter differences documented in **Table 3**). All parameters should be reviewed against actual application implementations to ensure a successful migration. For applications that utilize the erase suspend and/or program suspend features, it is important to review the system software ramifications of GL064S having a longer latency between issuance of the suspend and resume commands and the flash updating status and completing the transition between modes.

Note that all table specifications apply to the best speed option (90 ns for GL064N and 70 ns for GL064S), industrial temperature rated device with $V_{CC} = V_{IO} = 2.7–3.6$ V. See individual datasheets for performance specifications for other operating conditions.

Table 5 AC Specification Differences

Parameter	Description	Type	GL064N	GL064S
Async Read				
$t_{RC}/t_{ACC}/t_{CE}$	Read Cycle Time	Min	90 ns	70 ns
t_{PACC}	Page Access Time	Min	25 ns	15 ns
t_{DF}	Chip Enable to Output High-Z	Max	20 ns	15 ns
t_{DF}	Output Enable to Output High-Z	Max	20 ns	15 ns
Async Write				
t_{WC}	Write Cycle Time	Min	90 ns	60 ns
t_{DS}	Data Setup Time	Min	35 ns	30 ns
t_{WP}	Write Pulse Width	Min	35 ns	25 ns
t_{WPH}	Write Pulse Width HIGH	Min	30 ns	20 ns
t_{CP}	CE# Pulse Width	Min	35 ns	25 ns
t_{CPH}	CE# Pulse Width HIGH	Min	25 ns	20 ns

DC and AC Parameter Differences

Parameter	Description	Type	GL064N	GL064S
Suspend Resume				
t_{ESL}	Erase Suspend / Erase Resume	Max	N/A	30 µs
t_{PSL}	Program Suspend / Program Resume	Max	N/A	23.5 µs
t_{ERS}	Erase Resume to next Erase Suspend	Typ	N/A	100 µs
t_{PRS}	Program Resume to next Program Suspend	Typ	N/A	100 µs
Array Update				
	Sector Erase Time	Typ	500ms	235 ms
	Chip Erase Time	Typ	64 s	38.4 s
	Single Word Programming Time	Typ	60 µs	150 µs
	Total Write Buffer Program Time (1)	Typ	240 µs	400 µs
	Total Accelerated Effective Write Buffer Program Time (32 bytes)	Typ	200 µs	200 µs
	Chip Program Time for a full Write Buffer operation	Typ	63 s	13.11 s

Note:

1. *Maximum Write Buffer Size varies: GL064N = 32 bytes, GL064S = 256 bytes.*

6 Packaging

GL064S flash is available in two TSOP packages: 48-pin TSOP (TS048) and 56-pin TSOP (TS056), and three ball grid array packages: 48-ball fine pitch BGA (VBK048 8.15 mm × 1.0 mm), 64-ball fortified ball grid array (LAA064, 13 mm × 11 mm) and 64-ball fortified ball grid array (LAE064, 9 mm × 9 mm). GL064N is also available in two TSOP packages: 48-pin TSOP (TS048) and 56-pin TSOP (TS056) and three ball grid array packages: 48-ball fine pitch BGA (VBK048 8.15 mm × 1.0 mm), 64-ball fortified ball grid array (LAA064, 13 mm × 11 mm) and 64-ball fortified ball grid array (LAE064, 9 mm × 9 mm). The electrical contact dimensions and footprints are compatible with the GL064N flash.

7 References

[1] 3.0V GL-S Flash Memory, S29GL064S 64 Mbit Datasheet

[2] S29GL064N, S29GL032N 64 Mbit, 32 Mbit 3 V Page Mode MirrorBit Flash

Revision history

Document version	Date of release	Description of changes
**	2017-08-25	Initial release
*A	2021-01-18	Updated page access time in Table 5

Trademarks
All referenced product or service names and trademarks are the property of their respective owners.

Edition 2021-01-18
Published by
Infineon Technologies AG
81726 Munich, Germany

Do you have a question about this document?
Go to www.cypress.com/support

Document reference
002-20470 Rev. *A

IMPORTANT NOTICE
The information contained in this application note is given as a hint for the implementation of the product only and shall in no event be regarded as a description or warranty of a certain functionality, condition or quality of the product. Before implementation of the product, the recipient of this application note must verify any function and other technical information given herein in the real application. Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind (including without limitation warranties of non-infringement of intellectual property rights of any third party) with respect to any and all information given in this application note.

The data contained in this document is exclusively intended for technically trained staff. It is the responsibility of customer's technical departments to evaluate the suitability of the product for the intended application and the completeness of the product information given in this document with respect to such application.

For further information on the product, technology, delivery terms and conditions and prices please contact your nearest Infineon Technologies office (**www.infineon.com**).

WARNINGS
Due to technical requirements products may contain dangerous substances. For information on the types in question please contact your nearest Infineon Technologies office.

Except as otherwise explicitly approved by Infineon Technologies in a written document signed by authorized representatives of Infineon Technologies, Infineon Technologies' products may not be used in any applications where a failure of the product or any consequences of the use thereof can reasonably be expected to result in personal injury.