Best Practice for WRR Command for SPI Devices

AN200381 describes precautions that need to be considered to minimize the risk of corrupting the configuration and status registers caused by power loss or system reset after a command to modify the nonvolatile and OTP bits is issued (WRR command).

1 Introduction

Cypress SPI NOR Flash devices offer status registers (SR1 and SR2) and configuration registers (CR1) to query the status and control the features of the memory device and allowing user configuration. As described in the data sheet some of the bits can be modified, others are read-only. Furthermore, some of the bits are volatile, others are non-volatile; some bits can be programmed only once, others may be modified from a logical 0 to 1 and back.

This document describes precautions that need to be considered to minimize the risk of corrupting the configuration and status registers caused by power loss or system reset after a command to modify the non-volatile and OTP bits is issued (WRR command).

2 Write Registers (WRR) Command

As described in the data sheet, the WRR command is used to write and modify the contents of the status register (SR1) and configuration register (CR1) at the same time. Since these registers control the lock status of the memory device as well as the configuration of the I/O, it is crucial to maintain a stable operating condition while the command is executed. The internally timed program operation is running an algorithm to maintain a normal read window and stable data. A power loss event during this operation may corrupt the register settings. This can cause a locked or misconfigured device. Besides the described power event, a reset could cause the same issue. Once the device is locked or misconfigured the user application may not be able to recover.

3 Best Practice

Cypress recommends minimizing the number of program operations using the WRR command. It is common practice to set the flash configuration registers during production to a permanent state, which is unlikely to be modified during the product life cycle, in order to avoid additional use of the WRR command.

It is strongly recommended to maintain a stable power supply condition, e.g. don't connect or disconnect a large load to the power supply, after the WRR command is issued. The memory device should not undergo any Reset operations once the WRR command has been issued.

Document History Page

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**	–	–	01/29/2014	Initial version
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