Functional Description

7.1.2.1 GPMC Signals

Table 7-5 shows the use of address and data GPMC controller pins based on the type of external device.

Table 7-5. GPMC Pin Multiplexing Options

GPMC Signal	Non Multiplexed Address Data 16-Bit Device[1]	Non Multiplexed Address Data 8-Bit Device	Multiplexed Address Data 16-Bit Device[1]	16-Bit NAND Device	8-Bit NAND Device
GPMC_A[27]	A26	A27	A26	Not Used	Not Used
GPMC_A[26]	A25	A26	Not Used	Not Used	Not Used
GPMC_A[25]	A24	A25	Not Used	Not Used	Not Used
GPMC_A[24]	A23	A24	Not Used	Not Used	Not Used
GPMC_A[23]	A22	A23	Not Used	Not Used	Not Used
GPMC_A[22]	A21	A22	Not Used	Not Used	Not Used
GPMC_A[21]	A20	A21	Not Used	Not Used	Not Used
GPMC_A[20]	A19	A20	Not Used	Not Used	Not Used
GPMC_A[19]	A18	A19	Not Used	Not Used	Not Used
GPMC_A[18]	A17	A18	Not Used	Not Used	Not Used
GPMC_A[17]	A16	A17	Not Used	Not Used	Not Used
GPMC_A[16]	A15	A16	Not Used	Not Used	Not Used
GPMC_A[15]	A14	A15	Not Used	Not Used	Not Used
GPMC_A[14]	A13	A14	Not Used	Not Used	Not Used
GPMC_A[13]	A12	A13	Not Used	Not Used	Not Used
GPMC_A[12]	A11	A12	Not Used	Not Used	Not Used
GPMC_A[11]	A10	A11	Not Used	Not Used	Not Used
GPMC_A[10]	A9	A10	A25	Not Used	Not Used
GPMC_A[9]	A8	A9	A24	Not Used	Not Used
GPMC_A[8]	A7	A8	A23	Not Used	Not Used
GPMC_A[7]	A6	A7	A22	Not Used	Not Used
GPMC_A[6]	A5	A6	A21	Not Used	Not Used
GPMC_A[5]	A4	A5	A20	Not Used	Not Used
GPMC_A[4]	A3	A4	A19	Not Used	Not Used
GPMC_A[3]	A2	A3	A18	Not Used	Not Used
GPMC_A[2]	A1	A2	A17	Not Used	Not Used
GPMC_A[1]	A0	A1	A16	Not Used	Not Used
GPMC_A[0]	Not Used	A0	Not Used	Not Used	Not Used
GPMC_AD[15]	D15	Not Used	A/D[15]	D15	Not Used
GPMC_AD[14]	D14	Not Used	A/D[14]	D14	Not Used
GPMC_AD[13]	D13	Not Used	A/D[13]	D13	Not Used
GPMC_AD[12]	D12	Not Used	A/D[12]	D12	Not Used
GPMC_AD[11]	D11	Not Used	A/D[11]	D11	Not Used
GPMC_AD[10]	D10	Not Used	A/D[10]	D10	Not Used
GPMC_AD[9]	D9	Not Used	A/D[9]	D9	Not Used
GPMC_AD[8]	D8	Not Used	A/D[8]	D8	Not Used
GPMC_AD[7]	D7	D7	A/D[7]	D7	D7
GPMC_AD[6]	D6	D6	A/D[6]	D6	D6

(1) The values in this column represent the signals on the memory. Be aware that some 16-bit memories may label the address lines differently. Some label the LSB as A0, while others use A1 for the LSB. These columns assume the LSB is A0.

Table 7-5. GPMC Pin Multiplexing Options (continued)

GPMC Signal	Non Multiplexed Address Data 16-Bit Device[1]	Non Multiplexed Address Data 8-Bit Device	Multiplexed Address Data 16-Bit Device[1]	16-Bit NAND Device	8-Bit NAND Device
GPMC_AD[5]	D5	D5	A/D[5]	D5	D5
GPMC_AD[4]	D4	D4	A/D[4]	D4	D4
GPMC_AD[3]	D3	D3	A/D[3]	D3	D3
GPMC_AD[2]	D2	D2	A/D[2]	D2	D2
GPMC_AD[1]	D1	D1	A/D[1]	D1	D1
GPMC_AD[0]	D0	D0	A/D[0]	D0	D0
GPMC_CS[0]n	CS0n (Chip Select)	CS0n (Chip Select)	CS0n (Chip Select)	CE0n (Chip Enable)	CE0n (Chip Enable)
GPMC_CS[1]n	CS1n	CS1n	CS1n	CE1n	CE1n
GPMC_CS[2]n	CS2n	CS2n	CS2n	CE2n	CE2n
GPMC_CS[3]n	CS3n	CS3n	CS3n	CE3n	CE3n
GPMC_CS[4]n	CS4n	CS4n	CS4n	CE4n	CE4n
GPMC_CS[5]n	CS5n	CS5n	CS5n	CE5n	CE5n
GPMC_CS[6]n	CS6n	CS6n	CS6n	CE6n	CE6n
GPMC_ADVn_ALE	ADVn (Address Value)	ADVn (Address Value)	ADVn (Address Value)	ALE (address latch enable)	ALE (address latch enable)
GPMC_BE0n_CLE	BE0n (Byte Enable)	BE0n (Byte Enable)	BE0n (Byte Enable)	CLE (command latch enable)	CLE (command latch enable)
GPMC_BE1n	BE1n	BE1n	BE1n		
GPMC_CLK	CLK	CLK	CLK		
GPMC_OE_REn	OEn (Output Enable)	OEn (Output Enable)	OEn (Output Enable)	REn (read enable)	REn (read enable)
GPMC_WAIT0	WAIT0	WAIT0	WAIT0	R/B0n (ready/busy)	R/B0n (ready/busy)
GPMC_WAIT1	WAIT1	WAIT1	WAIT1	R/B1n (ready/busy)	R/B1n (ready/busy)
GPMC_WEn	WEn (Write Enable)	WEn (Write Enable)	WEn (Write Enable)	WEn (write enable)	WEn (write enable)
GPMC_WPn	WPn (Write Protect)	WPn (Write Protect)	WPn (Write Protect)	WPn (write protect)	WPn (write protect)

With all device types, the GPMC does not drive unnecessary address lines. They stay at their reset value of 00.

Address mapping supports address/data-multiplexed 16-bit wide devices:

- The NOR flash memory controller still supports non-multiplexed address and data memory devices.
- Multiplexing mode can be selected through the GPMC_CONFIG1_i[9-8] MUXADDDATA bit field.
- Asynchronous page mode is not supported for multiplexed address and data devices.

7.1.2.2 GPMC Modes

This section shows three GPMC external connections options:

- Figure 7-3 shows a connection between the GPMC and a 16-bit synchronous address/data-multiplexed (or AAD-multiplexed, but this protocol use less address pins) external memory device.
- Figure 7-4 shows a connection between the GPMC and a 16-bit synchronous nonmultiplexed external memory device .
- Figure 7-5 shows a connection between the GPMC and a 8-bit NAND device

Figure 7-3. GPMC to 16-Bit Address/Data-Multiplexed Memory