# Migration from AM29LV-D to S29GL-N (64 Mb)

***Application Note***

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## 1. Abstract

The 64 Mb devices in the Am29LV-D family of 230 nm floating gate devices can migrate to the second generation S29GL064N 110 nm MirrorBit® technology products. The second generation 110 nm technology products will be offered with full voltage range (2.7V - 3.6V), replacing the regulated voltage range of the Am29LV-D (3.0V - 3.6V). The S29GL064N series flash has ASP (Advanced Security Protection) security features for safeguarding code, which replaces the traditional hardware sector group protection feature that requires a $V_{ID}$ voltage on the RESET# pin.

## 2. Feature Comparison Summary of Am29LV640/641/065D and S29GL064N

**Table 2.1** Feature Comparison

| Feature | Am29LV640D, Am29LV641D | Am29LV065D | S29GL064N |
|---|---|---|---|
| Technology | 230 nm floating gate process | 230 nm floating gate process | 110 nm MirrorBit process |
| Sector Architecture | Uniform 64-kbyte sectors | Uniform 64-kbyte sectors | 8 boot sectors (8 kbytes each) Remaining sectors are 64 kbytes each, or uniform 64-kbyte sectors |
| Bus Architecture | x16 data bus (Am29LV640D/Am29LV641D) | x8 data bus (Am29LV065D) | X8/x16 data bus |
| Read Page Buffer | N/A | N/A | 16 bytes (8 words) |
| Write Buffer | N/A | N/A | 32 bytes (16 words) |
| WP#/ACC | Separate pins on TSOP and SSOP Packages<br>WP# not available on BGA Package | ACC only supported | Accelerated programming/hardware protect first or last sector |
| Pinout | Common footprint | Common footprint | Common footprint |
| Device ID | D7h | 93h | 7E0C01h, 7E1000h, 7E1001h, 7E1301h |
| Secured Silicon Region | 256-byte OTP sector | 256-byte OTP sector | 256-byte OTP sector |
| Data Polling | Standard Data polling | Standard Data polling | Standard Data polling |
| Sector Protection and Unprotection | $V_{ID}$ voltage (+12V) required on RESET# | $V_{ID}$ voltage (+12V) required on RESET# | Advanced Sector Protection (ASP) mode under normal $V_{CC}$ voltage. Also offers Persistent Sector Protection and password sector protection mode. |
| Temporary protection | $V_{ID}$ voltage required on RESET# | $V_{ID}$ voltage required on RESET# | Dynamic Protection mode |
| Package | TS048, SSO056, LAA065, FBE064 | TS048, FBE063 | TS048, TS056, VBK048 (ball footprint is the same as FBE063), LAA064 |

**Table 2.2** DC Parameter Differences

| Parameter | Description | Am29LV640D/ Am29LV641D | Am29LV065D | S29GL064N |
|---|---|---|---|---|
| $V_{CC}$ | Core Voltage | 3.0 - 3.6V | 3.0 - 3.6V | 2.7 - 3.6V |
| $V_{IO}$ | I/O Voltage | 1.8 - 2.9V or 3.0 - 5.0V | 1.8 - 2.9V or 3.0 - 5.0V | 1.65 - 1.95V or 2.7 - 3.6V |
| ILI (WP#/ACC only) | Input Load Current | ± 5 µA (WP#) ± 1 µA (ACC) | ± 1 µA (ACC) | ± 2 µA |
| $I_{CC1}$ (1 MHz) | $V_{CC}$ Initial Read Current | 2 / 4 mA (typ/max) | 2 / 4 mA (typ/max) | 6 / 10 mA (typ/max) |
| $I_{CC1}$ (5 MHz) | $V_{CC}$ Initial Read Current | 9 / 16 mA (typ/max) | 9 / 16 mA (typ/max) | 25 / 30 mA (typ/max) |
| $I_{CC2}$ (Am29LV-D) $I_{CC3}$ (S29GL064N) | Vcc Active Erase / Program Current | 26/30 mA (typ/max) | 26/30 mA (typ/max) | 50/60 mA (typ/max) |
| $I_{CC3}$ (Am29LV-D) $I_{CC4}$ (S29GL064N) | $V_{CC}$ Standby Current | 0.2 / 5 µA (typ/max) | 0.2 / 5 µA (typ/max) | 1 / 5 µA (typ/max) |
| $I_{CC4}$ (Am29LV-D) $I_{CC5}$ (S29GL064N) | $V_{CC}$ Reset Current | 0.2 µA (typ) | 0.2 µA (typ) | 5 µA (typ) |
| $I_{CC5}$ (Am29LV-D) $I_{CC6}$ (S29GL064N) | Automatic Sleep Mode | 0.2 µA (typ) | 0.2 µA (typ) | 1 µA (typ) |
| $I_{ACC}$ (ACC, Am29LV64xD) $I_{ACC}$ (WP#/ACC, S29GL064N) | ACC Accelerated Program Current | 5 / 10 mA | N/A | 10 / 20 mA |
| $V_{IL}$ ($V_{IO}$ = $V_{CC}$) | Input Low Voltage | -0.5 / 0.8 (min/max) | -0.5 / 0.8 (min/max) | -0.1 / 1.08V (min/max) |
| $V_{IH}$ ($V_{IO}$ = $V_{CC}$) | Input High Voltage | 1.89 / 3.9V (min/max) | 1.89 / 3.9V (min/max) | 1.89 / 3.9V (min/max) |
| $V_{ID}$ ($V_{IO}$ = $V_{CC}$) | Voltage for Autoselect | 8.5V (min) | 8.5 V (min) | 11.5 V (min) |
| $V_{OL}$ ($V_{IO}$ = $V_{CC}$) | Output Low Voltage | 0.45V (max) | 0.45V (max) | 0.54V (max) |
| $V_{OH2}$ ($V_{IO}$ = $V_{CC}$) | Output High Voltage $I_{OL}$ = -100 µA | 2.30V (min) | 2.30V (min) | 2.295V (min) |

**Figure 2.1** Speed Grade Migration Key

| From | To |
|---|---|
| Am29LVxxxD | S29GL064N |
| 90 ns | 90 ns |
| 100 ns | 90 ns |
| 120 ns | 110 ns |

**Table 2.3** AC Parameter Differences (Sheet 1 of 2)

| Parameter | Description | Am29LV640D/ Am29LV641D | Am29LV065D | S29GL064N |
|---|---|---|---|---|
| **Read Only Operations** | | | | |
| | Speed Options | 90 / 120 ns | 90 / 100 / 120 ns | 90 / 110 ns |
| $T_{RC}$ | Read Cycle Time | 90 / 120 ns (min) | 90 / 100 / 120 ns (min) | 90 / 110 ns (min) |
| $T_{ACC}$ | Address to Output Delay | 90 / 120 ns (max) | 90 / 100 / 120 ns (max) | 90 / 110 ns (max) |
| $T_{CE}$ | Chip Enable to Output Delay | 90 / 120 ns (max) | 90 / 100 / 120 ns (max) | 90 / 110 ns (max) |
| $T_{PACC}$ ($V_{IO}$ = $V_{CC}$) | Page Access Time | N/A | N/A | 25 ns (max) |
| $T_{OE}$ ($V_{IO}$ = $V_{CC}$) | Output Enable to Output Delay | 35 / 50 ns (max) | 35 / 35 / 50 ns (max) | 25 / 25 ns (max) |
| $T_{DF}$ | Chip Enable to Output High-Z | 30 ns (max) | 30 ns (max) | 20 ns (max) |
| $T_{DF}$ | Output Enable to Output High-Z | 30 ns (max) | 30 ns (max) | 20 ns (max) |
| **Erase and Program Operations** | | | | |
| | Speed Options | 90 / 120 ns | 90 / 100 / 120 ns | 90 / 110 ns |
| $T_{WC}$ | Write Cycle Time | 90 / 120 ns (min) | 90 / 100 / 120 ns (min) | 90 / 110 ns (min) |

**Table 2.3** AC Parameter Differences (Sheet 2 of 2)

| Parameter | Description | Am29LV640D/ Am29LV641D | Am29LV065D | S29GL064N |
|---|---|---|---|---|
| $T_{AH}$ | Address Hold Time | 45 / 50 ns (min) | 45 / 45 / 50 ns (min) | 45 ns (min) |
| $T_{DS}$ | Data Setup Time | 45 / 50 ns (min) | 45 / 45 / 50 ns (min) | 35 ns (min) |
| $T_{CEPH}$ | CE# High during toggle bit polling | N/A | N/A | 20 ns (min) |
| $T_{WP}$ | Write Pulse Width | 35 / 50 ns (min) | 35 / 35 / 50 ns (min) | 35 ns (min) |
| $T_{WHWH1}$ | Write Buffer Program Operation | N/A | N/A | 240 µs (typ) |
| $T_{WHWH1}$ | Single Word Program Operation | 11 µs (typ) | N/A | 60 µs (typ) |
| $T_{WHWH1}$ | Single Byte Program Operation | N/A | 5 µs (typ) | N/A |
| $T_{WHWH1}$ | Accelerated Single Word Program Operation | 7 µs (typ) | N/A | 54 µs (typ) |
| $T_{WHWH2}$ | Sector Erase Operation | 0.9 s (typ) | 0.9 s (typ) | 0.5 s (typ) |
| $T_{BUSY}$ | WE# High to RY/BY# Low | 90 ns (min) | 90 / 90 / 90 ns (min) | 90 / 110 ns (min) |
| **Alternate CE# Controlled Erase and Program Operations** | | | | |
| | Speed Options | 90 / 120 ns | 90 / 100 / 120 ns | 90 / 110 ns |
| $T_{WC}$ | Write Cycle Time | 90 / 120 ns (min) | 90 / 100 / 120 ns (min) | 90 / 110 ns (min) |
| $T_{AH}$ | Address Hold Time | 45 / 50 ns (min) | 45 / 45 / 50 ns (min) | 45 ns (min) |
| $T_{DS}$ | Data Setup Time | 45 / 50 ns (min) | 45 / 45 / 50 ns (min) | 35 ns (min) |
| $T_{CP}$ | CE# Pulse Width | 45 / 50 ns (min) | 45 / 45 / 50 ns (min) | 35 ns (min) |
| $T_{CPH}$ | CE# Pulse Width High | 30 ns (min) | 30 ns (min) | 25 ns (min) |
| $T_{WHWH1}$ | Write Buffer Program Operation | N/A | N/A | 240 µs (typ) |
| $T_{WHWH1}$ | Single Word Program Operation | 11 µs (typ) | N/A | 60 µs (typ) |
| $T_{WHWH1}$ | Single Byte Program Operation | N/A | 11 µs (typ) | N/A |
| $T_{WHWH1}$ | Accelerated Single Word Program Operation | 7 µs (typ) | N/A | 54 µs (typ) |
| $T_{WHWH2}$ | Sector Erase Operation | 0.9 s (typ) | 0.9 s (typ) | 0.5 s (typ) |
| $T_{RH}$ | RESET# High Time Before Write | N/A | N/A | 50 ns (min) |
| **Erase and Programming Performance** | | | | |
| | Sector Erase Time | 0.9 / 15 s (typ/max) | 0.9 / 15 s (typ/max) | 0.5 / 3.5 s (typ/max) |
| | Chip Erase Time | 115 s (typ) | 115 s (typ) | 64 / 128 s (typ/max) |
| | Word Program Time | 11 / 300 µs (typ/max) | N/A | N/A |
| | Accelerated Word Program Time | 7 / 210 µs (typ/max) | N/A | N/A |
| | Byte Program Time | N/A | 5 / 150 µs (typ/max) | N/A |
| | Accelerated Byte Program Time | N/A | 4 / 120 µs (typ/max) | N/A |
| | Total Write Buffer Program Time | N/A | N/A | 240 µs (typ) |
| | Total Accelerated Effective Write Buffer Program Time | N/A | N/A | 200 µs (typ) |
| | Chip Program Time | 48 / 144 s (typ/max) | 42 / 126 s (typ/max) | 63 s (typ) |
| | Typical Program and Erase Times assume 25°C, 3.0V $V_{CC}$ and: | 1,000,000 cycles | 1,000,000 cycles | 10,000 cycles |

# 3. Discussion of Differences

## 3.1 Bus Architecture

The Am29LV64xD has a x16 data bus width as the Am29LV065D has a x8 data bus width. The S29GL064N supports both configurations via the selectable BYTE# pin. Pulling the BYTE# pin to logic level '0' configures the S29GL064N into the x8 data bus width while pulling the BYTE# pin to logic level '1' or allowing it to float (no connection) configures the S29GL064N into the x16 data bus width.

Migration from either the Am29LV64xD or the Am29LV065D to the S29GL064N is supported by selecting the correct data bus width configuration via the BYTE# pin. The option exists when migrating from the Am29LV065D to the S29GL064N to double the data bus width by adding an upper byte of data signals and configuring the device properly by pulling the BYTE# pin to a logical high.

## 3.2 Read Page Buffer

The Am29LV64xD and the Am29LV065D devices do not feature a read page buffer. All read accesses are random accesses. As such, the timing for all read accesses will be characterized via the $T_{ACC}$ specification.

The S29GL064N has a 16 byte (8 word) read page buffer, which improves effective read bandwidth. Upon an initial random access into the memory array, data is provided onto the data bus pins in $T_{ACC}$ time (ex. 120 ns). In parallel to this request, the S29GL064N will also pre-fetch the next 15 bytes (7 words) and store them in the read page buffer. Subsequent read accesses into the flash array with addresses within the buffer depth away from the initial random access address will have the appropriate data provided within the $T_{PACC}$ (25 ns) specification.

With respect to the read page buffer, drop-in compatibility is met without software changes when migrating from the Am29LV64xD and the Am29LV065D to the S29GL064N. Although the S29GL064N will cache the look-ahead data automatically, the flash interface will be expecting the data within the $T_{ACC}$ time (ex. 120 ns) while the data will actually be presented with the $T_{PACC}$ (25 ns) time. Software changes for a processor with page mode support, essentially a processor with a Memory Management Unit (MMU) with variable wait states, can enable significantly improved read bandwidths.

## 3.3 ACC

The programming accelerate function is enabled via the ACC pin on the Am29LV64xD devices, the Am29LV065D device and the S29GL064N devices. It exists individually as the ACC input signal on the Am29LV64xD devices and the Am29LV065D device while implemented along with the write protect function (WP#) on the S29GL064N as the WP#/ACC input signal. When ACC = $V_{ID}$, programming function completes approximately 10% faster.

## 3.4 Device ID

Device IDs are different across the Am29LV64xD devices, the Am29LV065D devices and the S29GL064N devices. Note that all MirrorBit devices, including the S29GL064N, use a three-byte Device ID. See the Spansion Application Note titled Migrating from Single-byte to Three-byte Device IDs available on the Spansion website for further details. The device IDs are shown in Table 2.1, *Feature Comparison* on page 1.

If driver software reads the Device IDs upon power-up, migration to the S29GL064N from either the Am29LV64xD or the Am29LV065D may require software modifications.

## 3.5 Am29LV64xD and Am29LV065D: 12V Sector Group Protection

### 3.5.1 WP#

The WP# input pin is used for Hardware Write Protection. WP# can protect the Highest address sector or Lowest address sector for Uniform Sector Flash when WP#=$V_{IL}$. For Boot Sector Flash products, it provides the top or bottom two address sectors protection when WP#=$V_{IL}$. The Sectors can be unprotected by turning the WP# back to Logic High ($V_{IH}$). The WP# signal can be controlled by a GPIO (General Purpose Input/ Output) signal from the host processor if needed.

This kind of protection can only provide 64-kbyte (uniform sector) or 2x8-kbyte (boot sector) protection. Other areas of the Flash need to be protected. You must use the other type of protection: Sector Group Protection.

WP# is not available on the BGA package of the Am29LV64xD devices or on the Am29LV065D device.

### 3.5.2 Sector Group Protection

The hardware sector group protection feature disables both program and erase operations in any sector group, and the unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection requires $V_{ID}$ on the RESET# pin before the protection/unprotection algorithms can be started. Sector group protection can be implemented either in system or by using stand-alone programming equipment.

The Flash devices are shipped with all sector groups unprotected. Spansion offers the option of programming and protecting sector groups at its factory prior to shipping the device through Spansion Programming Services.

Figure 3.1 and Figure 3.2 are the RESET# hardware circuitry that can be used to control the 12V ($V_{ID}$) voltage that is required for the protection and unprotection operation. For details please refer to the Reset Pin Circuitry for Flash Memory Sector Protection Management Application Note.

**Figure 3.1** RESET# Pin Isolation Circuitry

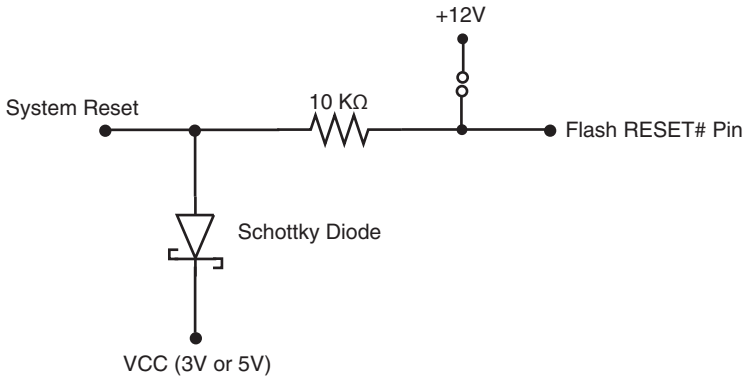
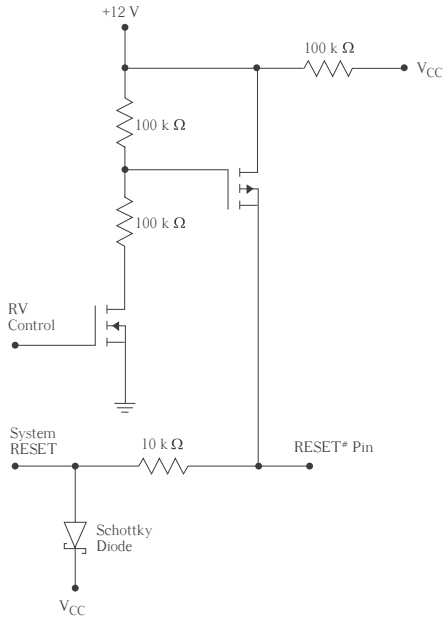



**Figure 3.2** $V_{ID}$ Routing Circuitry



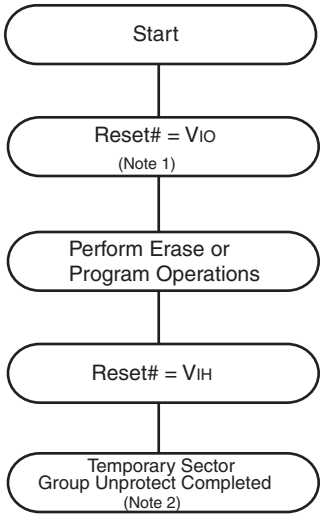
### 3.5.3 Unprotection

The sector group unprotection is a reversed operation, which also needs a 12V $V_{ID}$ on RESET# pin before the flow. For details please refer to the data sheet.

### 3.5.4 Temporary Sector Group Unprotect

This feature allows temporary unprotection of previously protected sector groups to change the data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to $V_{ID}$. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once $V_{ID}$ is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 3.3 shows the algorithm.

**Figure 3.3** Temporary Sector Group Unprotect Operation




***Notes:***

1. *All protected sector groups unprotected (If WP# = $V_{IL}$, the highest or lowest address sector remains protected for uniform sector devices; the top or bottom two address sectors remains protected for boot sector devices).*
2. *All previously protected sector groups are protected once again.*

## 3.6 S29GL064N: Advanced Sector Protection

The new migrated S29GL064N products keep the same WP#/ACC protection function, but they remove the 12V sector groups protection and unprotection mode, which has been replaced by Spansion Advanced Sector Protection (ASP). The Advanced Sector Protection features several levels of sector protection, which can disable both the program and erase operations in sectors.

### 3.6.1 Dynamic/Persistent Sector Protection

Dynamic/Persistent Sector Protection are the most commonly used types of Advanced Sector Protection. They offer security through the following three features:

- Dynamic Protection Bits (DYB bits)
- Persistent Protection Bits (PPB bits)
- Secure Silicon Sector (SecSi Sector)

This mode gives users the flexibility to protect their code with both volatile DYB bits and non-volatile PPB bits that prohibit program and erase options on selected sectors. With the exception of the Secured Silicon Sector, each sector or sector group protection status is defined by the logic or the corresponding DYB bit and PPB bit. Non-volatile PPB bits can be modified only when the global volatile PPB lock bit is unlocked. This mode can be used in applications that need in-system security against viruses and other threats without different user's privilege. By default no sectors are protected when devices are shipped from Spansion.

### 3.6.2 Dynamic Protection Bits

Dynamic Protection Bits (DYB) are volatile protection bits that, when locked, prevent sectors from being programmed or erased. Since DYB are volatile bits, their states are lost whenever power is removed. There is one DYB assigned for every sector or sector group, depending on the product. Dynamic Protection Bits allows software to easily protect against inadvertent changes, yet does not prevent the easy removal of protection when changes are needed.

#### Using Dynamic Protection Bits

The user can program a DYB to “Lock” state, which protects that sector against program or erase commands. The user can also erase individual DYBs to set them to “Unlock,” which allows the sector to be programmed or erased. The status of the individual DYBs can be read using the Read command.

#### Dynamic Protection Lock Bit

Along with the Dynamic Protection Bits there is a Dynamic Protection Lock Bit (DYB Lock Bit). The DYB Lock Bit defines the state of all the DYBs after a power cycle. If the DYB Lock Bit is set to “Unlock” then all the DYBs are set to “Unlock” after a power cycle. If the DYB Lock Bit is set to “Lock” then all the DYBs are set to “Lock” after a power cycle.

**Note:** For the details of the ASP operation, please refer to the Spansion standard data sheet.

## 3.7 Password Sector Protection

Password Sector Protection offers a higher level of security than the Persistent Sector protection, as it requires the user to enter a valid 64-bit password to unlock the PPB lock bit before modifying Persistent Protection. It includes all of the features listed below:

- Password
- Dynamic Protection Bits (DYB bits)
- Persistent Protection Bits (PPB bits)
- Secure Silicon Sector

This security mode is typically used in applications where a service provider wants to be able to protect their code from being altered by other users who don't have the password. The password is stored in a one-time programmable (OTP) region outside of the Flash memory. Once the Password Protection Mode Lock Bit is set, the password is permanently set with no means to read, program, or erase it.

To increase the protection provided by the 64-bit password there is a built-in 2 µs delay for each password check after the valid 64-bit password is entered for the PPB Lock Bit to be cleared to the “unfreezed state”. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password. Testing all the possible password combinations would take 1,169,109 years.

## 3.8 DC and AC Parameter Differences

### 3.8.1 $V_{CC}$ Range

The S29GL064N supports a standard $V_{CC}$ voltage range of 2.7V - 3.6V, which is wider than the regulated $V_{CC}$ voltage range of 3.0V - 3.6V supported by the Am29LV-D devices. No circuit modifications are required to operate the S29GL064N with $V_{CC}$ in the 3.0V - 3.6V range supported by the Am29LV-D devices.

### 3.8.2 $V_{IO}$ Range

The S29GL064N supports $V_{IO} = V_{CC}$ voltage connections, identical to the Am29LV-D devices. No circuit modifications are required to operate the S29GL064N with $V_{IO} = V_{CC}$ in the 3.0V - 3.6V range supported by the Am29LV-D devices.

Additionally, the S29GL064N is available with support for $V_{IO}$ = 1.65V - 3.6V. The supported $V_{IO}$ voltage range is signified by the first character in the ordering part number model number: “V” signifies $V_{IO}$ = 1.65V - 3.6V and $V_{CC}$ = 2.7V - 3.6V (e.g., S29GL-N), “0” signifies $V_{IO} = V_{CC}$ = 2.7V - 3.6V (e.g., S29GL-N).

With the Am29LV-D devices, supported $V_{IO}$ voltage range is defined by the last character in the ordering part number speed option: “0” signifies $V_{IO}$ = 3.0V - 5.0V and $V_{CC}$ = 3.0V - 3.6V, “1” signifies $V_{IO}$ = 1.8V - 2.9V and $V_{CC}$ = 3.0V - 3.6V.

### 3.8.3 Leakage Currents

Minor differences in leakage currents between the S29GL064N and Am29LV-D devices will not require circuit modifications to accommodate.

### 3.8.4 Active $I_{CC}$ Read Currents

Active read current specification differences between the S29GL-N and Am29LV-D devices will not require circuit modifications to accommodate. The system power regulation circuitry providing power to the flash should be designed to accommodate the maximum flash $I_{CC}$ load which of 60 mA during programming and erase operations on the S29GL-N as this load exceeds all read operation loads.

### 3.8.5 Accelerated Program Current

Accelerated program current specification differences between the S29GL-N and Am29LV-D devices will not require circuit modifications to accommodate. The power regulation circuitry providing power to the flash ACC pin should be designed to accommodate the maximum flash IACC load which is 20 mA during the accelerated programming operations on the S29GL-N.

### 3.8.6 Signal Voltages

Two voltage specification differences should be considered when migrating from the Am29LV-D devices to the S29GL064N: $V_{IL}$ min and $V_{ID}$ min. When $V_{IO} = V_{CC}$, $V_{IL}$ min for the Am29LV-D devices is -0.5V while the $V_{IL}$ min for the S29GL064N device is -0.1V. Hence input low voltages, including undershoot, should not be below -0.1V on applications using the S29GL064N.

In addition, the minimum $V_{ID}$ – the high voltage required to perform a few commands in the High Voltage Method of the Autoselect mode - is 11.5V for the S29GL064N as compared to 8.5V for the Am29LV-D devices. Thus, when migrating from the Am29LV-D devices to the S29GL064N device, please ensure that the source for $V_{ID}$ voltage provides a minimum of 11.5V.

### 3.8.7 Speed Grades

The S29GL064N is available in 90 ns and 110 ns speed grades only and is not available in the 100 ns or 120 ns speed grade that were additional options for the Am29LV-D devices. Applications that required 90 ns or 100 ns speed grade versions of the Am29LV-D devices should use the 90 ns speed grade version of the S29GL064N. In addition applications that used the 120 ns speed grade versions of the Am29LV-D devices should use the 110 ns version of the S29GL064N. Except for feature and parameter difference specifically noted in this document, there are no issues with using the 90 ns speed grade version of the S29GL064N in an application that can accommodate the 100 ns speed grade of the Am29LV-D devices or with using the 110 ns speed grade version of the S29GL064N in an application that can accommodate the 120 ns speed grade of the Am29LV-D devices.

### 3.8.8 Read Cycle Time (TRC)

The S29GL064N supports minimum 110 ns read cycle times for the 110 ns speed grade device. If the speed grade migration recommendation (key above) is followed, minimum read cycle time of the S29GL064N will either match that or be less than that of the Am29LV-D device. This guarantees the read cycle time requirement will be met when moving to the faster S29GL064N device.

### 3.8.9 Address to Output Delay ($T_{ACC}$), Chip Enable to Output Delay ($T_{CE}$), Output Enable to Output Delay ($T_{OE}$), Chip Enable to Output High-Z ($T_{DF}$), Output Enable to Output High-Z ($T_{DF}$)

When following the speed grade migration recommendation, the specs (listed above) of the new device are either equal to or less than that of the original device. Since the maximum time for the above specs are met

by the Am29LV-D device within the application, proper operation after migration to the S29GL064N device requires that the S29GL064N specs should be equal to or less than that of the Am29LV-D devices. A review of the above specs shows that the S29GL064N device has lower maximum specs than that of the Am29LV-D devices. Therefore proper timing during read only operations after migration will be met. No modifications are necessary when migrating to the S29GL064N.

### 3.8.10 Intra-Page Access Time ($T_{PACC}$)

The S29GL064N supports maximum 25 ns intra-page read accesses of for all speed grades of the device. The Am29LV-D devices do not support page mode operation. This spec is a measure of how quickly the S29GL064N provides valid data after the address – within the buffer range – is changed. If the access address is outside of the range of the buffer depth, then valid data will be provide at $T_{ACC}$ (90 or 110 ns depending on the selected speed option). To be utilized, page mode must be supported by the microcontroller - one whose Memory Management Unit (MMU) can support variable wait states and the appropriate software must be written and executed. $T_{PACC}$ is required to be met after migration to the S29GL064N device only if the software is modified to utilize the read page buffers.

### 3.8.11 Write Cycle Time ($T_{WC}$), Address Hold Time ($T_{AH}$), Data Setup Time ($T_{DS}$), Write Pulse Width ($T_{WP}$)

When following the speed grade migration recommendation, the specs (listed above) of the new device are either equal to or less than that of the original device. Since the maximum time for the above specs are met by the Am29LV-D device within the application, proper operation after migration to the S29GL064N device requires that the S29GL064N specs should be equal to or less than that of the Am29LV-D devices. A review of the above specs shows that the S29GL064N device has lower maximum specs than that of the Am29LV-D devices. Therefore proper timing during read only operations after migration will be met. No modifications are necessary when migrating to the S29GL064N.

### 3.8.12 CE# High during Toggle Bit Polling ($T_{CEPH}$)

This specifies the minimum time CE# signal is inactive between active periods. It is held to 20 ns minimum. The Am29LV-D devices do not support this specification. It is required to be met after migration to the S29GL064N device when the processor is polling the DQ bits for embedded command completion status.

### 3.8.13 Write Buffer Program Operation ($T_{WHWH1}$)

Write Buffer Programming methodology is supported with the S29GL064N and is the recommended programming method. Write Buffer Programming is not supported in the Am29LV-D devices. $T_{WHWH1}$ specifies the typical amount of time to complete the write buffer program operation. For the S29GL064N, $T_{WHWH1}$ is 240 µs (typ). No hardware changes are necessary to support write buffer programming once migration to the S29GL064N has occurred. Appropriate software will need to be written to employ the write buffer programming methodology with the S29GL064N.

### 3.8.14 Single Word Program Operation ($T_{WHWH1}$)

Single Word Programming is supported with the Am29LV64xD devices and with the S29GL064N. With the Am29LV-D devices $T_{WHWH1}$ is 11 µs (typ); with the S29GL064N TWHWH1 is 60 µs. If the application uses either DQ Polling or the RY/BY# signal to denote the completion of an embedded operation, no changes are necessary when migrating to the S29GL064N. However, if the application uses a timeout to denote the embedded operation complete, the timeout value for single word programming would need to be increased beyond 60 µs.

### 3.8.15 Single Byte Program Operation ($T_{WHWH1}$)

Single Byte Programming is only supported with the Am29LV065D device and not with the S29GL064N. When migrating from the Am29LV065D to the S29GL064N, software modifications are required to employ either the write buffer methodology or the single word programming methodology. In addition, from a hardware standpoint, the upper byte of data will need to be added to the design.

### 3.8.16 Accelerated Single Word Program Operation ($T_{WHWH1}$)

Accelerated Single Word Programming is supported with the Am29LV64xD devices and with the S29GL064N and provides an approximate 10% improvement in programming time. The specification $T_{WHWH1}$ is 7 µs (typ) with the Am29GL64xD devices and is 54 µs with the S29GL064N. If the application uses either DQ Polling or the RY/BY# signal to denote the completion of an embedded operation, no changes are necessary when migrating to the S29GL064N. However, if the application uses a timeout to denote the embedded operation complete, the timeout value for single word programming would need to be increased beyond 54 µs.

### 3.8.17 Sector Erase Operation ($T_{WHWH2}$)

Sector Erase in the Am29LV-D devices completes in 0.9 s (typ) while sector erase in the S29GL064N competes in 0.5 s (typ). No hardware changes are required to support the migration to the S29GL064N. If the software uses RY/BY# signal or DQ Polling, nothing is required to change and the software will run with highest performance. If the software employs the use of time-outs with respect to sector erase operations, nothing is required to be modified. However, for highest possible performance, the timeout values should be reduced downward to the 0.5 s per sector rate.

### 3.8.18 WE# High to RY/BY# Low ($T_{BUSY}$)

$T_{BUSY}$ is specified at 90 ns minimum in the Am29LV-D devices and 90 ns in the 90 ns speed grade of the S29GL064N and 110 ns in the 110 ns speed grade of the S29GL064N. If one is migrating to the 90 ns speed grade of the S29GL064N nothing needs to be done. However, if one is migrating to the 110 ns speed grade of the S29GL064N, some software modification may be required. If DQ Polling or RY/BY# methods are employed in software, nothing will be required. However if time-outs are used, then an update to the timeout value may be warranted to support the increase in the RY/BY fall of 20 ns.

### 3.8.19 CE# Pulse Width ($T_{CP}$)

When migrating to the S29GL064N from the Am29LV-D devices, $T_{CP}$ specification is reduced from either 45 or 50 ns minimum to 35 ns minimum. No hardware changes are necessary. This reduction in the CE# pulse width allows for faster operation of the interface when a microcontroller can support it. Software changes may be needed to optimize the interface.

### 3.8.20 CE# Pulse Width High ($T_{CPH}$)

When migrating to the S29GL064N from the Am29LV-D devices, $T_{CP}$ specification is reduced from 30 ns minimum to 25 ns minimum. No hardware changes are necessary. This reduction in the CE# pulse width High allows for faster operation of the interface when a microcontroller can support it. Software changes may be needed to optimize the interface.

### 3.8.21 RESET# High Time Before Write ($T_{RH}$)

When migrating to the S29GL064N, $T_{RH}$ will need to be considered. It is defined as the minimum time after RESET# signal deactivates before WE# activates and is specified at 50 ns minimum. Please ensure that a valid write doesn't occur within 50 ns after a reset condition. This specification does not exist with the Am29LV-D devices.

## 4. Package Migrations

When migrating from the Am29LV-D devices to the S29GL064N, some packages will transition without layout considerations, i.e. they will be identical. These include device migrations from packages TSO48 and LAA064.

The SSO056, 56-pin Small will not be available in the S29GL064N. Thus migrations from the Am29LV64xD devices in the SSO056 package will require a selection of a new package and a relay out of the printed circuit board.

Migration from the FBE063 package requires a move to the VBK048 package with the removal of outrigger balls accounting for the ball count reduction. See Figure 4.2 for further details.

**Table 4.1** Am29LV-D to S29GL064N Package Migration

| From Am29LV64xD | To S29GL064N |
|---|---|
| TS048 | TS048, TS056 |
| SSO056 | N/A |
| LAA064 | LAA064 |
| FBE063 | VBK048 |

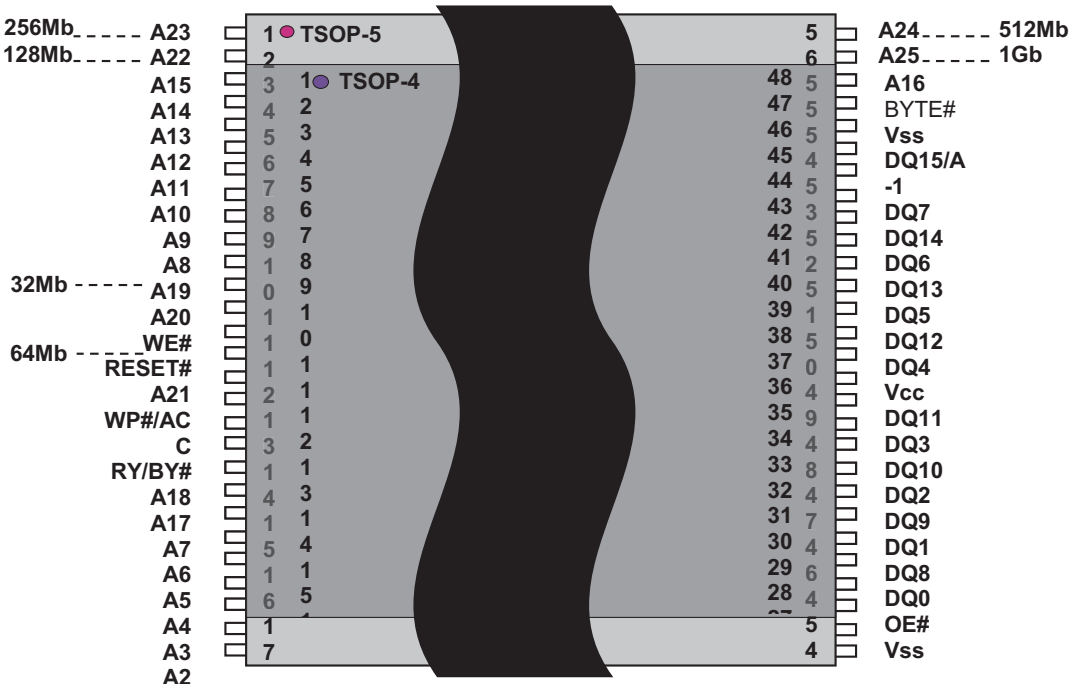
## 4.1 TSOP-48 to TSOP-56

Density migration with Spansion devices in the TSOP packages can run from 4 Mb to 1 Gb. For this feature to be enabled, one must place down the 56-pin TSOP footprint on the board. The 56-pin TSOP footprint can be populated with either the TSOP-56 package or properly justified TSOP-32, TSOP-40 or TSOP-48 packages.

Similarly, when one migrates from the Am29LV64xD in the TS048 package to the S29GL064N, you could place the 56-pin TSOP footprint onto the board and fill it with either the TSO48 package or the TSO56 package.

Figure 4.1 shows the pin mapping with the 48-pin and 56-pin packages.

**Figure 4.1** TSOP-48 to TSOP-56 Package Migration

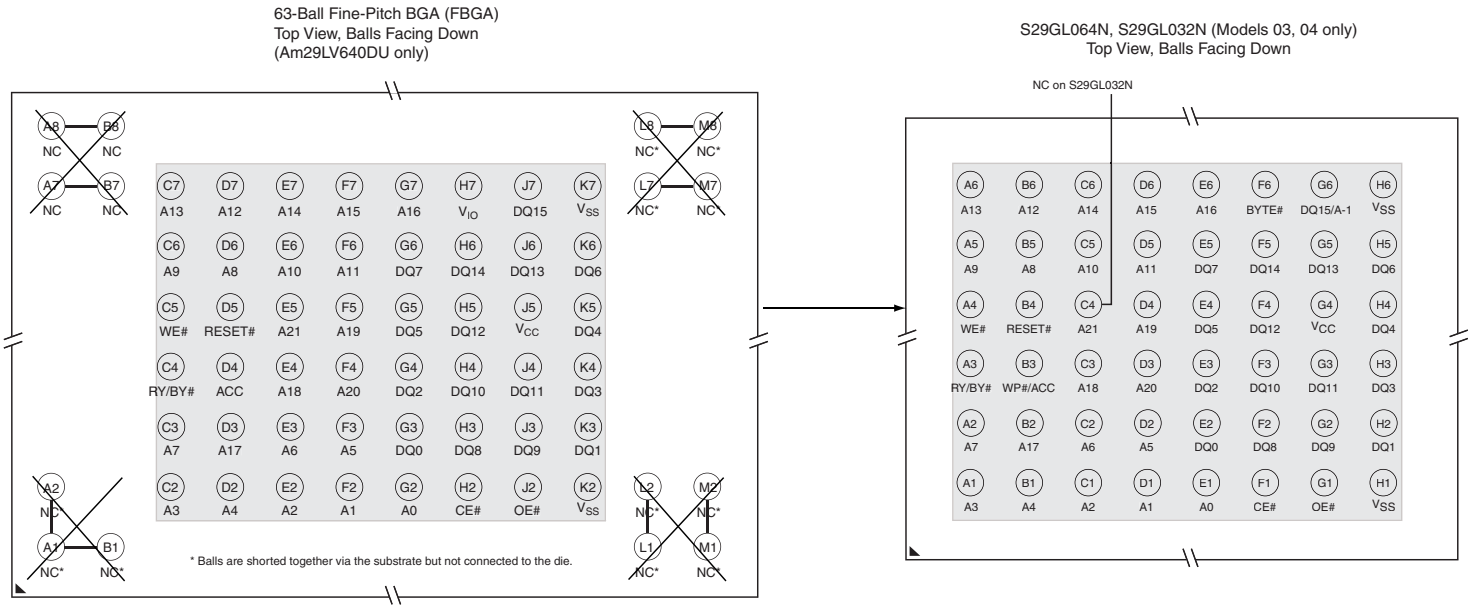


## 4.2 FBE063 to VBK048 Package

Another package migration involves the FBE063 package to the VBK048 package. The core footprint of the FBE063 maps to the footprint of the VBK048. However, the outrigger balls of the FBE063 package are not required with the VBK048 package and have been removed.

The diagram in Figure 4.2 shows how this physical mapping occurs.

**Figure 4.2** Migration from the FBE063 Package to the VBK048 Package



# 5. Revision History

| Section | Description |
|---|---|
| **Revision 01 (January 3, 2012)** | |
| | Initial release |

### *Colophon*

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