AN217010

Migrating from S25FL1-K Serial NOR Flash to S25FL064L Serial NOR Flash

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Associated Part Family: S25FL-L

AN217010 provides guidelines for migrating from Cypress' S25FL1-K family of serial NOR Flash to the S25FL064L serial NOR Flash product. It describes the similarities and differences in specifications between them to facilitate this conversion.

Contents

1 Introduction

This document provides guidelines for migrating from Cypress' S25FL1-K Serial NOR Flash to the S25FL064L Serial NOR Flash family of products. It discusses the known differences that may be encountered when facilitating this conversion.

The S25FL1-K family is a 3.0-V, single-supply flash memory based on 90-nm floating gate technology. The S25FL064L is also a 3.0-V, single-supply flash memory device, but it is based on an advanced 65-nm floating gate process technology. The S25FL064L flash offers additional features such as extended 4-byte addressing to enable access for densities higher than 16 MB (128 Mb), array protection, individual and regional protection, read/write any register, Double Data Rate (DDR), and Quad Peripheral Interface (QPI). See the S25FL064L datasheet for a full description of all new features and functions.

2 Feature Comparison

S25FL064L supports a superset of the S25FL1-K feature set. Table 1 summarizes the feature similarities and differences, which are discussed in detail in later sections. S25FL1-K features that are not supported or that are different in the S25FL-L are highlighted in yellow.

Table 1. Feature Comparison

Feature/Parameter	S25FL1-K	S25FL064L
Technology Node	90-nm NOR Flash	65-nm NOR Flash
Architecture	Floating Gate	Floating Gate
Density	64 Mb, 32 Mb, 16 Mb	64 Mb
Bus Width	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7 V–3.6 V	2.7 V–3.6 V
Normal Read Speed (SIO)	6.25 MBps (50 MHz)	6.25 MBps (50 MHz)
Fast Read Speed (SIO)	13.5 MBps (108 MHz)	13.5 MBps (108 MHz)
Dual Read Speed (DIO)	27 MBps (108 MHz)	27 MBps (108 MHz)
Quad Read Speed (QIO)	52 MBps (108 MHz)	52 MBps (108 MHz)
Quad Read Speed (QIO-DDR)	–	54 MBps (54 MHz)
Program Buffer Size	256 Bytes	256 Bytes
Erase Sector/Block Size	4 KB/64 KB	4 KB/32 KB/64 KB
Parameter Sector Size	4 KB	–
Security Registers	Three 256-Byte	Four 256-Byte
Data Protection	Legacy Block Pointer Region	Legacy Block Pointer Region Individual Block Lock
Suspend/Resume	Erase/Program	Erase/Program
Addressing	3 Byte	3-Byte or 4-Byte plus Bank Address Register
Hardware Reset	No	Yes
Operating Temperature	–40 °C to +85 °C	–40 °C to +85 °C
	–40 °C to +105 °C	–40 °C to +105 °C
	No	–40 °C to +125 °C
Deep Power Down	Yes – 2 µA (typical)	Yes – 2 µA (typical)
ID and SFDP Interface	Yes	Yes
Packages	8-lead SOIC (208 mils)	8-lead SOIC (208 mils)
	8-Contact WSON (5x6 mm)	USON (4x4 mm)
	24-Ball FBGA (6x8 mm)	24-Ball FBGA (6x8 mm)
	16-lead SOIC (300 mil)	16-lead SOIC (300 mil)
	KGD/KGW	KGD

S25FL116K and S25FL132K densities migrate to the S25FL064L.
The S25FL1-K family has 4-KB parameter sectors that are not uniformly distributed across the flash array. However, S25FL064L has uniform 4-KB sectors, so every parameter sector in S25FL1-K maps to a 4-KB sector in S25FL064L.

The Known Good Wafer (KGW) option provided for the S25FL1-K family is not supported in S25FL064L.

3 Status and Configuration Registers

The initial power-up and post-power-up configuration of S25FL1-K and S25FL064L devices are determined by configuration bits stored in the internal configuration registers. The status registers, in addition to storing some configuration bits, also provide the status for embedded operations. Table 2 shows the compatible registers for each device family. Table 3 through Table 5 show register bit comparisons.

Table 2. Compatible Registers

Register Read Command	S25FL1-K Registers		S25FL064L Registers	
	Register Name	Default State	Register Name	Default State
05h	Status Register 1 (SR1)	00h	Status Register 1 (SR1)	00h
07h	–	–	Status Register 2 (SR2)	00h
35h	Status Register 2 (SR2)	04h	Configuration Register 1 (CR1)	00h
15h	–	–	Configuration Register 2 (CR2)	60h
33h	Status Register 3 (SR3)	70h	Configuration Register 3 (CR3)	78h

Table 3. Status Register 1 (SR1) Bits Are Identical for Both Devices

SR1 Bit	S25FL1-K and S25FL064L		
	Name	Function	Default
7	SRP0	Status Register Protect 0	0
6	SEC	Sector/Block Protect	0
5	TBPROT	Top/Bottom Protect	0
4	BP2	Block Protect Bits	0
3	BP1		0
2	BP0		0
1	WEL	Write Enable Latch	0
0	WIP	Write In Progress	0

Table 4. Register Bits Comparison (SR2 Versus CR1)

Bit	S25FL1-K (SR2)			S25FL064L (CR1)		
	Name	Function	Default	Name	Function	Default
7	SUS	Suspend Status	0	SUS	Suspend Status	0
6	CMP	Complement Protect	0	CMP	Complement Protect	0
5	LB3	Security Register Lock Bits	0	LB3	Security Region Lock Bits	0
4	LB2		0	LB2		0
3	LB1		0	LB1		0
2	LB0		1	LB0		0
1	QE	Quad Enable	0 or 1[1]	QUAD	Quad I/O mode	0
0	SRP1	Status Register Protect 1	0	SRP1	Status Register Protect 1	0

[1] The default setting depends upon the model number in the ordering part number: QUAD=1 for model number "Q1"; otherwise QUAD=0. See the S25FL1-K datasheet for details.

Table 5. Register Bits Comparison (SR3 Versus CR3)

Bit	S25FL1-K (SR3)			S25FL064L (CR3)		
	Name	Function	Default	Name	Function	Default
7	RFU	Reserved	0	RFU	Reserved	0
6	W6	Burst Wrap Length	1	WL	Wrap Length	1
5	W5		1			1
4	W4	Burst Wrap Enable	1	WE	Wrap Enable	1
3	LC	Variable Read Latency Control	0[1]	RL	Read Latency	1[1]
2			0			0
1			0			0
0			0			0

[1] The default settings are for up to 108 MHz and have the same number of mode and dummy bytes for Fast Read (0Bh), Dual Output Read (3Bh), and Quad Output Read (6Bh); the mode and dummy byte counts are different for Dual I/O Read (BBh) and Quad I/O Read (EBh).

Latency codes in the S25FL1-K SR3 register and S25FL064L CR3 register define how many mode cycles and dummy cycles are required for each read command. Mode cycles are used by the host to control special features of the read command. Dummy cycles are used to wait for the initial read access time required for a given clock frequency for that read command. Table 6 shows the default number of mode and dummy cycles for each shared read command for the two device families for frequencies up to 108 MHz.

Table 6. Default Number of Dummy Cycles

Command	S25FL1-K		S25FL064L	
	Mode	Dummy	Mode	Dummy
Fast Read (0Bh)	0	8	0	8
Dual Output Read (3Bh)	0	8	0	8
Dual I/O Read (BBh)	4	0	4	8
Quad Output Read (6Bh)	0	8	0	8
Quad I/O Read (EBh)	2	4	2	8

See the datasheets for detailed tables showing how to tune the latency codes for each command over frequency.

4 Command Set Comparison

Table 7 summarizes the supported commands for each device. Key differences are highlighted in yellow.

Table 7. Command Set Comparison

Function	Command	Description	S25FL164K[3] S25FL132K[3] S25FL116K[3]	S25FL064L[4]
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Fh	9Fh
	RDQID	Read Quad ID	–	AFh
	RUID	Read Unique ID	5Ah	4Bh
	READ_ID	Read Manufacturer and Device Identification	90h	–
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah[1]
Register Access	RDSR1	Read Status Register 1	05h	05h
	RDSR2	Read Status Register 2	–	07h
	RDCR1/RDSR 2	Read Configuration Register 1/Status Register 2	35h	35h
	RDCR2	Read Configuration Register 2	-–	15h
	RDCR3/RDSR 3	Read Configuration Register 3/Status Register 3	33h	33h
	WRR	Write Register (Status-1 and Conf-1,2,3) / (Status – 1,2,3)	01h	01h
	WRDI	Write Disable	04h	04h
	WREN	Write Enable for Nonvolatile Data Change	06h	06h
	WRENV	Write Enable for Volatile Status and Configuration Registers	50h	50h
	CLSR	Clear Status Register	–	30h
	4BEN	Enter 4-Byte Address Mode	–	B7h
	4BEX	Exit 4-Byte Address Mode	–	E9h
	SBL	Set Burst Length	77h	77h
	QPIEN	Enter QPI	–	38h
	QPIEX	Exit QPI	–	F5h
	DLPRD	Data Learning Pattern Read	–	41h
	PDLRNV	Program NV Data Learning Register	–	43h
	WDLRV	Write Volatile Data Learning Register	–	4Ah
	RDAR	Read Any Register	–	65h[1]
	WRAR	Write Any Register	–	71h[1]
Read Flash Array	READ	Read	03h	03h[1]
	FAST_READ	Fast Read	0Bh	0Bh[1]
	DOR	Dual Output Read	3Bh	3Bh[1]
	QOR	Quad Output Read	6Bh	6Bh[1]
	DIOR	Dual I/O Read	BBh	BBh[1]
	QIOR	Quad I/O Read	EBh	EBh[1]

Function	Command	Description	S25FL164K[3] S25FL132K[3] S25FL116K[3]	S25FL064L[4]
	DDRQIOR	DDR Quad I/O Read	–	Edh[1]
	4READ	Read	–	13h[2]
	4FAST_READ	Fast Read	–	0Ch[2]
	4DOR	Dual Output Read	–	3Ch[2]
	4QOR	Quad Output Read	–	6Ch[2]
	4DIOR	Dual I/O Read	–	BCh[2]
	4QIOR	Quad I/O Read	–	ECh[2]
	4DDRQIOR	DDR Quad I/O Read	–	EEh[2]
Program Flash Array	PP	Page Program	02h	02h[1]
	QPP	Quad Page Program	–	32h[1]
	4PP	Page Program	–	12h[2]
	4QPP	Quad Page Program	–	34h[2]
Erase Flash Array	CE	Chip Erase/Bulk Erase	60h	60h
	CE	Chip Erase/Bulk Erase (alternate instruction)	C7h	C7h
	SE	Sector Erase	20h	20h[1]
	HBE	Half Block Erase	–	52h[1]
	BE	Block Erase	D8h	D8h[1]
	4SE	Sector Erase	–	21h[2]
	4HBE	Half Block Erase	–	53h[2]
	4BE	Block Erase	–	DCh[2]
Erase/Program Suspend/Resume	EPS	Erase/Program Suspend	75h	75h
	EPR	Erase/Program Resume	7Ah	7Ah
Security Region Array	SECRE	Security Region Erase	44h	44h[1]
	SECRP	Security Region Program	42h	42h[1]
	SECRR	Security Region Read	48h	48h[1]
Array Protection	GBL	Global IBL Lock	–	7Eh
	GBUL	Global IBL Unlock	–	98h
	IBLRD	IBL Read	–	3Dh[1]
	IBL	IBL Lock	–	36h[1]
	IBUL	IBL Unlock	–	39h[1]
	SPRP	Set Pointer Region Protection	39h	FBh[1]
	4IBLRD	IBL Read	–	E0h[2]
	4IBL	IBL Lock	–	E1h[2]
	4IBUL	IBL Unlock	–	E2h[2]
	4SPRP	Set Pointer Region Protection	–	E3h[2]
Individual and Region Protection	IRPRD	IRP Register Read	–	2Bh
	IRPP	IRP Register Program	–	2Fh

Function	Command	Description	S25FL164K[3] S25FL132K[3] S25FL116K[3]	S25FL064L[4]
	PRRD	Protection Register Read	–	A7h
	PRL	Protection Register Lock (NVLOCK Bit Write)	–	A6h
	PASSRD	Password Read	–	E7h
	PASSP	Password Program	–	E8h
	PASSU	Password Unlock	–	EAh
Reset	RSTEN	Software Reset Enable	66h	66h
	RST	Software Reset	99h	99h
	MBR	Mode Bit Reset	FFh	FFh
Deep Power Down	DPD	Deep Power Down	B9h	B9h
	RES	Release from Deep Power Down/Device ID	ABh	ABh

[1] Legacy Commands Requiring 4-Byte Addressing after POR when CR2NV[1]=ADP_NV Is Set

[2] New Commands Requiring 4-Byte Addressing

[3] S25FL1-K uses a 3-byte (24-bit) address to access up to 16 MB (128 Mb) of flash address space.

[4] The S25FL-L supports 3-byte addressing to access up to 16 MB (128 Mb), and 4-byte addressing to access larger densities.

The two families have compatible ID read commands RDID (9Fh) and RSFDP (5Ah). The Unique ID is read via two different commands for the two families (5Ah versus 4Bh), and the READ_ID (90h) command is not supported in the S25FL-L. See the next two sections for additional details.

Even though the WRR (01h) command is the same for both device families, arguments for this command are different and are incompatible for certain register matchups. More details are provided in Section 4.3.

Another command difference is the SPRP command for the Pointer Region Protection which is different in the two families (39h versus FBh).

In addition, note that all 3-byte address commands that work in the S25FL1-K family can be used to address more than 16 MB (128 Mb) in the S25FL-L family by using the Bank Address Register to select the flash bank for the 3-byte address. To use 4-byte addressing, existing S25FL1-K command sequences must be modified to add another address cycle, but they can use the same command code so long as the register bit CR2NV[1]=ADP_NV is set. *Note that 4-byte addressing is not required for migration to the single-die S25FL064L.*

4.1 Device Identification

For the S25FL1-K family, the READ_ID (90h) command outputs one byte of manufacturer's identification, followed by one byte of device identification. Table 8 provides the byte sequence showing the Manufacturer and Device ID values output by the command. S25F064L does not support this command.

Table 8. S25FL1-K Manufacturer/Device ID Command Byte Sequence

Byte	Meaning	S25FL116K	S25FL132K	S25FL164K
1	Command	90h	90h	90h
2	Dummy	00h	00h	00h
3	Dummy	00h	00h	00h
4	Dummy	00h	00h	00h
5	Manufacturer	01h	01h	01h
6	Device ID	14h	15h	16h

The JEDEC ID or RDID (9Fh) command is supported by both families. This command outputs one byte of manufacturer identification followed by two bytes of device identification. Table 9 provides the byte sequence, showing the identification values output by the command.

Table 9. S25FL1-K and S25FL064L JEDEC ID Command Byte Sequence

Byte	Meaning	S25FL116K	S25FL132K	S25FL164K	S25FL064L
1	Command	9Fh	9Fh	9Fh	9Fh
2	Manufacturer	01h	01h	01h	01h
3	Device ID	40h	40h	40h	60h
4	Capacity	15h	16h	17h	17h

Serial Flash Discoverable Parameters (SFDP) are provided in both devices and are accessed by the RSDDP (5Ah) command. The SFDP table, which is address-based, is defined in the JEDEC-216B specification and consists of a header table that identifies the SFDP. See Table 10 for the SFDP address/byte sequences. Consult the datasheets for details on the SFDP data structure.

Table 10. SFDP Header and Parameter Address Map

	S25FL1-K	S25FL064L
SFDP Header Start	0000h	0000h
SFDP Header End	007Fh	02FFh
SFDP Parameter Start	0080h	0300h
SFDP Parameter End	00BFh	05FFh

4.2 Unique Identification

The Unique ID provides a 64-bit unique number for each device. In S25FL1-K, the unique ID number can be read by the RSFDP (5Ah) command with address F8h to FFh. S25FL064L provides a dedicated RUID (4Bh) command. The address map for unique identification for both devices is shown in Table 11.

Table 11. S25FL164K Unique ID Address Map

UID Byte	S25FL1-K	S25FL064L
0	F8h	00h
7	FFh	07h
8		08h
15		0Fh

4.3 Write Registers (WRR 01h) Differences

S25FL064L and S25FL1-K both support the WRR (01h) command, which allows new values to be written to the Status and Configuration registers. Table 12 compares the WRR command sequence; in this case the colored highlights show compatible registers. Table 13 for the register

Table 12. WRR (01h) Command Sequence

Byte	S25FL1-K	S25FL064L
1	WRR (01h)	WRR (01h)
2	SR1	SR1
3	SR2	CR1
4	SR3	CR2
5	-	CR3

WARNING

Byte 4 in S25FL1-K (SR3) and S25FL064L (CR2) are not compatible (see Table 13). Therefore, the WRR software must be changed to input a correct CR2 value in Byte-4 for the S25FL064L WRR sequence. Otherwise, writing the SR3 value (S25FL1-K) into the CR2 register (S25FL064L) can cause unexpected device behavior. Specifically, if QPI bit in CR2 is set inadvertently, the device can only be operated by QPI protocol where the commands input in quad mode via IO0 to IO3 and be no longer operated by legacy SPI protocol where the commands input in single I/O mode via IO0. This situation is critical for SPI host controllers that do not support QPI protocol because there is no way to reset QPI bit in CR2 by issuing WRR command in the QPI protocol.

Table 13. Register Mismatch for the WRR Command Sequence

Bit	S25FL1-K (SR3)			S25FL064L (CR2)		
	Name	Function	Default	Name	Function	Default
7	RFU	Reserved	0	IO3R_NV	IO3_Reset	0
6	W6	Burst Wrap Length	1	OI_NV	Output Impedance	1
5	W5		1			1
4	W4	Burst Wrap Enable	1	RFU	Reserved	1
3	LC	Variable Read Latency Control	1	QPI_NV	QPI	0
2			0	WPS_NV	Write Protect Selection	0
1			0	ADP_NV	Address Length at Power-Up	0
0			0	RFU	Reserved	0

4.4 Erase Endurance on Non-Volatile Register Array

S25FL064L and S25FL1-K both have 1K PE cycles endurance on non-volatile register array. In S25FL064L, each write to non-volatile registers that performed by WREN (06h) and WRR (01) commands causes PE cycle on non-volatile register array, even if rewriting registers with the same values. In the S25FL1-K family, rewriting with the same value does not cause PE cycles. For S25FL064L, it is highly recommended to write to volatile registers at system run time. Writing to volatile registers is performed by WRENV (50h) and WRR (01h) commands.

4.5 Deep Power-Down Mode

The S25FL1-K family of devices and S25FL064L both support Deep Power-Down modes. The same command can be used to read the device's electronic identification (ID) number.

4.6 Security Regions/Security Registers

Both S25FL1-K and S25FL064L support security regions consisting of four 256-byte regions, separately addressable from the main flash memory array. S25FL1-K Region 0 is used by Cypress to store and protect the SFDP information. The security regions that are not used for SFDP can be erased, programmed, and protected individually. Table 14 shows the address space regions for both devices.

Table 14. Secure Region Definitions

Security Region	Address (S25FL164K/132K/116K)	Address (S25FL064L)
0 (SFDP for S25FL-K)	0000h – 00FFh	0000h – 00FFh
1	1000h – 10FFh	0100h – 01FFh
2	2000h – 20FFh	0200h – 02FFh
3	3000h – 30FFh	0300h – 03FFh

4.7 Double Data Rate (DDR) Read Commands

S25FL064L supports the DDR Quad I/O Read command. A 4-byte address version of this command is also available. The S25FL1-K family does not support any DDR Read commands.

4.8 Data Protection

The S25FL1-K family of devices and S25FL064L flash devices implement data protection schemes that shield program and erase operations. Table 15 shows the data protection schemes supported in each device. For more details on the protection schemes, consult the respective device datasheets.

Table 15. Data Protection Scheme Supported

Data Protection Scheme	S25FL1-K	S25FL064L
Block Protection	Yes	Yes
Individual Block Lock Protection	-	Yes
Pointer Protection	Yes	Yes
Region Protection	Yes	Yes

4.9 Erase and Program Suspend/Resume Operations

S25FL1-K and S25FL064L support program and erase suspend and resume commands, which allow program and erase operations to be individually suspended (EPS:75h) and resumed (EPR: 7Ah) to access data in blocks that are not being modified. For S25FL064L, Status Register 2 is added to allow the host software to determine if a particular operation is in suspension. Also, the Read Status Register 2 (RDSR2:07h) command has been added to access this new register.

5 Hardware Comparison

Pertinent hardware differences are discussed in the subsequent sections.

5.1 Package Compatibility

Table 16. Package Compatibility

Package Name	16Mb	32Mb	64Mb		128Mb	256Mb
	S25FL116K	S25FL132K	S25FL164K	S25FL064L	S25FL128L	S25FL256L
8 - pin SOIC (208 mil)	✓	✓	✓	✓	✓	
8 - pin SOIC (150 mil)	✓	✓				
16 – pin SOIC (300mil)			✓	✓		✓
8 –Contact WSON (5x6 mm)	✓	✓	✓	✓	✓	
8 –Contact WSON (6x8 mm)						✓
8 –Contact USON (4x4 mm)		✓		✓		
5 x 5 ball FBGA (6 x 8 mm)	✓	✓	✓	✓	✓	✓
4 x 6 ball FBGA (6 × 8 mm)	✓	✓	✓	✓	✓	✓

5.2 HOLD Functionality

S25FL164K supports serial communications hold (stop) through the HOLD# pin. HOLD# is a multiplexed pin used during quad communication as IO3. S25FL064L does not support hold functionality. Instead, HOLD# is replaced by RESET# and acts like a hardware reset when CS# is HIGH. RESET# is again multiplexed with IO3 for Quad mode.

5.3 Software Reset

S25FL1-K and S25FL064L support the Software Rest command (RSTEN:66h, RESET:99h), which restores the device to its initial power-up state.

5.4 DC Parameters

Table 17 compares the DC parameters of S25FL164K and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 17. DC Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL1-K			S25FL064L			Units
		Min	Typical	Max	Min	Typical	Max	
V_{DD}	Supply Voltage	2.7	3	3.6	2.7	3	3.6	V
V_{DD} (min)	V_{DD} (minimum operation voltage)	2.7			2.7			V
V_{DD} (cutoff)	V_{DD} (cutoff where reinitialization is needed)	2.4			2.4			V
V_{DD} (low)	V_{DD} (low voltage for initialization to occur)	1			1			V
V_{IL}	Input Low Voltage	–0.5		0.3 x V_{DD} [1] 0.2 x V_{DD} [2]	–0.5		0.3 x V_{DD}	V
V_{IH}	Input High Voltage	0.7 x V_{DD}		V_{DD} +0.4	0.7 x V_{DD}		V_{DD} + 0.4	V
V_{OL}	Output Low Voltage			0.2			0.2	V
V_{OH}	Output High Voltage	V_{DD} – 0.2			V_{DD} – 0.2			V
I_{LI}	Input Leakage Current			±2			±4	µA
I_{LO}	Output Leakage Current			±2			±4	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR		9	13.5		25	35	mA
	Active Power Supply Current (READ) – Serial DDR					30	35	mA
I_{CC2}	Active Power Supply Current (Page Program)		20	25		40	50	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)		8	12		40	50	mA
I_{CC4}	Active Power Supply Current (SE)		20	25		40	50	mA
I_{CC5}	Active Power Supply Current (HBE, BE)		20	25		40	50	mA
I_{SB}	Standby Current		15	25		20	40	µA
I_{DPD}	Deep Power-Down Current		2	8 [1] 5 [2]		2	20	µA
I_{POR}	Power-On Reset Current					15	20	mA

Notes:

1. S25FL164K/S25FL132K.
2. S25FL116K

5.5 Single Data Rate (SDR) AC Parameters

Table 18 compares the AC parameters of the S25FL1-K family and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 18. SDR AC Parameter Comparison

Symbol	Parameter Operating Temperature Range (–40°C to +105°C)	S25FL1-K			S25FL064L			Units
		Min	Typ	Max	Min	Typ	Max	
f_{SCK} - 1	SCK Clock Frequency for dual and quad commands			108			108	MHz
f_{SCK} - 2	SCK Clock Frequency for READ and 4READ instructions			50			50	MHz
P_{SCK}	SCK Clock Period	9.25			1/ f_{SCK}			
t_{WH}, t_{CH}	Clock High Time	3.3			50% P_{SCK} -5%			ns
t_{WL}, t_{CL}	Clock Low Time	4.3			50% P_{SCK} -5%			ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1			0.1			V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1			0.1			V/ns
t_{CS}	CS# High Time (any Read instructions)	7			20			ns
	CS# High Time (all other non-Read instructions)	40			50			ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	5			3			ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	5			5			ns
t_{SU}	Data in Setup Time	2			3			ns
t_{HD}	Data in Hold Time	5			2			ns
t_V	Clock Low to Output Valid			7			8	ns
t_{HO}	Output Hold Time	2			1			ns
t_{DIS}	Output Disable Time			7			8	ns
t_{WPS}	WP# Setup Time	20			20			ns
t_{WPH}	WP# Hold Time	100			100			ns
t_{DP}	CS# High to Deep Power-Down Mode			3			3	µs
t_{RES}	CS# High to Release from Deep Power-Down Mode			3			5	µs
t_{QEN}	QIO or QPI Enter mode, time needed to issue next command						1.5	µs
t_{QEXN}	QIO or QPI Exit mode, time needed to issue next command						1	µs

Note:

1. All the AC parameters are same across densities in FL1-K family

5.6 Embedded Algorithm Performance

Table 19 compares the embedded algorithm performance parameters of S25FL1-K and S25FL064L. While most parameter differences should not cause performance issues when migrating, it is highly recommended that you carefully review all the parameter differences for any potential impact.

Table 19. Embedded Algorithm Performance Parameter Comparison

Symbol	Parameter Operating Temperature Range –40°C to +105°C	S25FL1-K			S25FL064L			Units
		Min	Typical	Max	Min	Typical	Max	
t_W	Nonvolatile Register Write Time		2	85		220	1200	ms
t_{PP}	Page Programming (256 bytes)		700	3000		450	1350	µs
t_{BP1}	Byte Programming (first byte)		15	50		75	90	µs
t_{BP2}	Additional Byte Programming (after first byte)		2.5	12		10	30	µs
t_{SE}	Sector Erase Time (4-KB physical sectors)		50	450		65	270	ms
t_{HBE}	Half Block Erase Time (32-KB physical sectors)					300	600	ms
t_{BE}	Block Erase Time (64-KB physical sectors)		500	2000		450	1150	ms
t_{CE}	Chip Erase Time		64	256		55	150	s

6 Summary

Migration from S25FL1-K to S25FL064L is straightforward and requires minimal accommodation with regard to either system software or hardware. After the accommodations are done, if required, the S25FL064L flash can enable the use of higher density devices with greater performance in existing systems and additional features of extended 4-byte addressing, array protection, individual and region protection, read/write any register, DDR, and QPI.

7 Related Documents

Table 20. Cypress SPI NOR Flash Product Datasheets

Product Family	Spec. Number	Title
FL1-K Family	002-00497	S25FL116K, S25FL132K, S25FL164K 16 Mbit (2 Mbyte), 32 Mbit (4 Mbyte), 64 Mbit (8 Mbyte) 3.0V SPI Flash Memory
FL-L Family	002-12878	S25FL064L Flash Datasheet – 64-Mbit (8-Mbyte) 3.0 V FL-L SPI Flash Memory

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5513895	BWHA	11/08/2016	New application note
*A	5807368	AESATMP8	07/10/2017	Updated logo and Copyright.
*B	5993870	TKUW	12/14/2017	Added FL116K and FL132K information Updated tables format Added detailed explanations for register difference Added Erase Endurance on Non-Volatile register Added Package Compatibility
*C	6252181	ZHFE	07/18/2018	Minor update in Table 1

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