AN218107

Migration from S25FL-S to S25FL-L Serial NOR Flash Memory

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Associated Part Family: S25FL-L

AN218107 provides guidelines for migration from Cypress's S25FL-S to S25FL-L Serial NOR Flash Memory products. It describes the similarities and differences in specifications to facilitate this conversion.

Contents

1 Introduction

The S25FL-S family is a 3.0-V Flash memory device based on the 65-nm MirrorBit® process technology. The S25FL-L family is a 3.0-V, single-supply (no V_{IO} power supply), 4-KB uniform sector Flash memory device based on the 65-nm Floating Gate process technology. The S25FL-L family of Flash devices is the first Cypress product with uniform 4-KB sectors that also has performance and features that are comparable to the S25FL-S family of Flash devices. This document provides guidelines for migrating from the 128-Mbit and 256-Mbit densities of the S25FL-S and S25FL-L families by comparing and contrasting each feature in turn.

2 Features Comparison

The S25FL-L family is command-subset-compatible and footprint-compatible with the S25FL-S family. Table 1 summarizes the feature similarities and differences between 256-Mb and 128-Mb density devices from each family.

Table 1. Features Comparison

Feature/Parameter	S25FL256L S25FL128L	S25FL256S S25FL128S	S25FL127S
Technology Node	65-nm NOR Flash	65-nm NOR Flash	65-nm NOR Flash
Architecture	Floating Gate	MirrorBit®	MirrorBit®
Density	256 Mb (S25FL256L) 128 Mb (S25FL128L)	256 Mb (S25FL256S) 128 Mb (S25FL128S)	128 Mb
Bus Width	x1, x2, x4	x1, x2, x4	x1, x2, x4
Supply Voltage	2.7 V – 3.6 V	2.7 V – 3.6 V / 1.65 V– 3.6 V V_{IO}	2.7 V – 3.6 V
Normal Read Speed (SIO)	6.25 MB/s (50MHz)	6.25 MB/s (50 MHz)	6.25 MB/s (50 MHz)
Fast Read Speed (SIO)	16.6 MB/s (133 MHz)	16.6 MB/s (133 MHz)	13.5 MB/s (108 MHz)
Dual Read Speed (DIO)	33.3 MB/s (133 MHz)	26 MB/s (104 MHz)	27 MB/s (108 MHz)
Quad Read Speed (QIO)	66.6 MB/s (133 MHz)	52 MB/s (104 MHz)	54 MB/s (108 MHz)
Quad Read Speed (QIO - DDR)	66 MB/s (66 MHz)	80 MB/s (80 MHz)	-
Program Buffer Size	256B	512B or 256B	512B or 256B
Erase Sector Size	4 KB / 32 KB / 64 KB	256 KB or 64 KB	256 KB or 64 KB
Parameter Sector Size	–	4 KB	4 KB
Security Region / OTP	1024B	1024B	1024B
Data Protection	Legacy Block Protection Individual and Region Protection	Legacy Block Protection Advanced Sector Protection	Legacy Block Protection Advanced Sector Protection
Suspend / Resume	Erase / Program	Erase / Program	Erase / Program
Addressing	3 / 4 Byte	3 / 4 Byte + Bank	3 / 4 Byte + Bank
Hardware Reset	Yes	Yes	Yes
Operating Temperature	–40°C to +85°C –40°C to +105°C –40°C to +125°C	–40°C to +85°C –40°C to +105°C –40°C to +125°C	–40°C to +85°C –40°C to +105°C
Deep Power Down	Yes – 2 µA (typical)	No	No
ID and CFI	No	Yes	Yes
ID and SFDP	Yes	No	Yes
Packages	8-pin SOIC (208 mils)[1] 16-pin SOIC (300 mils)[2] 8-Contact WSON (5 × 6 mm)[1] 8-Contact WSON (6 × 8 mm)[2] 24-Ball FBGA (6 × 8 mm)	16-pin SOIC (300 mils) 8-Contact WSON (6 × 8 mm) 24-Ball FBGA (6 × 8 mm)	8-pin SOIC (208 mils) 16-pin SOIC (300 mils) 8-Contact WSON (5 × 6 mm) 24-Ball FBGA (6 × 8 mm)

[1] S25FL128L only

[2] S25FL256L only

3 Sector Architecture

The S25FL-L family has a uniform sector architecture with 4-KB sectors, 32-KB half blocks, and 64-KB blocks. The S25FL-S family has two options for sector architecture depending on the Ordering Part Number (OPN). One is a hybrid sector size option with 64-KB sectors and 4-KB parameter sectors. Another option is uniform 256-KB sectors. Since the sector architectures are different, the S25FL-L and S25FL-S families offer different sector address maps. Table 2 and Table 3 show the sector address map comparison for S25FL256L and S25FL256S.

Table 2. Sector Address Map Comparison (Bottom 256 KB Address Range)

Address Range	S25FL256L			S25FL256S		
				Hybrid 64 KB + 4 KB		Uniform 256 KB
				CR1[2] = 0	CR1[2] = 1	
0000000h – 0000FFFh	Sector 0	Half Block 0	Block 0	Sector 0	Sector 0	Sector 0
…	…			…		
0007000h – 0007FFFh	Sector 7			Sector 7		
0008000h – 0008FFFh	Sector 8	Half Block 1		Sector 8		
…	…			…		
000F000h – 000FFFFh	Sector 15			Sector 15		
0010000h – 0010FFFh	Sector 16	Half Block 2	Block 1	Sector 16	Sector 1	
…	…			…		
0017000h – 0017FFFh	Sector 23			Sector 23		
0018000h – 0018FFFh	Sector 24	Half Block 3		Sector 24		
…	…			…		
001F000h – 001FFFFh	Sector 31			Sector 31		
0020000h – 0020FFFh	Sector 32	Half Block 4	Block 2	Sector 32	Sector 2	
…	…					
0027000h – 0027FFFh	Sector 39					
0028000h – 0028FFFh	Sector 40	Half Block 5				
…	…					
002F000h – 002FFFFh	Sector 47					
0030000h – 0030FFFh	Sector 48	Half Block 6	Block 3	Sector 33	Sector 3	
…	…					
0037000h – 0037FFFh	Sector 39					
0038000h – 0038FFFh	Sector 40	Half Block 7				
…	…					
003F000h – 003FFFFh	Sector 63					

Table 3. Sector Address Map Comparison (Top 256 KB Address Range)

Address Range	S25FL256L			S25FL256S		
				Hybrid 64 KB + 4 KB		Uniform 256 KB
				CR1[2] = 0	CR1[2] = 1	
1FC0000h – 1FC0FFFh	Sector 8128	Half Block 1016	Block 508	Sector 538	Sector 508	Sector 127
…	…					
1FC7000h – 1FC7FFFh	Sector 8135					
1FC8000h – 1FC8FFFh	Sector 8136	Half Block 1017				
…	…					
1FCF000h – 1FCFFFFh	Sector 8143					
1FD0000h – 1FD0FFFh	Sector 8144	Half Block 1018	Block 509	Sector 539	Sector 509	
…	…					
1FD7000h – 1FD7FFFh	Sector 8151					
1FD8000h – 1FD8FFFh	Sector 8152	Half Block 1019				
…	…					
1FDF000h – 1FDFFFFh	Sector 8159					
1FE0000h – 1FE0FFFh	Sector 8160	Half Block 1020	Block 510	Sector 540	Sector 510	
…	…				…	
1FE7000h – 1FE7FFFh	Sector 8167				Sector 517	
1FE8000h – 1FE8FFFh	Sector 8168	Half Block 1021			Sector 518	
…	…				…	
1FEF000h – 1FEFFFFh	Sector 8175				Sector 525	
1FF0000h – 1FF0FFFh	Sector 8176	Half Block 1022	Block 511	Sector 541	Sector 526	
…	…				…	
1FF7000h – 1FF7FFFh	Sector 8183				Sector 533	
1FF8000h – 1FF8FFFh	Sector 8184	Half Block 1023			Sector 534	
…	…				…	
1FFF000h – 1FFFFFFh	Sector 8191				Sector 541	

4 Command Set Comparison

Table 4 summarizes the commands supported for each device family. Subsequent sections discuss pertinent differences between the families.

Table 4. Command Set Comparison

Function	Command	Description	S25FL-L	S25FL-S
Read Device ID	RDID	Read ID (JEDEC Manufacturer ID)	9Fh	9Fh
	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah[1]
	RDQID	Read Quad ID	AFh	–
	RUID	Read Unique ID	4Bh	–
	READ_ID	Read Manufacturer and Device Identification	–	90h
	RES	Read Electronic Signature		ABh
Register Access	RDSR1	Read Status Register 1	05h	05h
	RDSR2	Read Status Register 2	07h	07h
	RDCR1	Read Configuration Register 1	35h	35h
	RDCR2	Read Configuration Register 2	15h	–
	RDCR3	Read Configuration Register 3	33h	–
	RDAR	Read Any Register	65h	–
	WRR	Write Register (Status-1 and Configuration-1,2,3)	01h	–
	WRR	Write Register (Status-1 and Configuration-1)	–	01h
	WRDI	Write Disable	04h	04h
	WREN	Write Enable for Non-volatile data change	06h	06h
	WRENV	Write Enable for Volatile Status and Configuration Registers	50h	–
	WRAR	Write Any Register	71h	–
	CLSR	Clear Status Register	30h	30h
	4BEN	Enter 4 Byte Address Mode	B7h	–
	4BEX	Exit 4 Byte Address Mode	E9h	–
	BRRD	Bank Register Read	–	16h
	BRWR	Bank Register Write	–	17h
	BRAC	Bank Register Access	–	B9h
	SBL	Set Burst Length	77h	–
	QPIEN	Enter QPI (Quad SPI 4-4-4)	38h	–
	QPIEX	Exit QPI (Quad SPI 4-4-4)	F5h	–
	DLPRD	Data Learning Pattern Read	41h	41h[2]
	PDLRNV	Program NV Data Learning Register	43h	43h[2]
	WDLRV	Write Volatile Data Learning Register	4Ah	4Ah[2]
	ECCRD	ECC Read (4-Byte Address)	–	18h[2]
	ABRD	AutoBoot Register Read	–	14h
	ABWR	AutoBoot Register Write	–	15h

[1] S25FL127S only

[2] Not supported by S25FL127S

Function	Command	Description	S25FL-L	S25FL-S
Read Flash Array	READ	Read	03h	03h
	4READ	Read (4-Byte Address)	13h	13h
	FAST_READ	Fast Read	0Bh	0Bh
	4FAST_READ	Fast Read (4-Byte Address)	0Ch	0Ch
	DDRFR	DDR Fast Read	–	0Dh[1]
	4DDRFR	DDR Fast Read (4-Byte Address)	–	0Eh[1]
	DOR	Dual Output Read	3Bh	3Bh
	4DOR	Dual Output Read (4-Byte Address)	3Ch	3Ch
	QOR	Quad Output Read	6Bh	6Bh
	4QOR	Quad Output Read (4-Byte Address)	6Ch	6Ch
	DIOR	Dual I/O Read	BBh	BBh
	4DIOR	Dual I/O Read (4-Byte Address)	BCh	BCh
	QIOR	Quad I/O Read	EBh	EBh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh	ECh
	DDRDIOR	DDR Dual I/O Read	–	BDh[1]
	4DDRDIOR	DDR Dual I/O Read (4-Byte Address)	–	BEh[1]
	DDRQIOR	DDR Quad I/O Read	EDh	EDh[1]
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh	EEh[1]
Program Flash Array	PP	Page Program	02h	02h
	4PP	Page Program (4-Byte Address)	12h	12h
	QPP	Quad Page Program	32h	32h / 38h
	4QPP	Quad Page Program (4-Byte Address)	34h	34h
Erase Flash Array	SE	Sector Erase	20h	–
	4SE	Sector Erase (4-Byte Address)	21h	–
	P4E	4-KB Parameter Sector Erase	–	20h
	4P4E	4-KB Parameter Sector Erase (4-Byte Address)	–	21h
	HBE	Half Block Erase	52h	–
	4HBE	Half Block Erase (4-Byte Address)	53h	–
	BE	Block Erase	D8h	–
	4BE	Block Erase (4-Byte Address)	DCh	–
	SE	64-KB or 256-KB Sector Erase	–	D8h
	4SE	64-KB or 256-KB Sector Erase (4-Byte Address)	–	DCh
	CE	Chip Erase / Bulk Erase	60h	60h
	CE	Chip Erase / Bulk Erase (alternate instruction)	C7h	C7h
Erase / Program Suspend / Resume	EPS	Erase / Program Suspend	75h	–
	EPR	Erase / Program Resume	7Ah	–
	ERSP	Erase Suspend	–	75h
	ERRS	Erase Resume	–	7Ah

[1] Not supported by S25FL127S

Function	Command	Description	S25FL-L	S25FL-S
	PGSP	Program Suspend	–	85h
	PGRS	Program Resume	–	8Ah
Security Region Array	SECRE	Security Region Erase	44h	–
	SECRP	Security Region Program	42h	–
	SECRR	Security Region Read	48h	–
	OTPP	Programs one byte of data in OTP memory space	–	42h
	OTPR	Read data in the OTP memory space	–	4Bh
Array Protection	IBLRD	IBL Read	3Dh	–
	4IBLRD	IBL Read (4-Byte Address)	E0h	–
	IBL	IBL Lock	36h	–
	4IBL	IBL Lock (4-Byte Address)	E1h	–
	IBUL	IBL Unlock	39h	–
	4IBUL	IBL Unlock (4-Byte Address)	E2h	–
	GBL	Global IBL Lock	7Eh	–
	GBUL	Global IBL Unlock	98h	–
	SPRP	Set Pointer Region Protection	FBh	–
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h	–
Individual and Region Protection	IRPRD	IRP Register Read	2Bh	–
	IRPP	IRP Register Program	2Fh	–
	PRRD	Protection Register Read	A7h	–
	PRL	Protection Register Lock (NVLOCK Bit Write)	A6h	–
	PASSRD	Password Read	E7h	–
	PASSP	Password Program	E8h	–
	PASSU	Password Unlock	EAh	–
Advanced Sector Protection	DYBRD	DYB Read	–	E0h
	DYBWR	DYB Write	–	E1h
	PPBRD	PPB Read	–	E2h
	PPBP	PPB Program	–	E3h
	PPBE	PPB Erase	–	E4h
	PLBRD	PPB Lock Bit Read	–	A7h
	PLBWR	PPB Lock Bit Write	–	A6h
	ASPRD	ASP Read	–	2Bh
	ASPP	ASP Program	–	2Fh
	PASSRD	Password Read	–	E7h
	PASSP	Password Program	–	E8h
	PASSU	Password Unlock	–	E9h
Reset	RSTEN	Software Reset Enable	66h	–
	RST/RESET	Software Reset	99h	F0h
	MBR	Mode Bit Reset	FFh	FFh
Deep Power Down	DPD	Deep Power Down	B9h	–

Function	Command	Description	S25FL-L	S25FL-S
	RES	Release from Deep Power Down / Device ID	ABh	–

4.1 Identification Commands

4.1.1 Read Identification (RDID 9Fh)

The S25FL-L family and the S25FL-S family both support the RDID (9Fh) command, which outputs manufacturer identification and device identification. The S25FL-S family also outputs the JEDEC Common Flash Interface (CFI) after three bytes of identification. Table 5 provides the comparison of the ID field definitions. The S25FL-L family does not have CFI tables.

Table 5. Read Identification (RDID 9Fh) Field Definitions

Byte #	Description	S25FL256L S25FL128L	S25FL256S S25FL128S S25FL127S
1	Manufacturer ID for Cypress	01h	01h
2	Device ID – Memory Interface Type	60h	02h (256 Mb) 20h (128 Mb)
3	Device ID – Density and Features	19h (256 Mb) 18h (128 Mb)	19h (256 Mb) 18h (128 Mb)
4	ID-CFI Length	Undefined	4Dh
5	Sector Architecture	Undefined	00h (256-KB Sector) 01h (64-KB Sector)
6	Family ID	Undefined	80h
7 - 8	ASCII characters for Model	Undefined	xxh (Model Number)
9 -15	Reserved	Undefined	xxh
16 -	CFI	Undefined	xxh

4.1.2 Read Quad Identification (RDQID AFh)

The S25FL-L family supports the RDQID (AFh) command, which provides the same information as the RDID (9Fh) command in QPI mode. The S25FL-S family does not support the RDQID command.

4.1.3 Read Serial Flash Discoverable Parameters (RSFDP 5Ah)

The S25FL-L family supports the RSFDP (5Ah) command, which outputs the Serial Flash Discoverable Parameters (SFDP). JEDEC (JEDEC-216B) defines the SFDP parameters and consists of a header table, which identifies the SFDP parameters. The S25FL127S device also supports SFDP; however, the number of parameter headers and parameter table contents are different from that of the S25FL-L family. For details regarding the SFDP byte contents, refer to the S25FL256L/S25FL128L and S25FL127S datasheets.

4.1.4 Unique Identification (RUID 4Bh)

The S25FL-L family provides a 64-bit unique number for each device via the RUID (4Bh) command. This can be an alternative feature to the Cypress Programmed Random Number supported by the S25FL-S family.

4.2 Status and Configuration Registers

The S25FL-L family and S25FL-S family both have Status and Configuration registers to report the status of device operations and to configure how the device operates. Table 6 summarizes the Status and Configuration Register Set comparison. The S25FL-L family has a nonvolatile and volatile version of each register. During Power-On Reset (POR), hardware reset, or software reset, the device copies the nonvolatile version of a register to the volatile version to provide the default state of the volatile register. For details regarding the nonvolatile and the volatile register functionalities, refer to the S25FL-L family datasheet.

Table 6. Register Set Comparison

Register Name	Register Features	S25FL-L	S25FL-S
Status Register 1	Reports ready/busy status and controls block protection functions	✓	✓
Status Register 2	Reports erase/program suspend status	✓	✓
Configuration Register 1	Controls certain interface and block protection functions	✓	✓
Configuration Register 2	Controls certain interface functions	✓	
Configuration Register 3	Controls read commands burst wrap behavior and read latency	✓	

Although the S25FL-L family and S25FL-S family both provide the same command codes for reading Status Register 1, 2, and Configuration Register 1, register bits assignments are different. Table 7 shows the at-a-glance comparison of status and configuration register bits assignments. Note that the functions of SR1V[6:5] are different between S25FL256L and the S25FL128L. For details of each status register bit, refer to the device-specific datasheet.

Table 7. Status Register Bits Comparison

Bits	Status Register 1			Status Register 2			Configuration Register 1	
	S25FL256L	S25FL128L	S25FL-S	S25FL-L	S25FL256S S25FL128S	S25FL127S	S25FL-L	S25FL-S
7	SRP0		SRWD	RFU		D8h_O	SUS	LC1
6	TBPROT	SEC	P_ERR	E_ERR	RFU	02h_O	CMP	LC0
5	BP3	TBPROT	E_ERR	P_ERR	RFU	IO3R_O	LB3	TBPROT
4	BP2			RFU			LB2	RFU
3	BP1			RFU			LB1	BPNV
2	BP0			RFU			LB0	TBPARM
1	WEL			ES			QUAD	
0	WIP			PS			SRP1	FREEZE

4.3 Read Latency

Some read commands require a read latency to allow time to access the Flash memory array. The read latency cycles are traditionally called dummy cycles. The number of dummy cycles can be configured in both the S25FL-L family (CR3[3:0]) and the S25FL-S family (CR1[7:6]); however, the strategy for the dummy cycles settings are different.

In the S25FL-L family, the 4-bit wide latency code bits for CR3[3:0] represents the exact number of dummy cycles (except 0000b, which represents 8 dummy cycles). In the S25FL-S family, the 2-bit wide latency code bits for CR1[7:6] represents the pointer to the pre-defined number of dummy cycles. Table 8 maps the latency code bits of both device families. Note that the maximum clock frequency supported per latency code bits setting is different in both device families.

For example, the S25FL-L family supports 65 MHz in QIOR with four dummy cycles, while the S25FL-S family supports 90 MHz. For details of the latency code bits including maximum clock frequency, refer to the device-specific datasheet.

Table 8. Latency Code Bits Map

S25FL-L CR3[3:0]	S25FL-S CR1[7:6]					
	FAST_READ	DOR	QOR	DIOR	QIOR	DDRQIOR
0000 (8)	00 / 01 / 10	00 / 01 / 10	00 / 01 / 10	–	–	10
0001 (1)	–	–	–	01	11	–
0010 (2)	–	–	–	10	–	–
0011 (3)	–	–	–	–	–	11
0100 (4)	–	–	–	–	00 / 01	–
0101 (5)	–	–	–	–	10	–
0110 (6)	–	–	–	–	–	00
0111 (7)	–	–	–	–	–	01
1000 (8)	00 / 01 / 10	00 / 01 / 10	00 / 01 / 10	–	–	10
1001 (9) ~ 1111 (15)	–	–	–	–	–	–

4.4 Extended Addressing

The S25FL-L family and S25FL-S family both support 4-byte addresses to access devices with densities higher than 128 Mb (16 MB). Table 9 shows the options to enable the extended addressing supported by the S25FL-L family and S25FL-S family.

Table 9. Extended Addressing Options

Option	S25FL-L	S25FL-S
4-Byte Address Commands	Supported	Supported
Extended Address Mode	Supported	Supported
Bank Address Register	Not Supported	Supported

4.4.1 4-Byte Address Commands

The S25FL-L family and S25FL-S family both support commands that always require 4-byte addresses. Table 10 lists all 4-byte commands supported by the S25FL-L family and S25FL-S family.

Table 10. 4-Byte Address Commands

Function	Command	Description	S25FL-L	S25FL-S
Read Flash Array	4READ	Read (4-Byte Address)	13h	13h
	4FAST_READ	Fast Read (4-Byte Address)	0Ch	0Ch
	4DDRFR	DDR Fast Read (4-Byte Address)	–	0Eh[1]
	4DOR	Dual Output Read (4-Byte Address)	3Ch	3Ch
	4QOR	Quad Output Read (4-Byte Address)	6Ch	6Ch
	4DIOR	Dual I/O Read (4-Byte Address)	BCh	BCh
	4QIOR	Quad I/O Read (4-Byte Address)	ECh	ECh
	4DDRDIOR	DDR Dual I/O Read (4-Byte Address)	–	BEh[2]
	4DDRQIOR	DDR Quad I/O Read (4-Byte Address)	EEh	EEh[2]
Program Flash Array	4PP	Page Program (4-Byte Address)	12h	12h

[1] Not Supported by S25FL127S

Function	Command	Description	S25FL-L	S25FL-S
	4QPP	Quad Page Program (4-Byte Address)	34h	34h
Erase Flash Array	4SE	Sector Erase (4-Byte Address)	21h	–
	4P4E	4-KB Parameter Sector Erase (4-Byte Address)	–	21h
	4HBE	Half Block Erase (4-Byte Address)	53h	–
	4BE	Block Erase (4-Byte Address)	DCh	–
	4SE	64-KB or 256-KB Sector Erase (4-Byte Address)	–	DCh
Array Protection	4IBLRD	IBL Read (4-Byte Address)	E0h	–
	4IBL	IBL Lock (4-Byte Address)	E1h	–
	4IBUL	IBL Unlock (4-Byte Address)	E2h	–
	4SPRP	Set Pointer Region Protection (4-Byte Address)	E3h	–
Advanced Sector Protection	DYBRD	DYB Read	–	E0h
	DYBWR	DYB Write	–	E1h
	PPBRD	PPB Read	–	E2h
	PPBP	PPB Program	–	E3h

4.4.2 Extended Address Mode

The S25FL-L family and S25FL-S family both provide a configuration bit that, when enabled, changes all 3-byte address commands to expect a 4-byte address. Most 3-byte address commands are legacy SPI commands. In the S25FL-L family, the Address Length Status (ADS) CR2V[0] bit controls the expected address length for all legacy commands. When the ADS set to '1', legacy commands are changed to require a 4-byte for address field. The 4BEN (B7h) command directory sets this bit to '1' and the 4BEX (E9h) command clears this bit to '0'. In the S25FL-S family, the Extended Address (EXTADD) BAR[7] bit controls the expected address length for all legacy commands. Table 11 lists all the commands requiring 4-byte addressing when the device has the Extended Address Mode enabled.

Table 11. Extended Address Mode with 3-Byte Address Commands

Function	Command	Description	S25FL-L	S25FL-S
Read Device ID	RSFDP	Read JEDEC Serial Flash Discoverable Parameters	5Ah	5Ah[1]
Read Flash Array	READ	Read	03h	03h
	FAST_READ	Fast Read	0Bh	0Bh
	DDRFR	DDR Fast Read	–	0Dh[2]
	DOR	Dual Output Read	3Bh	3Bh
	QOR	Quad Output Read	6Bh	6Bh
	DIOR	Dual I/O Read	BBh	BBh
	QIOR	Quad I/O Read	EBh	EBh
	DDRDIOR	DDR Dual I/O Read	–	BDh[2]
	DDRQIOR	DDR Quad I/O Read	EDh	EDh[2]
Program Flash Array	PP	Page Program	02h	02h
	QPP	Quad Page Program	32h	32h / 38h
Erase Flash Array	SE	Sector Erase	20h	–

[1] S25FL127S only

[2] Not Supported by S25FL127S

Function	Command	Description	S25FL-L	S25FL-S
	P4E	4-KB Parameter Sector Erase	–	20h
	HBE	Half Block Erase	52h	–
	BE	Block Erase	D8h	–
	SE	64-KB or 256 KB Sector Erase	–	D8h
Security Region Array	SECRE	Security Region Erase	44h	–
	SECRP	Security Region Program	42h	–
	SECRR	Security Region Read	48h	–
Array Protection	IBLRD	IBL Read	3Dh	–
	IBL	IBL Lock	36h	–
	IBUL	IBL Unlock	39h	–
	GBL	Global IBL Lock	7Eh	–
	GBUL	Global IBL Unlock	98h	–
	SPRP	Set Pointer Region Protection	FBh	–

4.4.3 Bank Address Register

The S25FL-S family has a Bank Address Register (BAR), which supplies the high-order bits of the address when legacy 3-byte address commands are in use. The S25FL-L family does not support this option.

4.5 QPI Mode

Legacy SPI commands always send the instruction one-bit wide (serial I/O) on the SI (IO0) signal. The S25FL-L family also supports the QPI mode in which all transfers between the host system and memory are four bits wide on IO0 to IO3, including all instructions. The S25FL-S family does not support QPI mode. For details of the QPI mode, refer to the S25FL-L family datasheet.

4.6 Double Data Rate (DDR) Read Commands

The S25FL-L family and the S25FL-S family, except S25FL127S, support Double Data Rate (DDR) commands. The S25FL-S family, except S25FL127S, supports DDR Single I/O, Dual I/O, and Quad I/O read commands but the S25FL-L family only supports the DDR Quad I/O Read command.

4.7 Suspend and Resume

The S25FL-L family and S25FL-S family both support Erase/Program suspend and resume. The S25FL-S family has dedicated suspend and resume commands for each erase and program; however, in the S25FL-L family, common commands are used for erase and program. Table 12 compares the suspend and resume commands.

Table 12. Suspend and Resume Commands

Function	S25FL-L	S25FL-S
Erase Suspend	EPS 75h	ERSP 75h
Program Suspend		PGSP 85h
Erase Resume	EPR 7Ah	ERRS 7Ah
Program Resume		PGRS 8Ah

4.8 Software Reset

The S25FL-L family and S25FL-S family both support Software Reset commands that restore the device to its initial power up state; however, the command code and its impact are different between two device families. For details of the Software Reset, refer to the datasheets.

5 Data Protection

5.1 Security Regions

The S25FL-L family and S25FL-S family both have a 1024-byte address space that is separated from the main Flash array, referred to as the “Security Regions” by the S25FL-L family and the “Secure Silicon Region (OTP)” by the S25FL-S family. Table 13 shows the feature/parameter comparison between the Security Regions and the Secure Silicon Region. The S25FL-L family does not have a Cypress Programmed Random Number in the Security Region, but it has the RUID (4Bh) command that provides a similar functionality.

Table 13. Security Regions Comparison

Feature/Parameter	S25FL-L	S25FL-S
Array Size	1024 Bytes (256 Byte x 4 Regions)	1024 Bytes (32 Byte x 32 Regions)
Read Array Command	SECRR (48h)	OTPR (4Bh)
Program Array Command	SECRP (42h)	OTPP (42h)
Erase Array Command	SECRE (44h)	Not Supported
Password Protection	Supported	Not Supported
Lock Method	LB3, LB2, LB1, LB0 (CR1NV[5:2]) NVLOCK (PR[0])	Lock Bytes in Region 0 FREEZE (CR1[0])
Cypress Programmed Random Number	Not Supported	Programmed in Region 0

5.2 Deep Power Down

The S25FL-L family supports the Deep Power Down (DPD) command that offers an alternative means of data protection. During DPD, the device ignores all commands, except for the Release from Deep Power Down (RES ABh) command and hardware reset. The S25FL-S family does not support this feature.

5.3 Status Register Protect

The S25FL-L family and S25FL-S family both have a legacy status register protection method via bit 7 in the Status Register (SRP0 in the S25FL-L and SRWD in the S25FL-S). The S25FL-L family has an additional SRP1 bit in the Configuration Register 1. The SRP1 adds more flexible and secure functionality to the status register protection.

5.4 Flash Array Protection

The S25FL-L family and S25FL-S family both have some Flash array protection methods. Subsequent sections summarize the similarities and differences of the device families.

5.4.1 Legacy Block Protection

The S25FL-L family and S25FL-S family both have the Legacy Block Protection that can protect an address range of the main Flash array from program and erase operations. The S25FL-L family provides more flexibility for the array protection map by additional Status and Configuration Register bits. Table 14 shows the related Status and Configuration Register bits to the Block Protection method of each device family. Note that in the S25FL-L family, Legacy Block Protection is mutually exclusive with the Individual Block Lock (IBL) protection mechanism. The Write Protect Selection (WPS) bit (CR2V[2]) is used for selecting one of the two protection mechanisms.

Table 14. Block Protection Register Bits

Function	S25FL-L	S25FL-S
Block Protection Bit (BPx)	SR1V[5:2] (S25FL256L) SR1V[4:2] (S25FL128L)	SR1[4:2]
Top or Bottom Protection (TBPROT)	SR1V[6]	TBPROT (CR1[5])
Complement Protection (CMP)	CR1V[6]	-
Sector / Block Protect (SEC)	SR1V[6]	-
Write Protect Selection (WPS)	CR2V[2]	-

5.4.2 Individual and Region Protection (IRP) / Advanced Sector Protection (ASP)

The S25FL-L family and S25FL-S family both have a set of protection methods, referred to as the “Individual and Region Protection (IRP)” by the S25FL-L family and the “Advanced Sector Protection (ASP)” by the S25FL-S family. The IRP and ASP both provide volatile and nonvolatile sector, block, or region protection methods but the actual functionalities are different. Table 15 summarizes a comparison of IRP and ASP features. For details of the IRP and ASP, refer to the datasheets.

Table 15. IRP and ASP Features Comparison

Feature	Parameter	S25FL-L	S25FL-S
Volatile Protection	Feature Name	Individual Block Lock (IBL)	Dynamic Protection Bits (DYB)
	Protection Granularity	Sector or Block	Sector
	Related Commands	IBLRD (3Dh) / 4IBLRD (E0h) IBL (36h) / 4IBL (E1h) IBUL (36h) / 4IBUL (E2h) GBL (7Eh) GBUL (98h)	DYBRD (E0h) DYBWR (E1h)
	Related Register Bits	WPS (CR2V[2]) IBLLBB (IRP[4])	-
Non-volatile Protection	Feature Name	Pointer Region Protection (PRP)	Persistent Protection Bits (PPB)
	Protection Granularity	Sector or Block Region	Sector
	Related Commands	SPRP (FBh) / 4SPRP (E3h) IRPRD (2Bh) IRPP (2Fh) PRRD (A7h) PRL (A6h) PASSRD (E7h) PASSP (E8h) PASSU (Eah)	PPBRD (E2h) PPBP (E3h) PPBE (E4h) PLBRD (A7h) PLBWR (A6h) ASPRD (2Bh) ASPP (2Fh) PASSRD (E7h) PASSP (E8h) PASSU (E9h)
	Related Register Bits	PWDMLB (IRP[2]) PSLMLB (IRP[1]) PERMLB (IRP[0]) NVLOCK (PR[0])	PWDMLB (ASPR[2]) PSTMLB (ASPR[1])

6 Hardware Comparison

6.1 Package Compatibility

Table 16 shows the supported packages in the S25FL-L family and S25FL-S family. S25FL128L does not support 16-pin SOIC (300 mil) and 8-contact WSON (6 x 8 mm) packages, while S25FL128S and/or S25FL127S support them.

Table 16. Package Compatibility

Package Name	256 Mb		128 Mb		
	S25FL256L	S25FL256S	S25FL128L	S25FL128S	S25FL127S
8-pin SOIC (208 mil)			✓		✓
16-pin SOIC (300 mil)	✓	✓		✓	✓
8-Contact WSON (5 × 6 mm)			✓		✓
8-Contact WSON (6 × 8 mm)	✓	✓		✓	
5 x 5 ball FBGA (6 × 8 mm)	✓	✓	✓	✓	✓
4 x 6 ball FBGA (6 × 8 mm)	✓	✓	✓	✓	✓

6.2 Versatile I/O Power Supply (V_{IO})

The S25FL-S family supports the Versatile I/O (V_{IO}) supply that is the voltage source for all device input receivers and output drivers. The S25FL-L family is a single-supply-voltage device that does not support the Versatile I/O (V_{IO}).

6.3 Hold (HOLD#) / IO3

The S25FL-S family supports serial communications hold (stop) through the HOLD# pin. HOLD# is a multiplexed pin; during Quad communication, it becomes IO3. The S25FL-L family does not support the hold functionality; instead, RESET# replaces HOLD# and acts as a hardware reset when CS# is HIGH. RESET# is also multiplexed with IO3 for Quad mode.

6.4 DC Characteristics

Table 17 shows a comparison of the DC parameters for S25FL256/128L and S25FL256/128S in the industrial plus (–40 °C to +105 °C) temperature range. For details and parameters at other temperature ranges, refer to the datasheets.

Table 17. DC Parameters Comparison

Symbol	Parameter Operating (–40 °C to +105 °C)	S25FL256L / S25FL128L			S25FL256S / S25FL128S			Unit
		Min	Typical	Max	Min	Typical	Max	
V_{DD} (min)	V_{DD} (minimum operation voltage)	2.7	–	–	2.7	–	–	V
V_{DD} (cut-off)	V_{DD} (Cut off where reinitialization is needed)	2.4	–	–	2.4	–	–	V
V_{DD} (low)	V_{DD} (low voltage for initialization to occur)	1.0	–	–	1.6	–	–	V
V_{IL}	Input Low Voltage	–0.5	–	0.3 x V_{DD}	–0.5	–	0.2 x V_{IO}	V
V_{IH}	Input High Voltage	0.7 x V_{DD}	–	V_{DD} + 0.4	0.7 x V_{IO}	–	V_{IO} +0.4	V
V_{OL}	Output Low Voltage	–	–	0.2		–	0.15 x V_{IO}	V
V_{OH}	Output High Voltage	V_{DD} – 0.2	–		0.85 x V_{IO}	–		V
I_{LI}	Input Leakage Current	–	–	±4	–	–	±4	µA
I_{LO}	Output Leakage Current	–	–	±4	–	–	±4	µA
I_{CC1}	Active Power Supply Current (READ) – Serial SDR@133 MHz	–	30	40	–	–	35	mA
	Active Power Supply Current (READ) – Quad DDR@66 MHz	–	30	40	–	–	75	mA
I_{CC2}	Active Power Supply Current (Page Program)	–	40	60	–	–	100	mA
I_{CC3}	Active Power Supply Current (WRR or WRAR)	–	40	60	–	–	100	mA
I_{CC4}	Active Power Supply Current (SE)	–	40	60	–	–	100	mA
I_{CC5}	Active Power Supply Current (HBE, BE)	–	40	60	–	–	100	mA
I_{SB}	Standby Current (SPI, DIO, QIO)	–	20	45	–	70	300	µA
	Standby Current (QPI)	–	60	110	–	–	–	µA
I_{DPD}	Deep Power Down Current	–	2	30	–	–	–	µA
I_{POR}	Power On Reset Current	–	15	30	–	–	–	mA

6.5 AC Characteristics

Table 18 and Table 19 show a comparison of the SDR/DDR AC parameters for S25FL256/128L and S25FL256/128S in the industrial plus (–40 °C to +105 °C) temperature range. For details and parameters at other temperature ranges, refer to the datasheets.

Table 18. SDR AC Characteristics Comparison

Symbol	Parameter (–40 °C to +105 °C)	S25FL256L / S25FL128L		S25FL256S / S25FL128S		Unit
		Min	Max	Min	Max	
$F_{SCK, R}$	SCK Clock Frequency for READ and 4READ instructions	–	50	–	50	MHz
$F_{SCK, C}$	SCK Clock Frequency for dual and quad commands	–	133	–	104	MHz
P_{SCK}	SCK Clock Period	1/ F_{SCK}	–	1/ F_{SCK}	–	ns
t_{WH}, t_{CH}	Clock HIGH Time	50% P_{SCK} ±5%	–	45% P_{SCK}	–	ns
t_{WL}, t_{CL}	Clock LOW Time	50% P_{SCK} ±5%	–	45% P_{SCK}	–	V/ns
t_{CRT}, t_{CLCH}	Clock Rise Time (slew rate)	0.1	–	0.1	–	V/ns
t_{CFT}, t_{CHCL}	Clock Fall Time (slew rate)	0.1	–	0.1	–	ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	20	–	10	–	ns
	CS# HIGH Time (All other Non-Read instructions)	50	–	50	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	3	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	5	–	3	3000	ns
t_{SU}	Data in Setup Time	3	–	2	–	ns
t_{HD}	Data in Hold Time	2	–	2	–	ns
t_V	Clock LOW to Output Valid	–	8	–	8	ns
t_{HO}	Output Hold Time	1	–	2	–	ns
t_{DIS}	Output Disable Time	–	8	–	8	ns
t_{WPS}	WP# Setup Time	20	–	20	–	ns
t_{WPH}	WP# Hold Time	100	–	100	–	µs
t_{DP}	CS# HIGH to Deep Power Down Mode	–	3	–	–	µs
t_{RES}	CS# HIGH to Release from Deep Power Down Mode	–	5	–	–	µs
t_{QEN}	QIO or QPI Enter mode,time needed to issue next command	–	1.5	–	–	µs
t_{QEXN}	QIO or QPI Exit mode, time needed to issue next command	–	1	–	–	µs

Table 19. DDR AC Characteristics Comparison

Symbol	Parameter (–40 °C to +105 °C)	S25FL256L / S25FL128L		S25FL256S / S25FL128S		Unit
		Min	Max	Min	Max	
$F_{SCK, R}$	SCK Clock Frequency for DDR READ instructions	–	66	–	80	MHz
$P_{SCK, R}$	SCK Clock Period for DDR READ instruction	1/ F_{SCK}	–	12.5	–	ns
t_{WH}, t_{CH}	Clock HIGH Time	50% P_{SCK} -5%	–	45% P_{SCK}	–	ns
t_{WL}, t_{CL}	Clock LOW Time	50% P_{SCK} -5%	–	45% P_{SCK}	–	V/ns
t_{CRT}	Clock Rise Time (slew rate)	1.5	–	–	–	V/ns
t_{CFT}	Clock Fall Time (slew rate)	1.5	–	–	–	ns
t_{CS}	CS# HIGH Time (Any Read Instructions)	20	–	10	–	ns
	CS# HIGH Time (All other Non-Read instructions)	50	–	-	–	ns
t_{CSS}	CS# Active Setup Time (relative to SCK)	3	–	3	–	ns
t_{CSH}	CS# Active Hold Time (relative to SCK)	–	–	3	–	ns
t_{SU}	Data in Setup Time	3	–	1.5	3000	ns
t_{HD}	Data in Hold Time	2	–	1.5	–	ns
t_V	Clock LOW to Output Valid	–	8	–	6.5	ns
t_{HO}	Output Hold Time	1	–	1.5	–	ns
t_{DIS}	Output Disable Time	–	8	–	8	ns
t_{LZ}	Clock to Output Low Impedance	–	–	0	8	ns
t_{O_skew}	First IO to last IO data valid time	–	600	–	600	ps

6.6 Embedded Algorithms Performance

Table 20 shows a comparison of the program and erase performance for S25FL256/128L and S25FL256/128S. For details of program and Erase performance, refer to the datasheets.

Table 20. Program and Erase Performance Comparison

Symbol	Parameter	S25FL256L / S25FL128L			S25FL256S / S25FL128S			Unit
		Min	Typical	Max	Min	Typical	Max	
t_W	Non-volatile Register Write Time	–	145	750	–	140	500	ms
t_{PP}	Page Programming (256 Bytes)	–	300	1200	–	250	750	µs
t_{BP1}	Byte Programming (First Byte)	–	50	60	–	–	–	µs
t_{BP2}	Additional Byte Programming (After First Byte)	–	6	20	–	–	–	µs
t_{SE}	Sector Erase Time (4-KB physical sectors)	–	50	200	–	130	650	ms
t_{HBE}	Half Block Erase Time (32-KB physical sectors)	–	190	363	–	–	–	ms
t_{BE}	Block Erase Time (64-KB physical sectors)	–	270	725	–	130	650	ms
t_{CE}	Chip Erase Time (256 Mb)	–	140	360	–	66	330	s
	Chip Erase Time (128 Mb)	–	70	180	–	33	165	s

7 Conclusion

The S25FL-L family is serial and multi-I/O command-subset- and footprint-compatible with the S25FL-S family. Migration from the S25FL-S family to the S25FL-L family requires some modifications to accommodate the sector architecture, register set, and data protection methods offered by the S25FL-L family.

8 Related Documents

Table 21. Cypress SPI NOR Flash Product Specific Datasheets

Product Family	Spec Number	Document Title
FL-S Family	001-98283	S25FL128S, S25FL256S 128 Mbit and 256 Mbit 3.0V SPI Flash Memory
	001-98282	S25FL127S 128 Mbit (16 Mbyte) 3.0V SPI Flash Memory
FL-L Family	002-00124	S25FL256L 256 Mbit, S25FL128L 128 Mbit SPI Flash Memory

Document History

Document Title: AN218107 – Migration from S25FL-S to S25FL-L Serial NOR Flash Memory

Document Number: 002-18107

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	5558266	TKUW	12/19/2016	New application note.
*A	5639512	TKUW	06/14/2017	Added Read Latency Added Package Compatibility Updated template

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