OV9650 Color CMOS SXGA (1.3 MegaPixel) CAMERACHIP™ with OmniPixel™ Technology

General Description

The OV9650 CAMERACHIP™ is a low voltage CMOS image sensors that provides the full functionality of a single-chip SXGA (1280x1024) camera and image processor in a small footprint package. The OV9650 provides full-frame, sub-sampled or windowed 8-bit/10-bit images in a wide range of formats, controlled through the Serial Camera Control Bus (SCCB) interface.

This product has an image array capable of operating at up to 15 frames per second (fps) in SXGA resolution with complete user control over image quality, formatting and output data transfer. All required image processing functions, including exposure control, gamma, white balance, color saturation, hue control, white pixel canceling, noise canceling, and more, are also programmable through the SCCB interface. In addition, OmniVision CAMERACHIPS use proprietary sensor technology to improve image quality by reducing or eliminating common lighting/electrical sources of image contamination, such as fixed pattern noise, smearing, etc., to produce a clean, fully stable color image.

Features

- High sensitivity for low-light operation
- Low operating voltage for embedded portable applications
- Standard SCCB interface
- Supports SXGA, VGA, QVGA, QQVGA, CIF, QCIF, QQCIF, and windowed outputs with Raw RGB, RGB (GRB 4:2:2), YUV (4:2:2) and YCbCr (4:2:2) formats
- VarioPixel™ method for sub-sampling formats (VGA, QVGA, QQVGA, CIF, QCIF, and QQCIF)
- Automatic image control functions including: Automatic Exposure Control (AEC), Automatic Gain Control (AGC), Automatic White Balance (AWB), Automatic Band Filter (ABF), and Automatic Black-Level Calibration (ABLC)
- Image quality controls including color saturation, hue, gamma, sharpness (edge enhancement), lens correction, white pixel canceling, noise canceling and 50/60 Hz luminance detection

Ordering Information

Product	Package
OV09650-KL1A (Color)	CSP-28

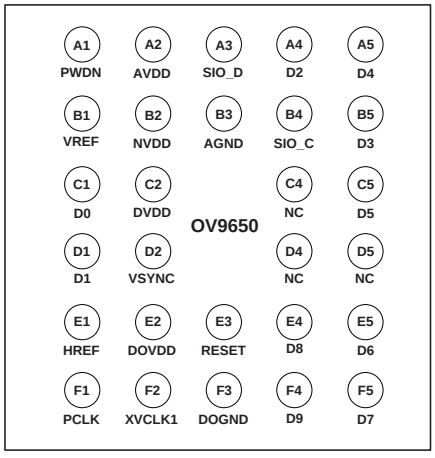
Applications

- Cellular and Picture Phones
- Toys
- PC Multimedia
- Digital Still Cameras

Key Specifications

Active Array Size		1300 x 1028
Power Supply	**Core**	1.8VDC ± 10%
	Analog	2.45 to 2.8 VDC
	I/O	2.5V to 3.3V
Power Requirements	**Active**	50 mW (15 fps, no I/O power)
	Standby	30 µW
Temperature Range	**Operation**	-20°C to 70°C
	Stable Image	0°C to 50°C
Output Formats (8-bit)		• YUV/YCbCr 4:2:2 • GRB 4:2:2 • Raw RGB Data
Lens Size		1/4"
Maximum Image Transfer Rate	**SXGA**	15 fps
	VGA	30 fps
	QVGA, QQVGA, CIF	60 fps
	QCIF, QQCIF	120 fps
Sensitivity		0.9 v/Lux-sec
S/N Ratio		40 dB
Dynamic Range		62 dB
Scan Mode		Progressive
Maximum Exposure Interval		1050 x t_{ROW}
Gamma Correction		Programmable
Pixel Size		3.18 µm x 3.18 µm
Dark Current		30 mV/s at 60°C
Well Capacity		28 K e
Fixed Pattern Noise		<0.03% of $V_{PEAK-TO-PEAK}$
Image Area		4.13 mm x 3.28 mm
Package Dimensions		5095 µm x 5715 µm

Figure 1 OV9650 Pin Diagram



Functional Description

Figure 2 shows the functional block diagram of the OV9650 image sensor. The OV9650 includes:

- Image Sensor Array (1300 x 1028 active image array)
- Analog Signal Processor
- A/D Converters
- Digital Signal Processor (DSP)
- Output Formatter
- Timing Generator
- SCCB Interface
- Digital Video Port

Figure 2 Functional Block Diagram

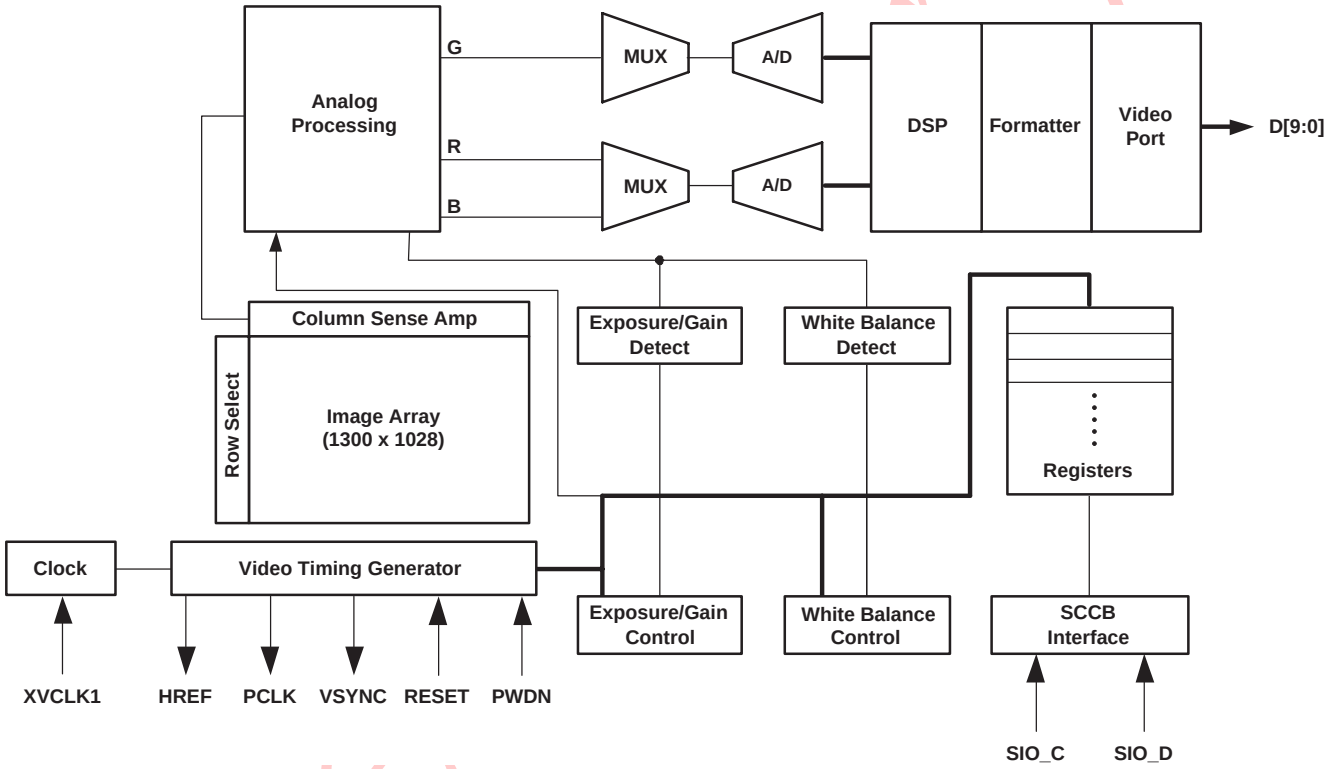
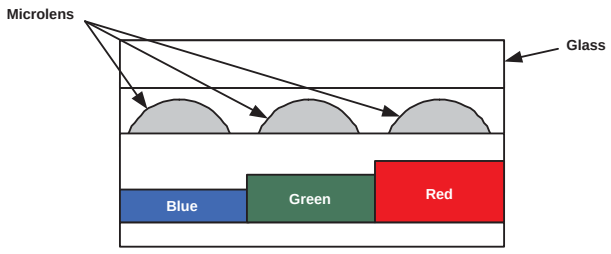


Image Sensor Array

The OV9650 sensor has an active image array of 1300 columns by 1028 rows (1,336,400 pixels). Figure 3 shows a cross-section of the image sensor array.

Figure 3 Image Sensor Array



Timing Generator

In general, the timing generator controls the following functions:

- Array control and frame generation (7 different format outputs)
- Internal timing signal generation and distribution
- Frame rate timing
- Automatic Exposure Control (AEC)
- External timing outputs (VSYNC, HREF/HSYNC, and PCLK)

Analog Signal Processor

This block performs all analog image functions including:

- Automatic Gain Control (AGC)
- Automatic White Balance (AWB)

A/D Converters

After the Analog Processing block, the bayer pattern Raw signal is fed to two 10-bit analog-to-digital (A/D) converters via two multiplexers, one for the G channel and one shared by the BR channels. These A/D converters operate at speeds up to 12 MHz and are fully synchronous to the pixel rate (actual conversion rate is related to the frame rate).

In addition to the A/D conversion, this block also has the following functions:

- Digital Black-Level Calibration (BLC)
- Optional U/V channel delay
- Additional A/D range controls

In general, the combination of the A/D Range Multiplier and A/D Range Control sets the A/D range and maximum value to allow the user to adjust the final image brightness as a function of the individual application.

Digital Signal Processor (DSP)

This block controls the interpolation from Raw data to RGB and some image quality control.

- Edge enhancement (a two-dimensional high pass filter)
- Color space converter (can change Raw data to RGB or YUV/YCbCr)
- RGB matrix to eliminate color cross talk
- Hue and saturation control
- Programmable gamma control
- Transfer 10-bit data to 8-bit
- White pixel canceling
- De-noise

Output Formatter

This block controls all output and data formatting required prior to sending the image out.

Digital Video Port

Register bits COM2[1:0] increase I_{OL}/I_{OH} drive current and can be adjusted as a function of the customer's loading.

SCCB Interface

The Serial Camera Control Bus (SCCB) interface controls the CAMERACHIP operation. Refer to *OmniVision Technologies Serial Camera Control Bus (SCCB) Specification* for detailed usage of the serial control port.

Pin Description

Table 1 Pin Description

Pin Location	Name	Pin Type	Function/Description
A1	PWDN	Function (default = 0)	Power Down Mode Selection - active high, internal pull-down resistor. 0: Normal mode 1: Power down mode
A2	AVDD	Power	Analog power supply (V_{DD-A} = 2.45 to 2.8 VDC)
A3	SIO_D	I/O	SCCB serial interface data I/O
A4	D2	Output	Output bit[2] - LSB for 8-bit YUV or RGB565/RGB555
A5	D4	Output	Output bit[4]
B1	VREF	V_{REF}	Internal voltage reference - connect to ground through 1µF capacitor
B2	NVDD	V_{REF}	Voltage reference
B3	AGND	Power	Analog ground
B4	SIO_C	Input	SCCB serial interface clock input
B5	D3	Output	Output bit[3]
C1	D0	Output	Output bit[0] - LSB for 10-bit Raw RGB data only
C2	DVDD	Power	Power supply (V_{DD-C} = 1.8 VDC ± 10%) for digital core logic
C4	NC	—	No connection
C5	D5	Output	Output bit[5]
D1	D1	Output	Output bit[1] - for 10-bit RGB only
D2	VSYNC	Output	Vertical sync output
D4	NC	—	No connection
D5	NC	—	No connection
E1	HREF	Output	HREF output
E2	DOVDD	Power	Digital power supply (V_{DD-IO} = 2.5 to 3.3 VDC) for I/O
E3	RESET	Function (default = 0)	Clears all registers and resets them to their default values. Active high, internal pull-down resistor.
E4	D8	Output	Output bit[8]
E5	D6	Output	Output bit[6]
F1	PCLK	Output	Pixel clock output
F2	XVCLK1	Input	System clock input
F3	DOGND	Power	Digital ground
F4	D9	Output	Output bit[9] - MSB for 10-bit Raw RGB data and 8-bit YUV or RGB565/RGB555
F5	D7	Output	Output bit[7]

NOTE:

D[9:2] for 8-bit YUV or RGB565/RGB555 (D[9] MSB, D[2] LSB)

D[9:0] for 10-bit Raw RGB data (D[9] MSB, D[0] LSB)

Electrical Characteristics

Table 2 Absolute Maximum Ratings

Ambient Storage Temperature		-40ºC to +95ºC
Supply Voltages (with respect to Ground)	**V_{DD-A}**	4.5 V
	V_{DD-C}	3 V
	V_{DD-IO}	4.5 V
All Input/Output Voltages (with respect to Ground)		-0.3V to V_{DD-IO}+1V
Lead-free Temperature, Surface-mount process		245ºC
ESD Rating, Human Body model		2000V

NOTE: Exceeding the Absolute Maximum ratings shown above invalidates all AC and DC electrical specifications and may result in permanent device damage.

Table 3 DC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DD-A}	DC supply voltage – Analog	–	2.45	2.5	2.8	V
V_{DD-C}	DC supply voltage – Core	–	1.62	1.8	1.98	V
V_{DD-IO}	DC supply voltage – I/O power	–	2.25	–	3.6	V
I_{DDA}	Active (Operating) Current	See Note [a]		20		mA
$I_{DDS-SCCB}$	Standby Current	See Note [b]		1		mA
$I_{DDS-PWDN}$	Standby Current			10		µA
V_{IH}	Input voltage HIGH	CMOS	0.7 x V_{DD-IO}			V
V_{IL}	Input voltage LOW				0.3 x V_{DD-IO}	V
V_{OH}	Output voltage HIGH	CMOS	0.9 x V_{DD-IO}			V
V_{OL}	Output voltage LOW				0.1 x V_{DD-IO}	V
I_{OH}	Output current HIGH	See Note [c]	8			mA
I_{OL}	Output current LOW		15			mA
I_L	Input/Output Leakage	GND to V_{DD-IO}			± 1	µA

a. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.0V
$I_{DDA} = \Sigma\{I_{DD-IO} + I_{DD-C} + I_{DD-A}\}$, f_{CLK} = 24MHz at 7.5 fps YUV output, no I/O loading

b. V_{DD-A} = 2.5V, V_{DD-C} = 1.8V, V_{DD-IO} = 3.0V
$I_{DDS:SCCB}$ refers to a SCCB-initiated Standby, while $I_{DDS:PWDN}$ refers to a PWDN pin-initiated Standby

c. Standard Output Loading = 25pF, 1.2KΩ

Table 4 Functional and AC Characteristics (-20°C < T_A < 70°C)

Symbol	Parameter	Min	Typ	Max	Unit
Functional Characteristics					
	A/D Differential Non-Linearity		± 1/2		LSB
	A/D Integral Non-Linearity		± 1		LSB
	AGC Range			18	dB
	Red/Blue Adjustment Range		12		dB
Inputs (PWDN, CLK, RESET)					
f_{CLK}	Input Clock Frequency	10	24	48	MHz
t_{CLK}	Input Clock Period	21	42	100	ns
$t_{CLK:DC}$	Clock Duty Cycle	45	50	55	%
$t_{S:RESET}$	Setting time after software/hardware reset			1	ms
$t_{S:REG}$	Settling time for register change (10 frames required)			300	ms
SCCB Timing (see Figure 4)					
f_{SIO_C}	Clock Frequency			400	KHz
t_{LOW}	Clock Low Period	1.3			µs
t_{HIGH}	Clock High Period	600			ns
t_{AA}	SIO_C low to Data Out valid	100		900	ns
t_{BUF}	Bus free time before new START	1.3			µs
$t_{HD:STA}$	START condition Hold time	600			ns
$t_{SU:STA}$	START condition Setup time	600			ns
$t_{HD:DAT}$	Data-in Hold time	0			µs
$t_{SU:DAT}$	Data-in Setup time	100			ns
$t_{SU:STO}$	STOP condition Setup time	600			ns
t_R, t_F	SCCB Rise/Fall times			300	ns
t_{DH}	Data-out Hold time	50			ns
Outputs (VSYNC, HREF, PCLK, and D[9:0] (see Figure 5, Figure 6, Figure 7, Figure 8, Figure 10, and Figure 11)					
t_{PDV}	PCLK[↓] to Data-out Valid			5	ns
t_{SU}	D[9:0] Setup time	15			ns
t_{HD}	D[9:0] Hold time	8			ns
t_{PHH}	PCLK[↓] to HREF[↑]	0		5	ns
t_{PHL}	PCLK[↓] to HREF[↓]	0		5	ns
AC Conditions:	• V_{DD}: V_{DD-C} = 1.8V, V_{DD-A} = 2.5V, V_{DD-IO} = 3.0V • Rise/Fall Times: I/O: 5ns, Maximum SCCB: 300ns, Maximum • Input Capacitance: 10pf • Output Loading: 25pF, 1.2KΩ to 3V • f_{CLK}: 24MHz				

Timing Specifications

Figure 4 SCCB Timing Diagram

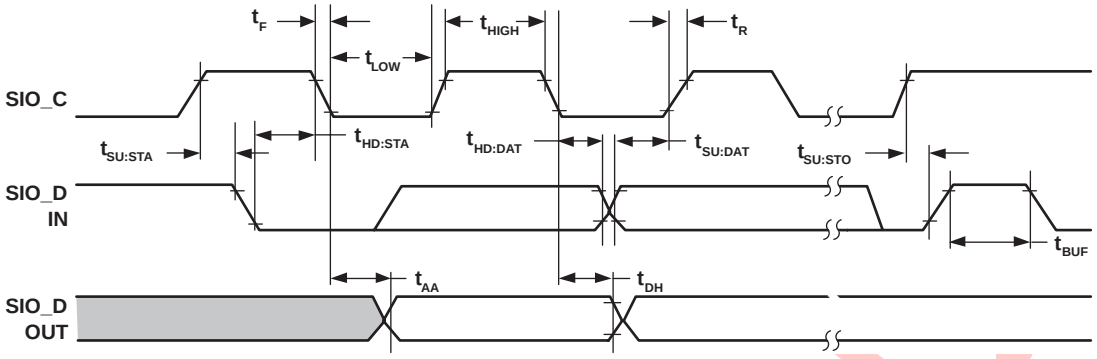


Figure 5 Horizontal Timing

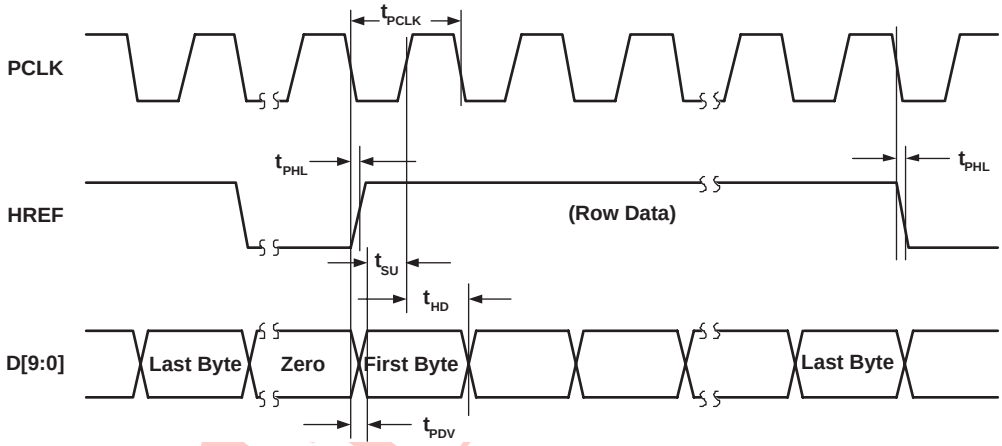
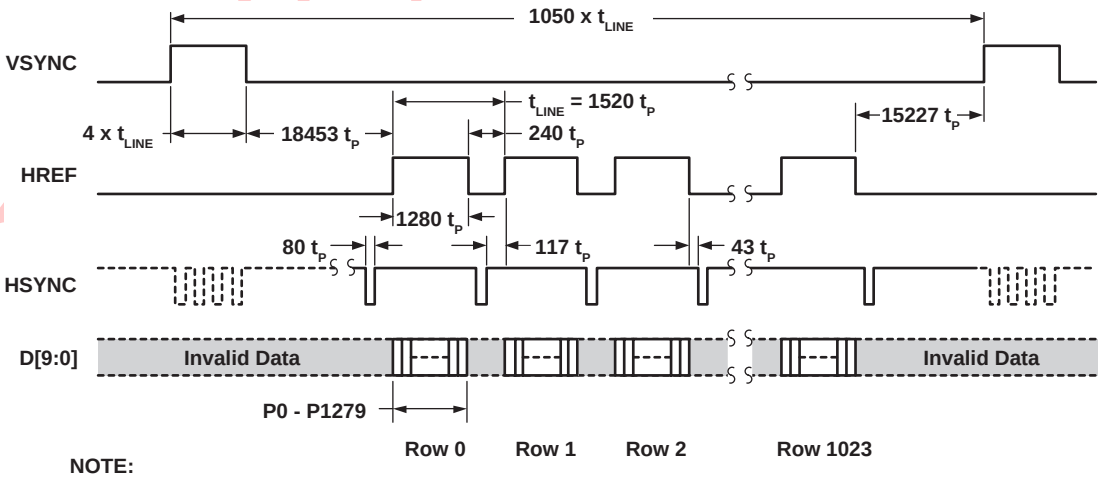
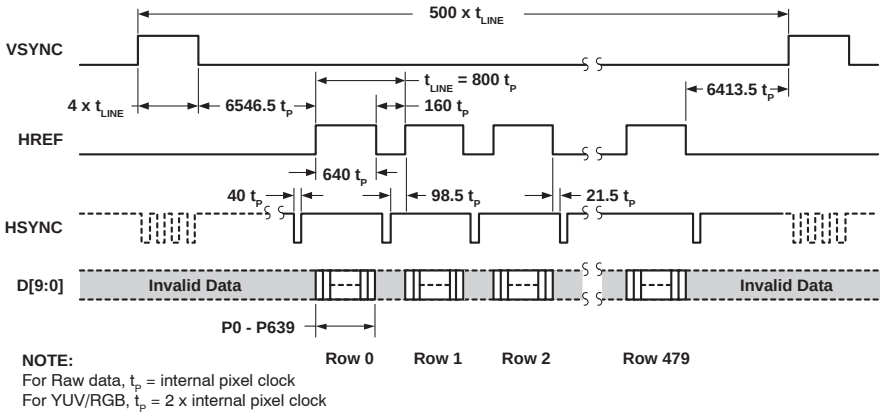


Figure 6 SXGA Frame Timing



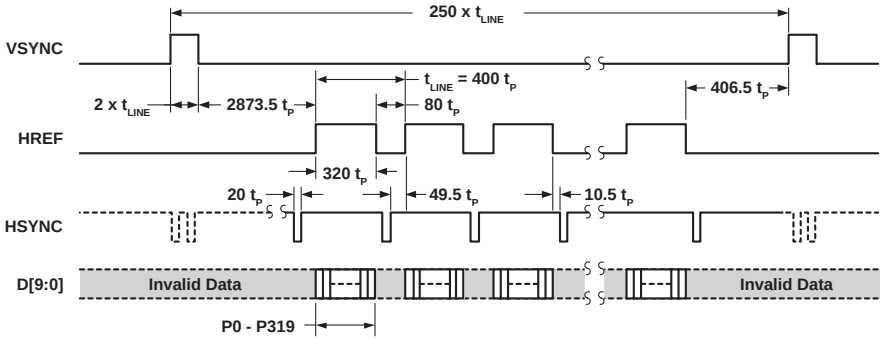
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 7 VGA Frame Timing



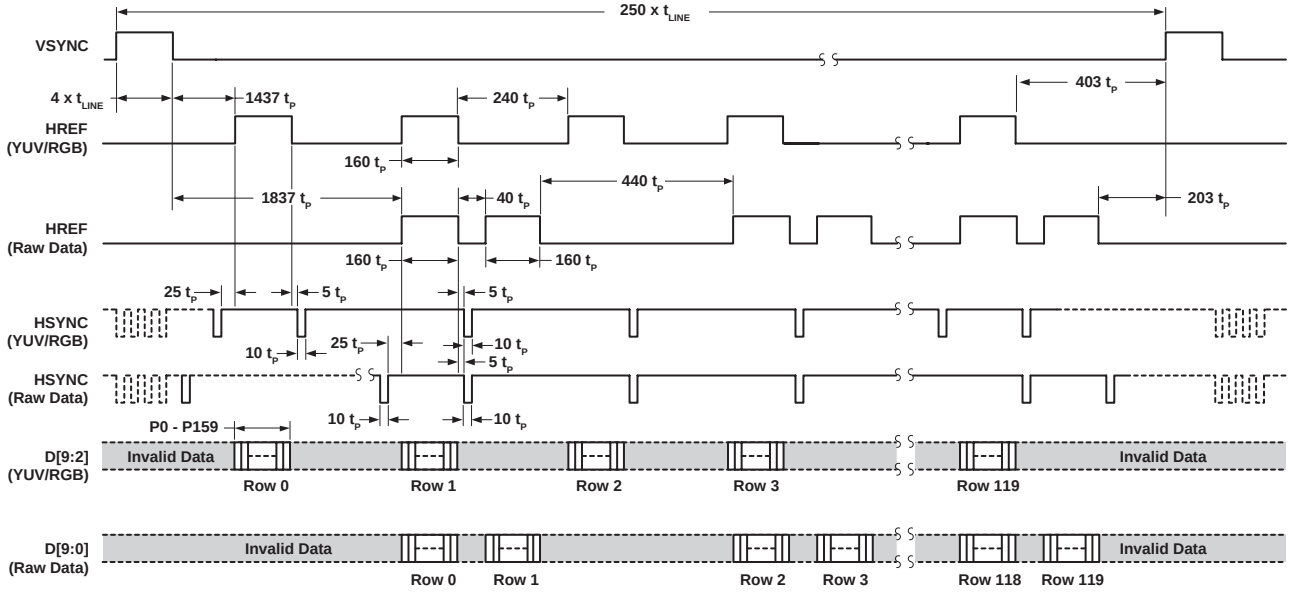
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 8 QVGA Frame Timing



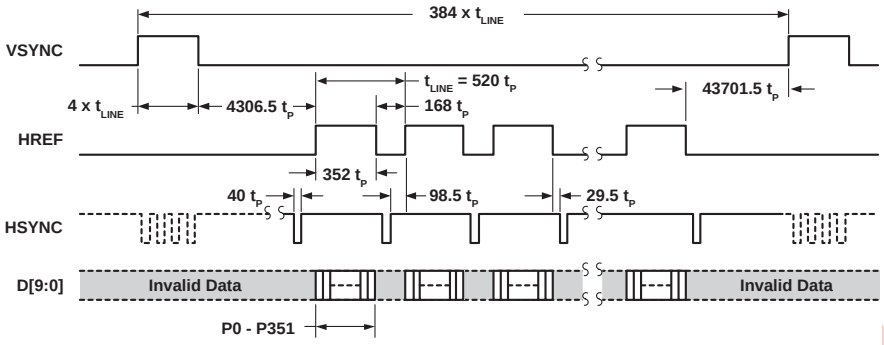
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 9 QQVGA Frame Timing



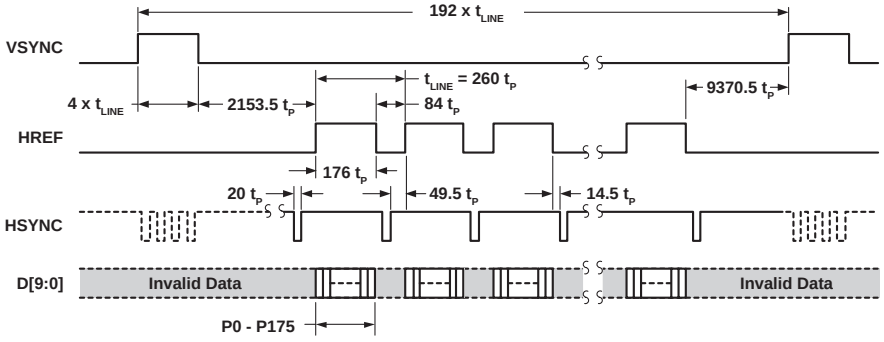
NOTE:
For YUV/RGB, $t_P = 2 \times t_{PCLK}$
For Raw data, $t_P = t_{PCLK}$

Figure 10 CIF Frame Timing



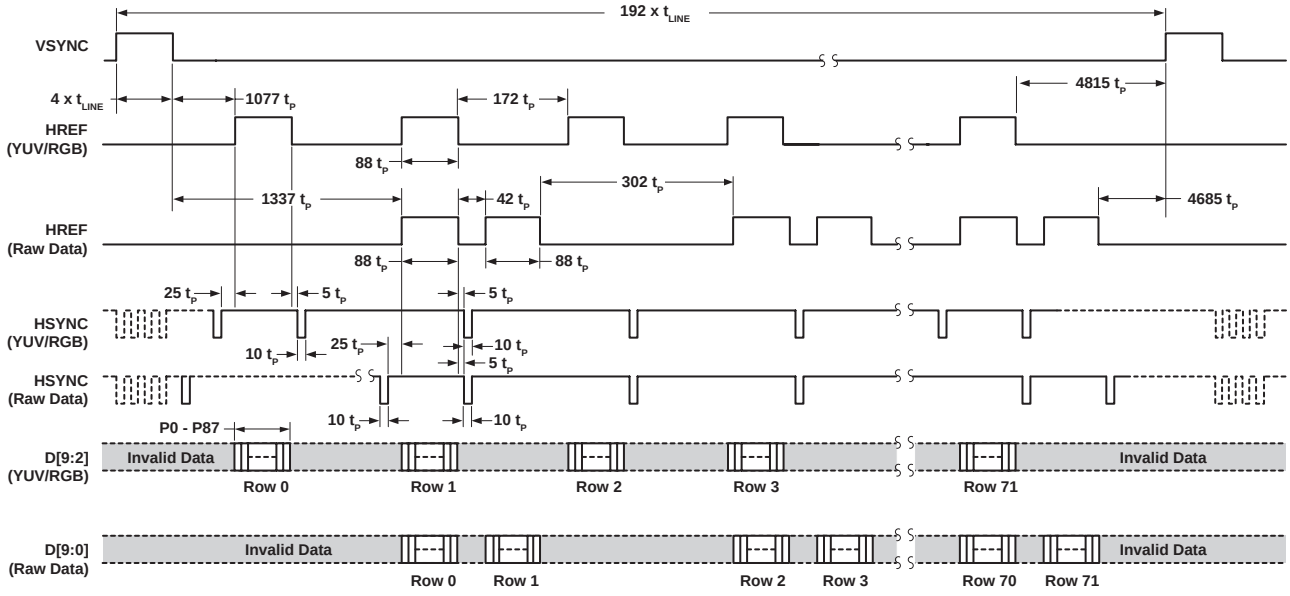
NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x internal pixel clock

Figure 11 QCIF Frame Timing



NOTE:
For Raw data, t_P = internal pixel clock
For YUV/RGB, t_P = 2 x Internal pixel clock

Figure 12 QQCIF Frame Timing



NOTE:
For YUV/RGB, $t_P = 2 \times t_{PCLK}$
For Raw data, $t_P = t_{PCLK}$

Figure 13 RGB 565 Output Timing Diagram

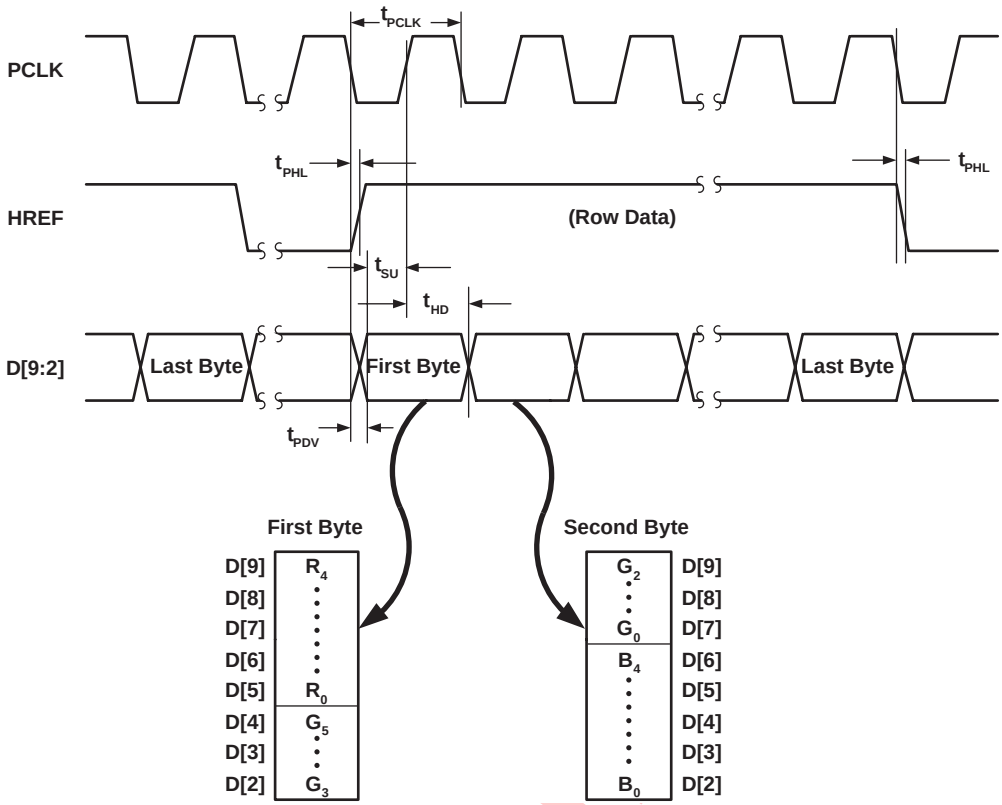
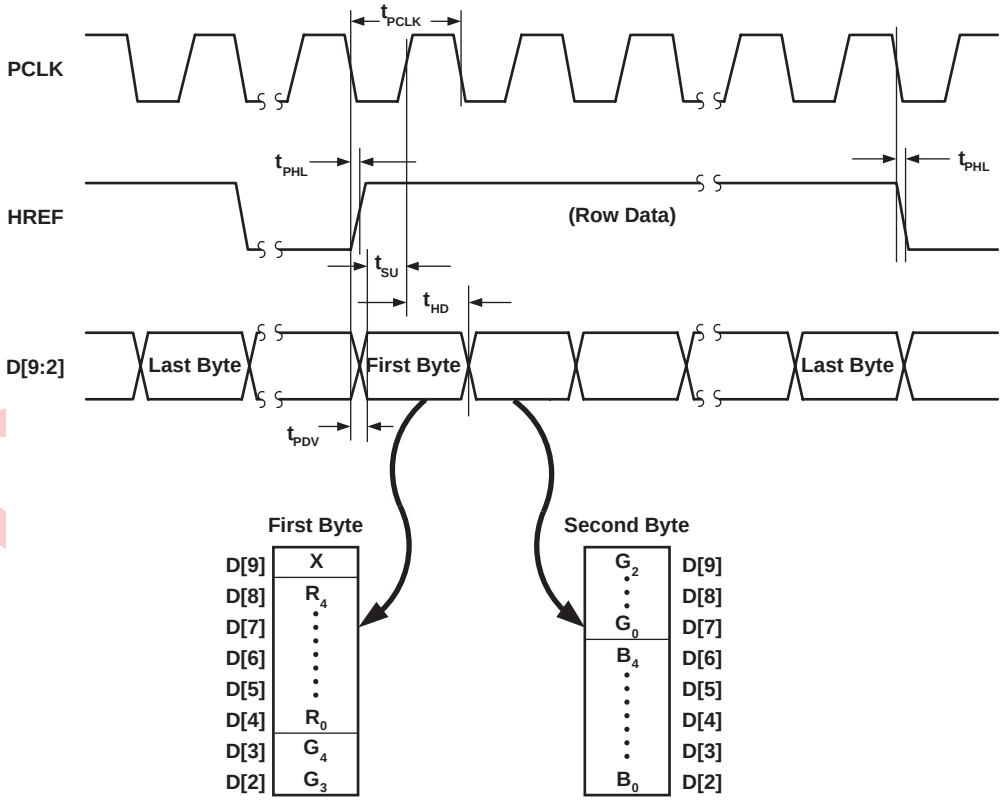
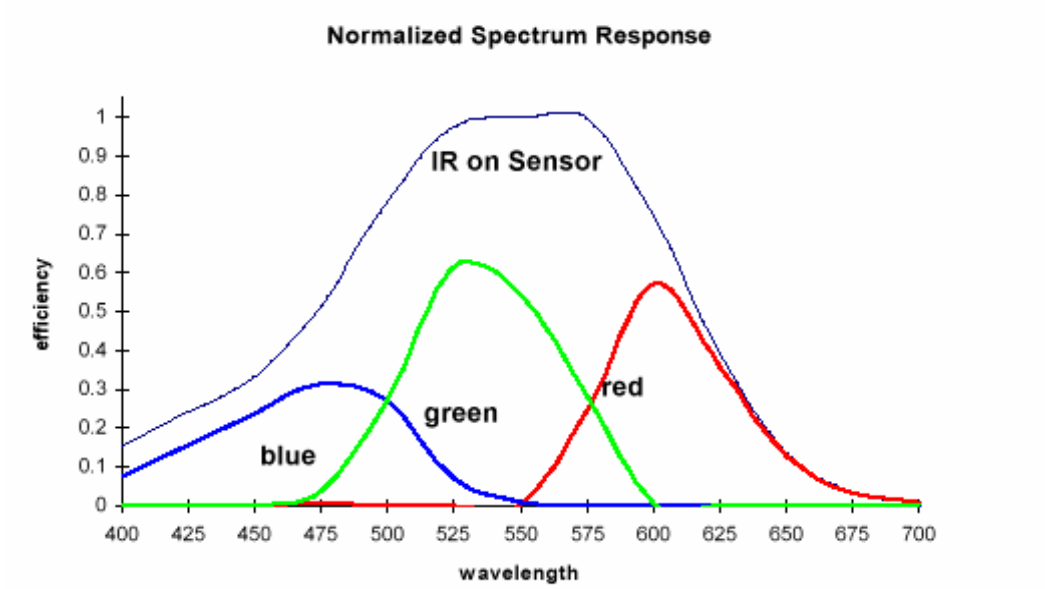


Figure 14 RGB 555 Output Timing Diagram



OV9650 Light Response

Figure 15 OV9650 Light Response



Register Set

Table 5 provides a list and description of the Device Control registers contained in the OV9650. For all register Enable/Disable bits, ENABLE = 1 and DISABLE = 0. The device slave addresses are 60 for write and 61 for read.

Table 5 Device Control Register List

Address (Hex)	Register Name	Default (Hex)	R/W	Description
00	GAIN	00	RW	AGC[7:0] – Gain control gain setting • Range: [00] to [FF]
01	BLUE	80	RW	AWB – Blue channel gain setting • Range: [00] to [FF]
02	RED	80	RW	AWB – Red channel gain setting • Range: [00] to [FF]
03	VREF	12	RW	Vertical Frame Control Bit[7:6]: AGC[9:8] (see register GAIN for AGC[7:0]) Bit[5:3]: VREF end low 3 bits (high 8 bits at VSTOP[7:0] Bit[2:0]: VREF start low 3 bits (high 8 bits at VSTRT[7:0]
04	COM1	00	RW	Common Control 1 Bit[7]: Reserved Bit[6]: CCIR656 format Bit[5]: QQVGA or QQCIF format. Effective only when QVGA or QCIF output is selected (register bit COM7[4]) and related HREF skip mode based on format is selected (register COM1[3:2]) Bit[4]: Reserved Bit[3:2]: HREF skip option 00: No skip 01: YUV/RGB skip every other row for YUV/RGB, skip 2 rows for every 4 rows for Raw data 1x: Skip 3 rows for every 4 rows for YUV/RGB, skip 6 rows for every 8 rows for Raw data Bit[1:0]: AEC low 2 LSB (see registers AECHM for AEC[15:10] and AECH for AEC[9:2])
05	BAVE	00	RW	U/B Average Level Automatically updated based on chip output format
06	GEAVE	00	RW	Y/Ge Average Level Automatically updated based on chip output format
07	RSVD	00	–	Reserved
08	RAVE	00	RW	V/R Average Level Automatically updated based on chip output format

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
09	COM2	01	RW	Common Control 2 Bit[7:5]: Reserved Bit[4]: Soft sleep mode Bit[3:2]: Reserved Bit[1:0]: Output drive capability 00: 1x 01: 2x 10: 2x 11: 4x
0A	PID	96	R	Product ID Number MSB (Read only)
0B	VER	50	R	Product ID Number LSB (Read only)
0C	COM3	00	RW	Common Control 3 Bit[7]: Reserved Bit[6]: Output data MSB and LSB swap Bit[5:4]: Reserved Bit[3]: Pin selection 1: Change RESET pin to EXPST_B (frame exposure mode timing) and change PWDN pin to FREX (frame exposure enable) Bit[2]: VarioPixel for VGA and CIF Bit[1]: Reserved Bit[0]: Single frame output (used for Frame Exposure mode only)
0D	COM4	00	RW	Common Control 4 Bit[7]: VarioPixel for QVGA, QCIF, QQVGA, and QQCIF Bit[6]: Reserved Bit[5]: Pixels for sub-sampling mode 0: Get average neighbor pixel in sub-sampling mode 1: Get sum instead of average neghbor pixel in sub-sampling mode Bit[4:3]: Reserved Bit[2]: Tri-state option for output clock at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[1]: Tri-state option for output data at power-down period 0: Tri-state at this period 1: No tri-state at this period Bit[0]: Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
0E	COM5	01	RW	Common Control 5 Bit[7]: System clock selection. If the system clock is 48 MHz, this bit should be set to high to get 15 fps for YUV or RGB Bit[6:5]: Reserved Bit[4]: Slam mode enable 0: Master mode 1: Slam mode (used for slave mode) Bit[3]: ADC offset manual control 0: Offset is controlled automatically 1: Register OFON[7:4] can enable ADC offset addition Bit[2:1]: Reserved Bit[0]: Exposure step can be set longer than VSYNC time 1: In Normal mode, AEC changes by 1/16 and in Fast mode, AEC changes by double
0F	COM6	43	RW	Common Control 6 Bit[7]: Output of optical black line option 0: Disable HREF at optical black 1: Enable HREF at optical black Bit[6:5]: Reserved Bit[4]: HREF is high from optical black line Bit[3]: Enable bias for ADBLC Bit[2]: ADBLC offset 0: Use 4-channel ADBLC 1: Use 2-channel ADBLC Bit[1]: Reset all timing when format changes Bit[0]: Enable ADBLC option
10	AECH	40	RW	Exposure Value Bit[7:0]: AEC[9:2] (see registers AECHM for AEC[15:10] and COM1 for AEC[1:0])
11	CLKRC	00	RW	Data Format and Internal Clock Bit[7]: Digital PLL option 0: Disable double clock option, meaning the maximum PCLK can be as high as half input clock 1: Enable double clock option, meaning the maximum PCLK can be as high as input clock Bit[6]: Use external clock directly (no clock pre-scale available) Bit[5:0]: Internal clock pre-scalar F(internal clock) = F(input clock)/(Bit[5:0]+1) • Range: [0 0000] to [1 1111]

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
12	COM7	00	RW	Common Control 7 Bit[7]: SCCB Register Reset 0: No change 1: Resets all registers to default values Bit[6]: Output format - VGA selection Bit[5]: Output format - CIF selection Bit[4]: Output format - QVGA selection Bit[3]: Output format - QCIF selection Bit[2]: Output format - RGB selection Bit[1]: Reserved Bit[0]: Output format - Raw RGB (COM7[2] must be set high)
13	COM8	8F	RW	Common Control 8 Bit[7]: Enable fast AGC/AEC algorithm Bit[6]: AEC - Step size limit (used only in fast condition and COM5[0] is low) 0: Fast condition change maximum step is VSYNC 1: Unlimited step size Bit[5]: Banding filter ON/OFF Bit[4]: Reserved Bit[3]: Enable AEC time can be less than 1 line option Bit[2]: AGC Enable Bit[1]: AWB Enable Bit[0]: AEC Enable
14	COM9	4A	RW	Common Control 9 Bit[7]: Reserved Bit[6:4]: Automatic Gain Ceiling - maximum AGC value 000: 2x 001: 4x 010: 8x 011: 16x 100: 32x 101: 64x 110: 128x Bit[3]: Exposure timing can be less than limit of banding filter when light is too strong Bit[2]: Data format - VSYNC drop option 0: VSYNC always exists 1: VSYNC will drop when frame data drops Bit[1]: Enable drop frame when AEC step is larger than VSYNC Bit[0]: Freeze AGC/AEC

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
15	COM10	00	RW	Common Control 10 Bit[7]: Set pin definition 1: Set RESET to SLHS (slave mode horizontal sync) and set PWDN to SLVS (slave mode vertical sync) Bit[6]: HREF changes to HSYNC Bit[5]: PCLK output option 0: PCLK always output 1: No PCLK output when HREF is low Bit[4]: PCLK reverse Bit[3]: HREF reverse Bit[2]: Reset signal end point option Bit[1]: VSYNC negative Bit[0]: HSYNC negative
16	RSVD	00	–	Reserved
17	HSTART	1A	RW	Output Format - Horizontal Frame (HREF column) start high 8-bit (low 3 bits are at HREF[2:0])
18	HSTOP	BA	RW	Output Format - Horizontal Frame (HREF column) end high 8-bit (low 3 bits are at HREF[5:3])
19	VSTRT	01	RW	Output Format - Vertical Frame (row) start high 8-bit (low 2 bits are at VREF[1:0])
1A	VSTOP	81	RW	Output Format - Vertical Frame (row) end high 8-bit (low 2 bits are at VREF[3:2])
1B	PSHFT	00	RW	Data Format - Pixel Delay Select (delays timing of the D[9:0] data relative to HREF in pixel units) • Range: [00] (no delay) to [FF] (256 pixel delay which accounts for whole array)
1C	MIDH	7F	R	Manufacturer ID Byte – High (Read only = 0x7F)
1D	MIDL	A2	R	Manufacturer ID Byte – Low (Read only = 0xA2)
1E	MVFP	00	RW	Mirror/VFlip Enable Bit[7:6]: Reserved Bit[5]: Mirror 0: Normal image 1: Mirror image Bit[4]: VFlip enable 0: VFlip disable 1: VFlip enable Bit[3:0]: Reserved
1F	LAEC	00	RW	Reserved
20	BOS	80	RW	B Channel ADBLC Result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range (high 7 bits)

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
21	GBOS	80	RW	Gb channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
22	GROS	80	RW	Gr channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
23	ROS	80	RW	R channel ADBLC result Bit[7]: Offset adjustment sign 0: Add offset 1: Subtract offset Bit[6:0]: Offset value of 10-bit range
24	AEW	78	RW	AGC/AEC - Stable Operating Region (Upper Limit)
25	AEB	68	RW	AGC/AEC - Stable Operating Region (Lower Limit)
26	VPT	D4	RW	AGC/AEC Fast Mode Operating Region Bit[7:4]: Upper limit of 4 MSB Bit[3:0]: Lower limit of 4 LSB
27	BBIAS	80	RW	B Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
28	GbBIAS	80	RW	Gb Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
29	Gr_COM	00	RW	Analog BLC and Regulator Control Bit[7:6]: Reserved Bit[5]: Bypass Analog BLC Bit[4]: Bypass regulator Bit[3:0]: Reserved
2A	EXHCH	00	RW	Dummy Pixel Insert MSB Bit[7:4]: 4 MSB for dummy pixel insert in horizontal direction Bit[3:2]: HSYNC falling edge delay 2 MSB Bit[1:0]: HSYNC rising edge delay 2 MSB
2B	EXHCL	00	RW	Dummy Pixel Insert LSB 8 LSB for dummy pixel insert in horizontal direction

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
2C	RBIAS	80	RW	R Channel Signal Output Bias (effective only when COM6[0] = 1) Bit[7]: Bias adjustment sign 0: Add bias 1: Subtract bias Bit[6:0]: Bias value of 10-bit range
2D	ADVFL	00	RW	LSB of insert dummy lines in vertical direction (1 bit equals 1 line)
2E	ADVFH	00	RW	MSB of insert dummy lines in vertical direction
2F	YAVE	00	RW	Y/G Channel Average Value
30	HSYST	08	RW	HSYNC Rising Edge Delay (low 8 bits)
31	HSYEN	30	RW	HSYNC Falling Edge Delay (low 8 bits)
32	HREF	A4	RW	HREF Control Bit[7:6]: HREF edge offset to data output Bit[5:3]: HREF end 3 LSB (high 8 MSB at register HSTOP) Bit[2:0]: HREF start 3 LSB (high 8 MSB at register HSTART)
33	CHLF	00	RW	Bit[7:0]: Reserved
34	ARBLM	03	RW	Bit[7:0]: Reserved
35-36	RSVD	XX	–	Reserved
37	ADC	04	RW	Bit[7:0]: Reserved
38	ACOM	12	RW	Bit[7:0]: Reserved
39	OFON	00	RW	Bit[7:4]: Reserved Bit[3]: Line buffer power down - must be set to "1" before chip power down Bit[2:0]: Reserved
3A	TSLB	0C	RW	Line Buffer Test Option Bit[7:6]: Reserved Bit[5]: Bit-wise reverse Bit[4]: UV output value 0: Use normal UV output 1: Use fixed UV value set in registers MANU and MANV as UV output instead of chip output Bit[3]: Output sequence is Y U Y V instead of U Y V Y Bit[2]: Output sequence is Y V Y U instead of Y U Y V Bit[1]: Reserved Bit[0]: Digital BLC

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3B	COM11	00	RW	Common Control 11 Bit[7]: Night mode 0: Night mode disable 1: Frame rate will adjust based on COM11[6:5] before AGC gain increases more than 2. Also, ADVFL and ADVFL will be automatically updated. Bit[6:5]: Night mode insert frame option 00: Normal frame rate 01: 1/2 frame rate 10: 1/4 frame rate 11: 1/8 frame rate Bit[4:3]: Average calculation window option 00: Use full frame 01: Use half frame 10: Use quarter frame 11: Use lower two-thirds Bit[2:1]: Reserved Bit[0]: Manual banding filter mode
3C	COM12	40	RW	Common Control 12 Bit[7]: HREF option 0: No HREF when VREF is low 1: Always has HREF Bit[6:3]: Reserved Bit[2]: Enable YUV average Bit[1:0]: Reserved
3D	COM13	99	RW	Common Control 13 Bit[7:6]: Gamma selection for signal 00: No gamma function 01: Gamma used for Y channel only 10: Gamma used for Raw data before interpolation 11: Not allowed Bit[5]: Reserved Bit[4]: Enable color matrix for RGB or YUV Bit[3]: Enable Y channel delay option 0: Delay UV channel 1: Delay Y channel Bit[2:0]: Output Y/UV delay
3E	COM14	0E	RW	Common Control 14 Bit[7:2]: Reserved Bit[1]: Enable edge enhancement for YUV output (effective only for YUV/RGB, no use for Raw data) Bit[0]: Edge enhancement option 0: Edge enhancement factor = EDGE[3:0] 1: Edge enhancement factor = 2 x EDGE[3:0]

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
3F	EDGE	88	RW	Edge Enhancement Adjustment Bit[7:4]: Edge enhancement threshold[3:0] (see register COM22[7:6} for Edge threshold[5:4]) Bit[3:0]: Edge enhancement factor
40	COM15	C0	RW	Common Control 15 Bit[7:6]: Data format - output full range enable 0x: Output range: [10] to [F0] 10: Output range: [01] to [FE] 11: Output range: [00] to [FF] Bit[5:4]: RGB 555/565 option (must set COM7[2] high) x0: Normal RGB output 01: RGB 565 11: RGB 555 Bit[3]: Swap R/B in RGB565/RGB555 format Bit[2:0]: Reserved
41	COM16	10	RW	Common Control 16 Bit[7:2]: Reserved Bit[1]: Color matrix coefficient double option Bit[0]: Reserved
42	COM17	08	RW	Common Control 17 Bit[7:5]: Reserved Bit[4]: Edge enhancement option Bit[3]: Reserved Bit[2]: Select single frame out Bit[1]: Tri-state output Bit[0]: Reserved
43-4E	RSVD	XX	–	Reserved
4F	MTX1	58	RW	Matrix Coefficient 1
50	MTX2	48	RW	Matrix Coefficient 2
51	MTX3	10	RW	Matrix Coefficient 3
52	MTX4	28	RW	Matrix Coefficient 4
53	MTX5	48	RW	Matrix Coefficient 5
54	MTX6	70	RW	Matrix Coefficient 6
55	MTX7	40	RW	Matrix Coefficient 7
56	MTX8	40	RW	Matrix Coefficient 8
57	MTX9	40	RW	Matrix Coefficient 9
58	MTXS	0F	RW	Matrix Coefficient Sign for coefficient 9 to 2 0: Plus 1: Minus
59-61	RSVD	XX	–	Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
62	LCC1	00	RW	Lens Correction Option 1
63	LCC2	00	RW	Lens Correction Option 2
64	LCC3	10	RW	Lens Correction Option 3
65	LCC4	80	RW	Lens Correction Option 4
66	LCC5	00	RW	Lens Correction Control
67	MANU	80	RW	Manual U Value (effective only when register TSLB[4] is high)
68	MANV	80	RW	Manual V Value (effective only when register TSLB[4] is high)
69	HV	00	RW	Manual Banding Filter MSB Bit[7:1]: Reserved Bit[0]: Matrix coefficient 1 sign
6A	MBD	00	RW	LSB of Banding Filter Value (effective only when COM11[0] is high).
6B	DBLV	0A	RW	Bit[7:0]: Reserved
6C-7B	GSP	XX	RW	Gamma curve
7C-8A	GST	XX	RW	Gamma curve
8B	COM21	04	RW	Common Control 21 Bit[7:4]: Reserved Bit[3]: VGA option - use VGA window mode Bit[2]: Reserved Bit[1]: Digital BLC option Bit[0]: UV channel uses sum or average of neighbor pixel in sub-sampling mode
8C	COM22	00	RW	Common Control 22 Bit[7:6]: Edge enhancement threshold[5:4] (see register EDGE[7:4} for Edge threshold[3:0]) Bit[5]: De-noise enable Bit[4:2]: Reserved Bit[1]: White-pixel erase enable Bit[0]: White-pixel erase option
8D	COM23	00	RW	Common Control 23 Bit[7:5]: Reserved Bit[4]: Color bar test mode Bit[3:2]: Reserved Bit[1]: Digital AWB enable Bit[0]: Reserved
8E	COM24	00	RW	Common Control 24 Bit[7:0]: Reserved

Table 5 Device Control Register List (Continued)

Address (Hex)	Register Name	Default (Hex)	R/W	Description
8F	DBLC1	0F	RW	Digital BLC Offset Sign Bit[7:4]: Reserved Bit[3]: Digital BLC B offset sign Bit[2]: Digital BLC R offset sign Bit[1]: Digital BLC Gb offset sign Bit[0]: Digital BLC Gr offset sign
90	DBLC_B	00	RW	Digital BLC B Channel Offset Value Bit[7:0]: Digital BLC B channel offset value
91	DBLC_R	00	RW	Digital BLC R Channel Offset Value Bit[7:0]: Digital BLC R channel offset value
92	DM_LNL	00	RW	Dummy Line low 8 bits Bit[7:0]: Control insert Dummy line[7:0]
93	DM_LNH	00	RW	Dummy Line high 8 bits Bit[7:0]: Control insert Dummy line[15:8]
94-9C	RSVD	XX	–	Reserved
9D	LCCFB	00	RW	Lens Correction B Channel Control
9E	LCCFR	00	RW	Lens Correction R Channel Control
9F	DBLC_Gb	00	RW	Digital BLC Gb Channel Offset Value Bit[7:0]: Digital BLC Gb channel offset value
A0	DBLC_Gr	00	RW	Digital BLC Gr Channel Offset Value Bit[7:0]: Digital BLC Gr channel offset value
A1	AECHM	40	RW	Exposure Value - AEC MSB 5 bits Bit[7:6]: Reserved Bit[5:0]: AEC[15:10] (see registers AECH for AEC[9:2] and COM1 for AEC[1:0])
A2-A3	RSVD	XX	–	Reserved
A4	COM25	00	RW	Common Control 25 Bit[7:0]: Reserved
A5	COM26	00	RW	Common Control 26 Bit[7:0]: Reserved
A6	G_GAIN	80	RW	Green Gain Option Bit[7:0]: Green gain when using digital AWB
A7	VGA_ST	14	RW	Vertical Start Point for VGA Bit[7:0]: Define vertical start point in VGA sub-windowing mode
A8-AA	ACOM	XX	–	Reserved
NOTE: All other registers are factory-reserved. Please contact OmniVision Technologies for reference register settings.				

Package Specifications

The OV9650 uses a 28-pin Chip Scale Package (CSP). Refer to Figure 16 for package information, Table 6 for package dimensions and Figure 17 for the array center on the chip.

Note: For OVT devices that contain lead, all part marking letters are upper case. For OVT devices that are lead-free, all part marking letters are lower case

Figure 16 OV9650 Package Specifications

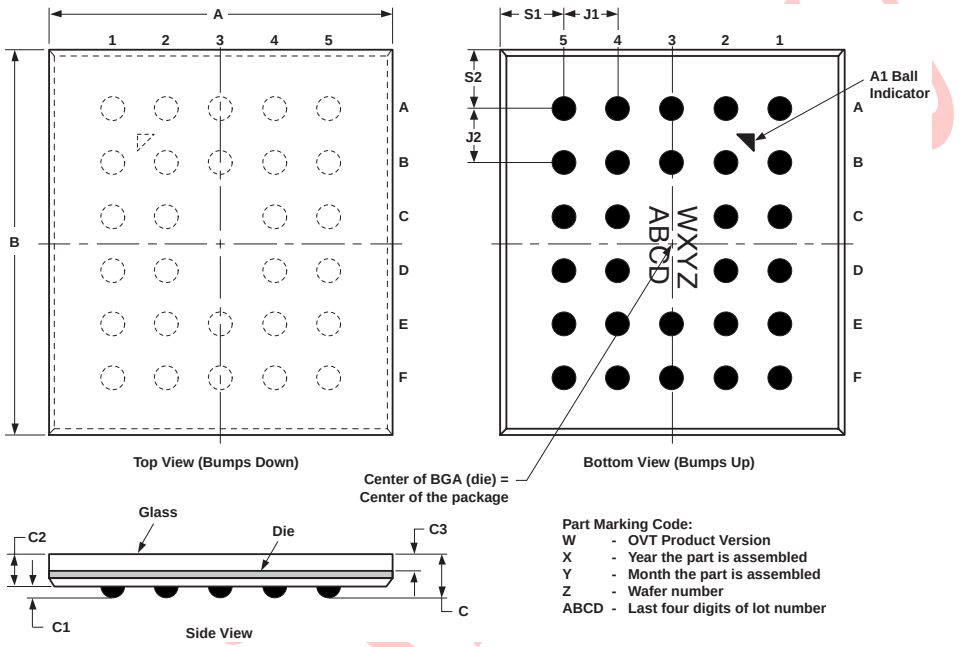
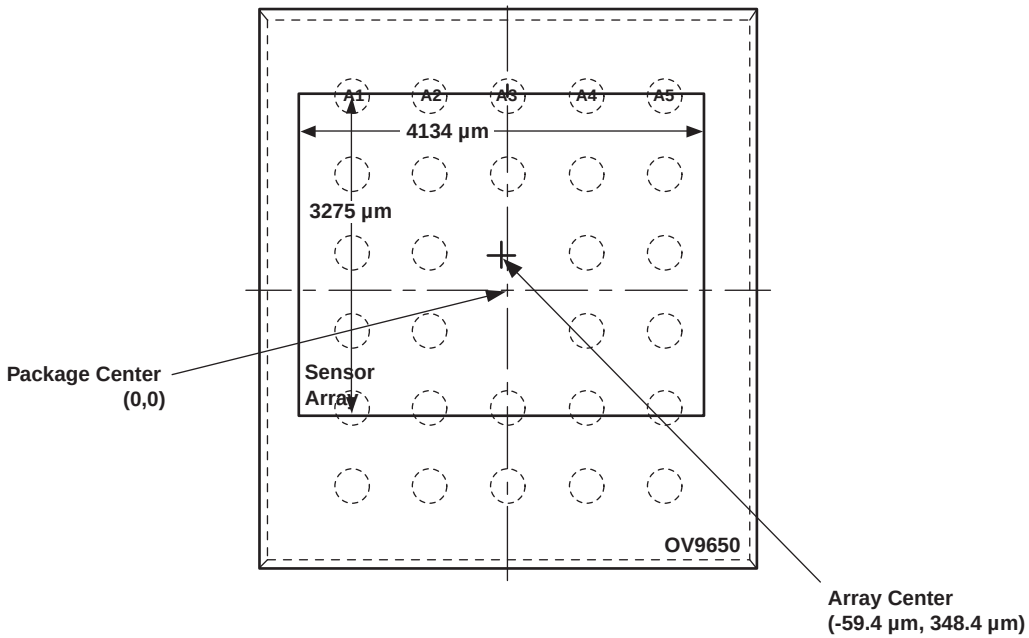


Table 6 CSP Package Dimensions

Parameter	Symbol	Min	Nominal	Max	Unit
Package Body Dimension X	A	5070	5095	5120	µm
Package Body Dimension Y	B	5690	5715	5740	µm
Package Height	C	760	820	880	µm
Ball Height	C1	150	180	210	µm
Package Body Thickness	C2	605	640	675	µm
Thickness of Glass Surface to Wafer	C3	395	415	435	µm
Ball Diameter	D	320	350	380	µm
Total Pin Count	N		28 (3 NC)		
Pin Count X-axis	N1		5		
Pin Count Y-axis	N2		6		
Pins Pitch X-axis	J1		800		µm
Pins Pitch Y-axis	J2		800		µm
Edge-to-Pin Center Distance Analog X	S1	918	948	978	µm
Edge-to-Pin Center Distance Analog Y	S2	828	858	888	µm

Sensor Array Center

Figure 17 OV9650 Sensor Array Center



NOTES: 1. This drawing is not to scale and is for reference only.

2. As most optical assemblies invert and mirror the image, the chip is typically mounted with pins A1 to A5 oriented down on the PCB.

The recommended lens chief ray angle for the OV9650 is 20 degrees.

IR Reflow Ramp Rate Requirements

OV9650 Lead-Free Packaged Devices

Note: For OVT devices that are lead-free, all part marking letters are lower case

Figure 18 IR Reflow Ramp Rate Requirements

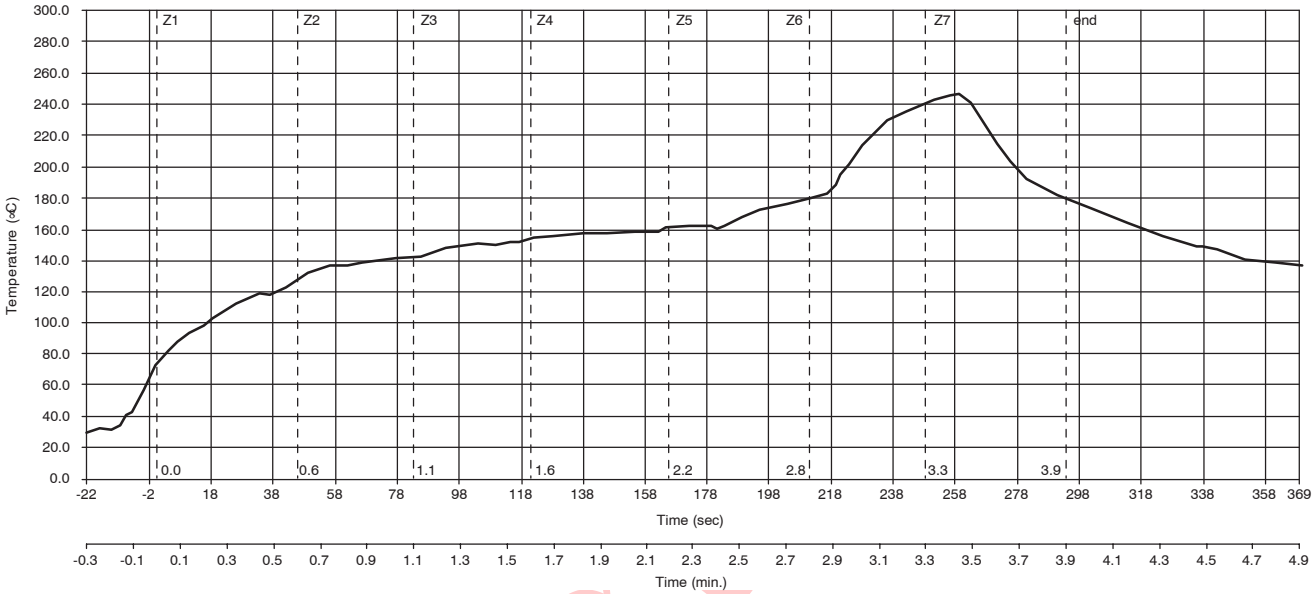


Table 7 Reflow Conditions

Condition	Exposure
Average Ramp-up Rate (30°C to 217°C)	Less than 3°C per second
> 100°C	Between 330 - 600 seconds
> 150°C	At least 210 seconds
> 217°C	At least 30 seconds (30 ~ 120 seconds)
Peak Temperature	245°C
Cool-down Rate (Peak to 50°C)	Less than 6°C per second
Time from 30°C to 255°C	No greater than 390 seconds

Environmental Specifications

Table 8 OV9650 Reliability Test Results

Parameter	Test Condition
Temperature/Humidity	85°C/85% Relative Humidity, 1000 hrs.[a]
Temperature Cycling (Air-to-Air)	-25°C / +125°C, 72 cycles/day, 1000 cycles[a]
Highly Accelerated Stress Test (HAST)	110°C / 85% Relative Humidity, 168 hrs.[a]
High Temperature Storage (HTS)	150°C, 1000 hrs.[a]
High Temperature Static Bias (HTSB)	125°C, 1000 hrs.[a]

a. Pre-Condition (Moisture Level II): 125°C, 24h → 85°C/60% RH/168h → IR Reflow 235°C, 10 sec, 3 cycles

Note:

- *All information shown herein is current as of the revision and publication date. Please refer to the OmniVision web site (http://www.ovt.com) to obtain the current versions of all documentation.*

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