# Problem Description:

**Type**  : CYPD4226-40LQXI

**Origin of Defect** : Board Assembly

|  |  |  |  |
| --- | --- | --- | --- |
| **Infineon Item** | **Customer Identification** | **DC** | **Lot Number** |
| 1 | N/A | 1937 | 611935195 |
| 2 | N/A | 1937 | 611935195 |
| 3 | N/A | 1937 | 611935195 |

**Customer Failure Description:**

1. Detailed description of failure per unit :

returned the 3 failed EVT-PCBA.

Customer ex-change the failure CYPD4226 and Ok CYPD4226 , the symptom follow the failure CYPD4226.

2. Isolation tests (e.g., thermal scan, boundary scan, impedance measurement on Cypress part/pins, etc.).

N/A

3. Failure detection point.

EVT Function Test.

4. Failure rate observed (quantity tested/failed).

total :100 pcs , 97 pass / 3 failed.

5. Time/ Cycles/ Distance to failure.

EVT

6. Date code/s affected or images showing condition and/or top-mark of the failure.

No

7. Firmware/ Hex image used on the failing unit.

8. Software/ Firmware SDK version used. Is it a production-released version?

Host SDK. Ver 3.2.1 it is production-released version can be download from Cypress Web.

9. Reject units sent on board, whether full board or cut board.

only sent Chip.

**Customer Production Date:** Not Provided

**Customer Observed Failure Date:** Not Provided

**Failure Detection Point:** Board Assembly

**Hours to Failure / Mileage (Auto):** 0

**Samples Tested:** 100

**Failure Rate (ppm):** Not Provided

**Additional Customer Provided Details / Attachments:** Not Provided

**Infineon Failure Verification:**

1. **Optical Microscopy**

S/N #: 1-3

Comment: The returned unit was optically inspected and showed no package related anomaly.

|  |  |
| --- | --- |
| Pin 1  **Top package** | **Bottom package**  Pin 1 |

1. **Acoustic Microscopy**

S/N #: 1-3

Comment: C-Mode Scanning Acoustic Microscopy (CSAM) showed no package delamination.

|  |
| --- |
| S/N 3  S/N 2  S/N 1  Pin 1 |

1. **Radiology**

S/N #: 1-3

Comment: X-ray photo showing no apparent wire anomaly.

|  |  |
| --- | --- |
| Pin 1  **S/N 1** | Pin 1  **S/N 2** |

|  |
| --- |
| Pin 1  **S/N 3** |

1. **Package decapsulation**

S/N #: 2-3

Comment: EOS damage was found.

|  |  |
| --- | --- |
| Pin 1  **S/N 2** | Pin 29  (P3[3]) |

|  |  |
| --- | --- |
| **S/N 3** | Pin 2  (P1[2]) |

**Physical Failure Analysis/Signature PFA Analysis Summary:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Type of Analysis** | **S/N** | **Technique** | **Result / Comment** |
| Visual / Mechanical | 1-3 | Optical microscopy | No package related defect was noted upon receipt. |
| 1-3 | Acoustic Microscopy | No package delamination |
| 1-3 | Radiology | No apparent anomaly. |
| 1-3 | Lead conditioning | All leads were reconditioned. |
| Electrical | 1-3 | Outgoing Production Test (ATE) | All units failed on continuity testing on the ATE using the QA test program at room temperature. |
| 1-3 | DC Bench Test | All units failed short:   * S/N 1 – short on pins 29 (P3[3]), 30 (P3[4]), 32 (VDDIO), and 33 (VCCD) * S/N 2 – short on pins 28 (P3[2]), 29 (P3[3]), 30 (P3[4]), 32 (VDDIO), and 33 (VCCD) * S/N 3 – short on pins 1 (P1[1]), 2 (P1[2]), 3 (P1[3]), and 32 (VDDIO) |
| Physical | 2, 3 | Chemical decap | Die was exposed. |
| Visual / Mechanical | 2, 3 | Optical Microscopy | EOS damage was revealed. |

**Effects of Failure to Customer Reported Failure Observation - Summary:**

| **S/N** | **Failure Analysis Observation** | **Customer Reported Failure Summary** | **Failure Confirmed / Correlated (Y/N)** |
| --- | --- | --- | --- |
| 1-3 | EOS damage | returned the 3 failed EVT-PCBA | Y |

# 3D - Containment Action:

**Initial Containment Actions Checklist:**

|  |  |  |  |
| --- | --- | --- | --- |
| **Containment Actions** | **Who** | **When** | **Status** |
| Conduct lot yield history to check for any abnormalities  **Results:** With MRB history | Cary Romero | 10-Dec-2020 | Completed |
| Check remnant of the affected lot at Bin Inventory and Finish Goods  **Results:** No available inventory at Finish Goods. | Cary Romero | 10-Dec-2020 | Completed |

**Lot Numbers and Failure Code:**

| **S/N** | **Customer Identification** | **Seal Date Code** | **Date Code** | **Mark**  **Lot** | **Assembly Lot** | **Fab**  **Lot** | **Failure Code** |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 1 | N/A | N/A | 1937 | 611935195 | 611935195 | 3828075+ | EOS |
| 2 | N/A | N/A | 1937 | 611935195 | 611935195 | 3828075+ | EOS |
| 3 | N/A | N/A | 1937 | 611935195 | 611935195 | 3828075+ | EOS |

**Manufacturing Sites and Technology:**

| **S/N** | **Fab Location** | **Assembly Location** | **Manufacturing Part#** | **Technology** |
| --- | --- | --- | --- | --- |
| 1 | F25 | RA | 7C64210A-LQI | S8 |
| 2 | F25 | RA | 7C64210A-LQI | S8 |
| 3 | F25 | RA | 7C64210A-LQI | S8 |

# 4D - Root Cause Analysis:

Physical analysis was done on S/N 2 and 3. Internal visual ispection after package decapsulation showed electrical overstress (EOS) damage on both units. The damage on both units was in the form of burnt metallization. Based on the electrical signature, S/N 1 most likely failed due to EOS damage.

In conclusion, the failure was confirmed. The units failed ATE due to EOS damage. We recommend that the application and test conditions be reviewed for any possibility of power surge or other sources of overstress. Please feel free to contact your local Field Application Engineer for assistance in device specification. For more information about EOS please visit the Cypress Quality webpage to review the white paper “Electrical Overstress (EOS) and FAQ” ( <http://www.cypress.com/?rID=40421> ).

# 5D - Corrective Action and Verification:

* N/A.

# 6D - Implementation of Permanent Corrective Action:

* N/A.

# 7D - Prevention:

* N/A.

# 8D - Information to Team:

This report has been reviewed and approved by Infineon Failure Analysis management.

|  |  |  |
| --- | --- | --- |
| **Approver(s)** | **Designation** | **Date** |
| Mohan Vompolu | Failure Analyst | December 14, 2020 |
| Rochelle Arreola | Sr Mgr Product Engrg | December 14, 2020 |

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| --- | --- |
| FA Case Stage | Description |
| Receiving / Lot Scoping | The receipt of the customer notification is acknowledged. If the lot or datecode information is available, lot scoping is performed and containment action determined. |
| Issue Confirmation | Initial device testing; verification of internal device settings, confirmation of customer problem description; outgoing quality testing. |
| Electrical Fault Isolation | If the device fails the outgoing test screens, further electrical fault isolation is performed to determine the root cause of the malfunction. |
| Physical Analysis | Based on electrical or visual-mechanical findings, the device is analyzed with physical analysis techniques (decapsulation, delayering, cross-section…) |
| Root Cause Analysis | Root cause analysis and corrective actions defined |
| Final Report | Analysis is complete. Final report is submitted to customer for review. |

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| --- | --- |
| **Abbreviation** | **Details (Full Form)** |
| ATE | Automated Test Equipment |
| BEOL | Back End of Line (processes dealing with the metal interconnects of the integrated circuit) |
| BER | Bit Error Rate |
| BT | Bluetooth |
| BTC | Biased Temperature Cycling |
| CDM | Charged Device Model |
| CIP | Continuous Improvement Program or Continuous Improvement Plan |
| CMP | Chemical Mechanical Polish – wafer level planarization process step |
| Decap | Decapsulation. Process of opening up an encapsulated package to expose the die |
| EDX | Energy Dispersive X-Ray |
| EFA | Electrical Failure Analysis |
| EIPD | Electrically Induced Physical Damage |
| EOS | Electrical OverStress |
| ESD | Electrostatic Discharge |
| FEOL | Front End of Line (processes dealing with the formation of transistors up to cosilicide) |
| FIB | Focused Ion Beam |
| FTIR | Fourier Transform Infrared Spectroscopy |
| GOX | Gate oxide |
| HAST | Highly Accelerated Stress Test |
| HBM | Human Body Model |
| IDS | Drain-Source Current |
| IoT | Internet of Things |
| ILD | Inter-Level Dielectric (may be preceded or followed by some number) is the oxide dielectric layer deposited on the wafer. |
| NRCL | Non-Reproducible Charge Loss |
| OBIRCH | Optical Beam Induced Resistance Change |
| P/E Cycle | Program-Erase Cycle |
| PEM | Photon Emission Microscopy |
| PER | Packet Error Rate |
| PFA | Physical Failure Analysis |
| POLY | Poly, polysilicon (also PLY and P as in P2 for Poly 2) |
| PVC | Passive Voltage Contrast |
| PVT | Process Voltage Temperature Controller |
| RIE | Reactive Ion Etch |
| SAM | Scanning Acoustic Microscopy |
| SBCL | Single Bit Charge Loss |
| SEM | Scanning Electron Microscopy |
| Shmoo | Two-Dimensional graph that shows the functionality of the device across voltage and timing parameter |
| S/N | Serial Number |
| TDR | Time-domain Reflectometer/Reflectometry |
| TEM | Transmission Electron Microscopy |
| TIVA | Thermally Induced Voltage Alteration |
| TNOX | Tunnel Oxide |
| UV | Ultraviolet (light) |
| Vt | Threshold Voltage |
| VWL | Wordline Voltage |

**Attachments/Enclosures/Comments:**