Programmable USB Type-C PD Controller

General Description

RT1711H is a USB Type-C controller that complies with the latest USB Type-C and PD standards. RT1711H integrates a complete Type-C Transceiver including the Rp and Rd resistors. It does the USB Type-C detection including attach and orientation. RT1711H integrates the physical layer of the USB BMC power delivery protocol to allow up to 100W of power and role swap. The BMC PD block enables full support for alternative interfaces of the Type-C specification.

Features

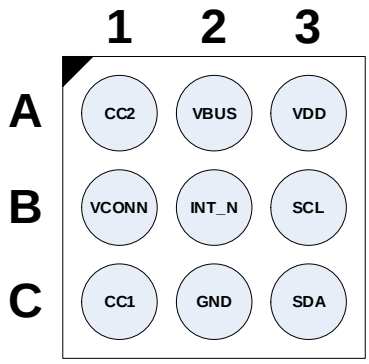
Dual-role PD compatible
Attach/Detach detection as host, device or DRP
Current capability definition and detection
Cable recognition
Alternate mode support
Supporting VCONN with programmable OCP
Dead battery support
Ultra-low power mode for attach detection(<10uA)
Simple I2C interface with AP or EC
BIST mode supported
e-fuse IP
WLCSP 1.3x1.3-9 package

Applications

Smartphones
Tablets
Laptops

Pin Configurations

(TOP VIEW)

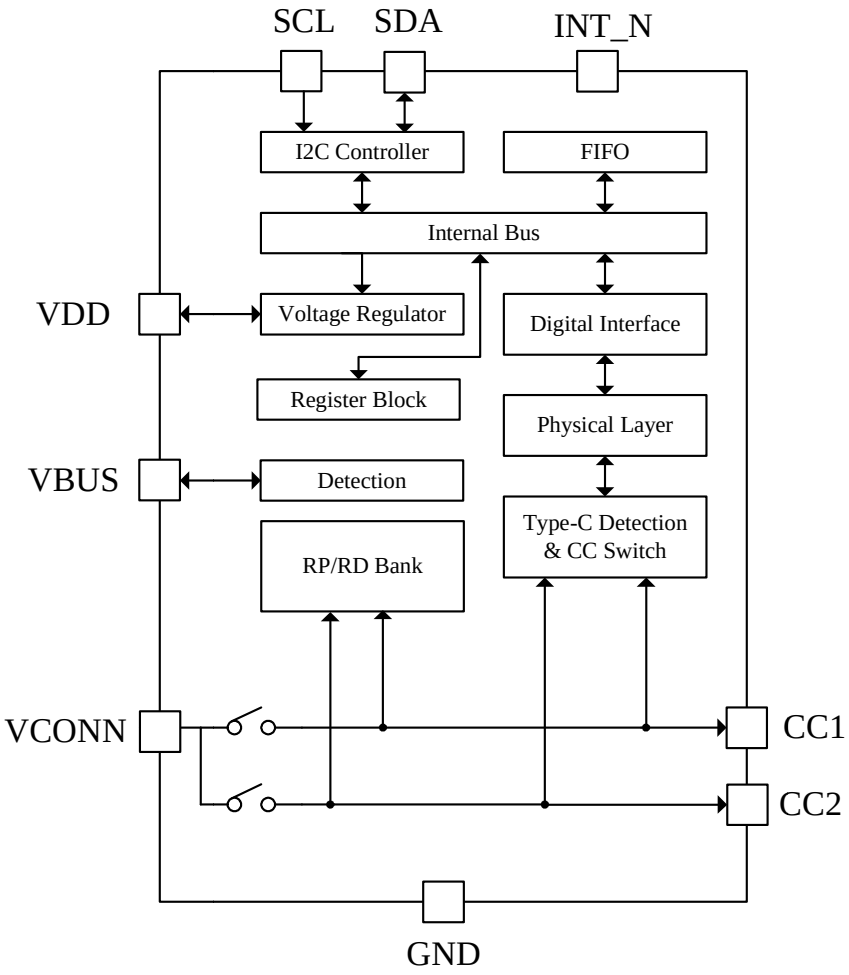


WLCSP 1.3x1.3-9

Functional Pin Description

Pin No.	Pin Name	Pin Function
A1	CC2	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
A2	VBUS	VBUS input pin for attach and detach detection when operating as an UFP port (Device).
A3	VDD	Input supply voltage.
B1	VCONN	Regulated input pin to be switched to correct CC pin as VCONN to power Type-C full-featured cables and other accessories.
B2	INT_N	Active low and open drain type interrupt output used to prompt the processor to read the registers.
B3	SCL	I^2C serial data signal to be connected to the I^2C master.
C1	CC1	Type-C connector Configuration Channel (CC) pins. Initially used to determine when an attach has occurred and what the orientation detected.
C2	GND	Ground pin
C3	SDA	I^2C serial data signal to be connected to the I^2C master.

Function Block Diagram



Absolute Maximum Ratings(Note1)

VDD/VCONN ---------- -0.3V to 6V

CC1/CC2 ---------- -0.3V to 28V

VBUS series with 169K resistor ---------- 28V

Package Thermal Resistance(Note 2)

WLCSP 3x3-9, θ_{JA} ---------- 31.5℃/W

WLCSP 3x3-9, θ_{JC} ---------- 7.5℃/W

Lead Temperature (Soldering, 10 sec.)---------- 260°C

Junction Temperature ---------- 150°C

Storage Temperature Range ---------- –65°C to 150°C

ESD Susceptibility (Note 3)

HBM (Human Body Model) ---------- 2KV

MM (Machine Model) ---------- 200V

Recommended Operating Conditions(Note 4)

Supply Input Voltage ---------- 2.7V to 5.5V

VCON Supply Current---------- 200 ~600mA

VCON Supply Voltage ---------- 4V to 5.5V

Ambient Temperature Range ---------- –40°C to 85°C

Junction Temperature Range ---------- –40°C to 125°C

Electrical Characteristics

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Common Normative Signaling Requirements						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Bit rate	fBitRate		270	300	330	Kbps

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

Common Normative Signaling Requirements for Transmitter						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Maximum difference between the bit-rate during the part of the packet following the Preamble and the reference bit-rate.	pBitRate				0.25	%
Time from the end of last bit of a Frame until the start of the first bit of the next Preamble.	tInterFrameGap		25			µs
Time before the start of the first bit of the Preamble when the transmitter shall start driving the line.	tStartDrive		-1		1	µs

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

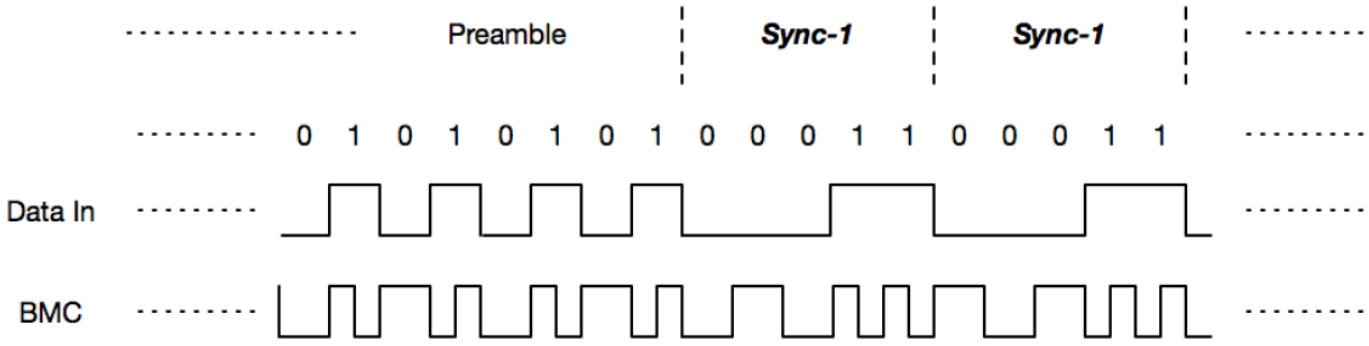
BMC Common Normative Requirements						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Time to cease driving the line after the end of the last bit of the Frame.	tEndDriveBMC				23	µs
Fall Time	tFall		300			ns
Time to cease driving the line after the final high-to-low transition	tHoldLowBMC		1			µs
Rise time	tRise		300			ns
Voltage Swing	vSwing		1.05	1.125	1.2	V
Transmitter output impedance	zDriver		33		75	Ω

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

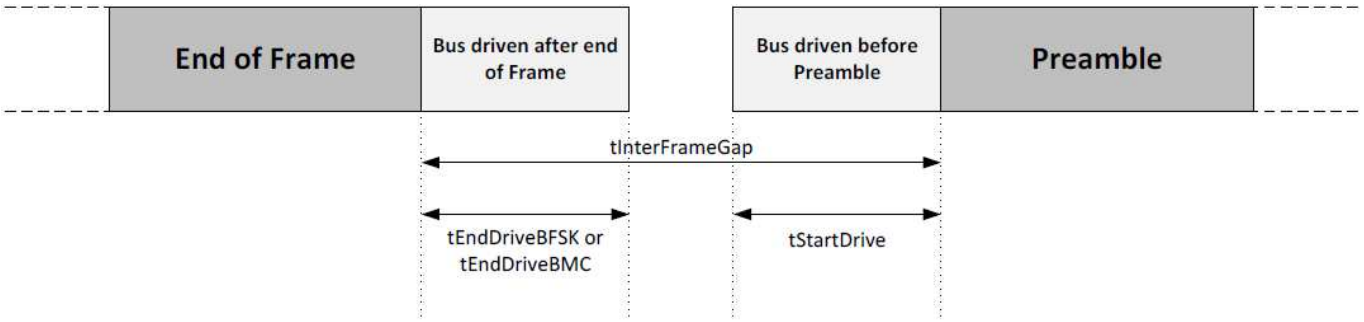
BMC Receiver Normative Requirements						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Cable Termination	RA		800		1200	Ω
Time window for detecting non-idle	tTransitionWindow		12		20	µs
Receiver Input Impedance	zBmcRx		10			MΩ

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

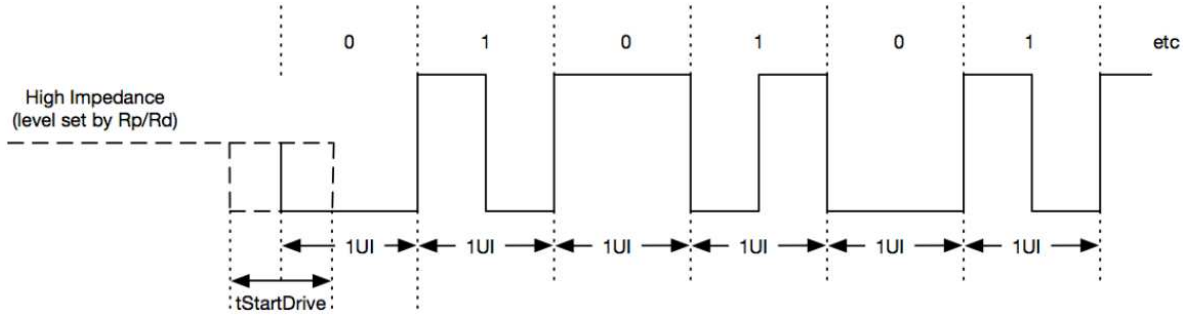
Type-C Port control						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Ron for VCONN switch	R_{ON}			1		Ω
OCP range	I_{OCP}		200		600	mA
Time for VCONN switch to turn-on state	T_{soft}			1.2		ms
DFP 80uA CC current	DFP_{80u}		64	80	96	uA
DFP 180uA CC current	DFP_{180u}		166	180	194	uA
DFP 330uA CC current	DFP_{330u}		304	330	356	uA
UFP Rd	Rd		4.59	5.1	5.61	KΩ
UFP pull-down voltage in dead battery under DFP_{80u} and DFP_{180u}	V_{DBL}				1.6	V
UFP pull-down voltage in dead battery under DFP_{330u}	V_{DBH}				2.6	V
VBUS detection valid voltage				4		V
VBUS measure range			4		23	V
VBUS measurement step when VBUS range under 4~10V				0.5		V
VBUS measurement step when VBUS range under 10~20V				1		V



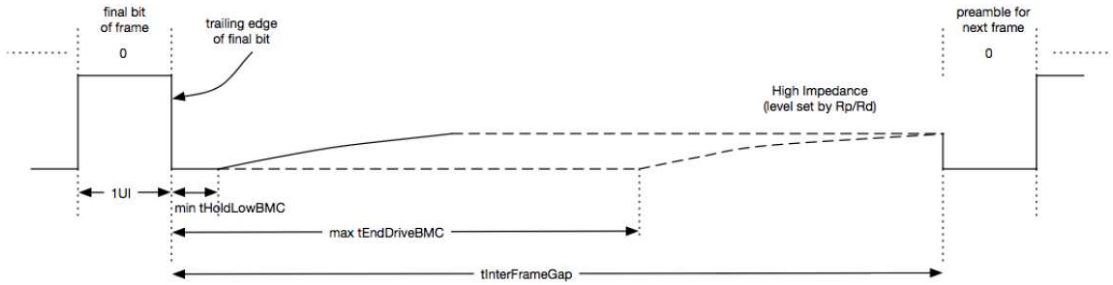
BMC Example



Inter-Frame Gap Timings



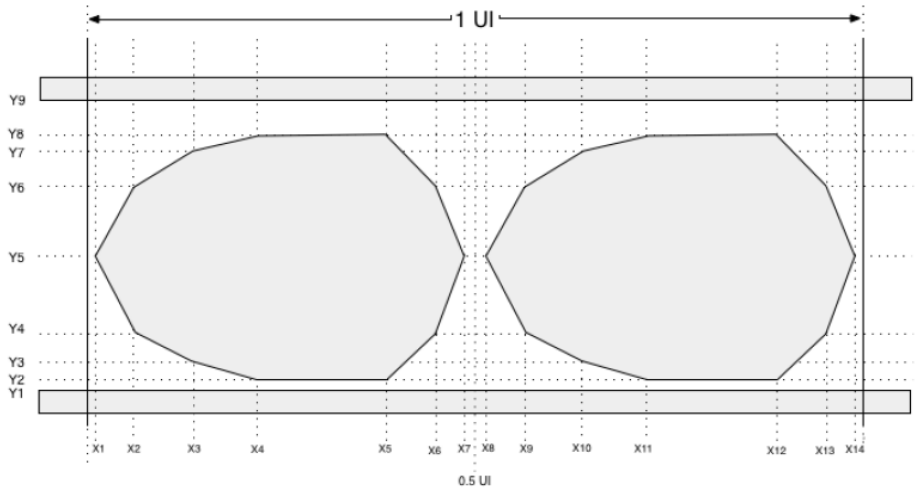
BMC Encoded Start of Preamble



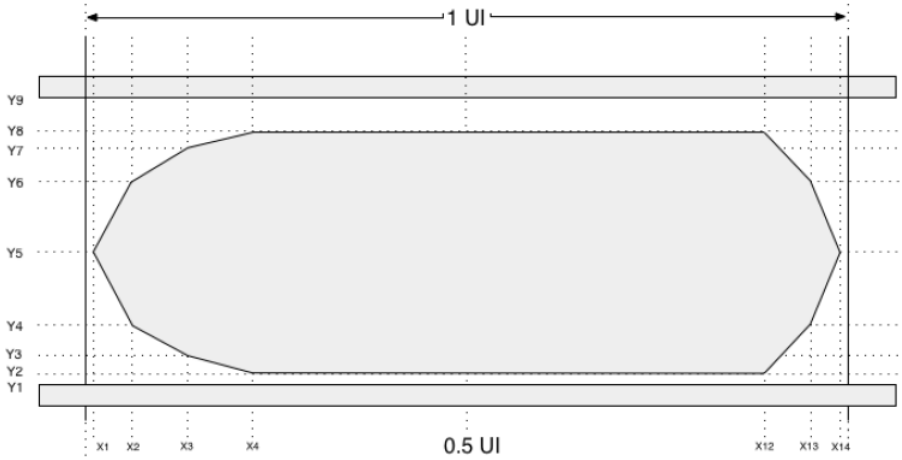
Transmitting or Receiving BMC Encoded Frame Terminated

BMC TC Mask Definition, X values						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Left Edge of Mask	X1Tx			0.015		UI
X2Tx point	X2Tx			0.07		UI
X3Tx point	X3Tx			0.15		UI
X4Tx point	X4Tx			0.25		UI
X5Tx point	X5Tx			0.35		UI
X6Tx point	X6Tx			0.43		UI
X7Tx point	X7Tx			0.485		UI
X8Tx point	X8Tx			0.515		UI
X9Tx point	X9Tx			0.57		UI
X10Tx point	X10Tx			0.65		UI
X11Tx point	X11Tx			0.75		UI
X12Tx point	X12Tx			0.85		UI
X13Tx point	X13Tx			0.93		UI
Right Edge of Mask	X14Tx			0.985		UI

BMC TC Mask Definition, Y values						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
Lower bound of Outer mask	Y1Tx			-0.075		V
Lower bound of inner mask	Y2Tx			0.075		V
Y3Tx point	Y3Tx			0.15		V
Y4Tx point	Y4Tx			0.325		V
Inner mask vertical midpoint	Y5Tx			0.5625		V
Y6Tx point	Y6Tx			0.8		V
Y7Tx point	Y7Tx			0.975		V
Y8Tx point	Y8Tx			1.04		V
Upper Bound of Outer mask	Y9Tx			1.2		V



BMC Tx ‘ONE’ Mask



BMC Tx ‘ZERO’ Mask

(V_{DD} = 3.3V, T_A = 25°C, unless otherwise specified)

I2C Electrical Characteristics						
Parameter	**Symbol**	**Test Conditions**	**Min**	**Typ**	**Max**	**Units**
I2C bus Supply Voltage	I2C_VDD		1.5		3.6	V
LOW-level input voltage	VIL		-0.5		0.3VDD	V
HIGH-level input voltage	VIH		0.7VDD		VDD+0.5	V
Hysteresis of Schmitt trigger inputs	VHYS		0.05VDD			V
LOW-level output voltage	VOL	Open-drain	-		0.4	V
Input current each IO Pin	II	0.1VDD< VI<0.9VDDMAX	-10		+10	uA
SCL Clock Frequency	FSCL		0		1000	KHz
Pulse width of spikes that must be suppressed by the input filter	tSP				50	ns
LOW period of the SCL clock	tLOW		0.5		-	us
HIGH period of the SCL clock	tHIGH		0.26		-	us
Data hold time	tHD:DAT		0		-	us
Data set-up time	tSU:DAT		50		-	ns
Bus free time between a STOP and START condition	tBUF		0.5		-	us
Data valid time	tVD:DAT				0.45	us
Data valid acknowledge time	tVD:ACK				0.45	us

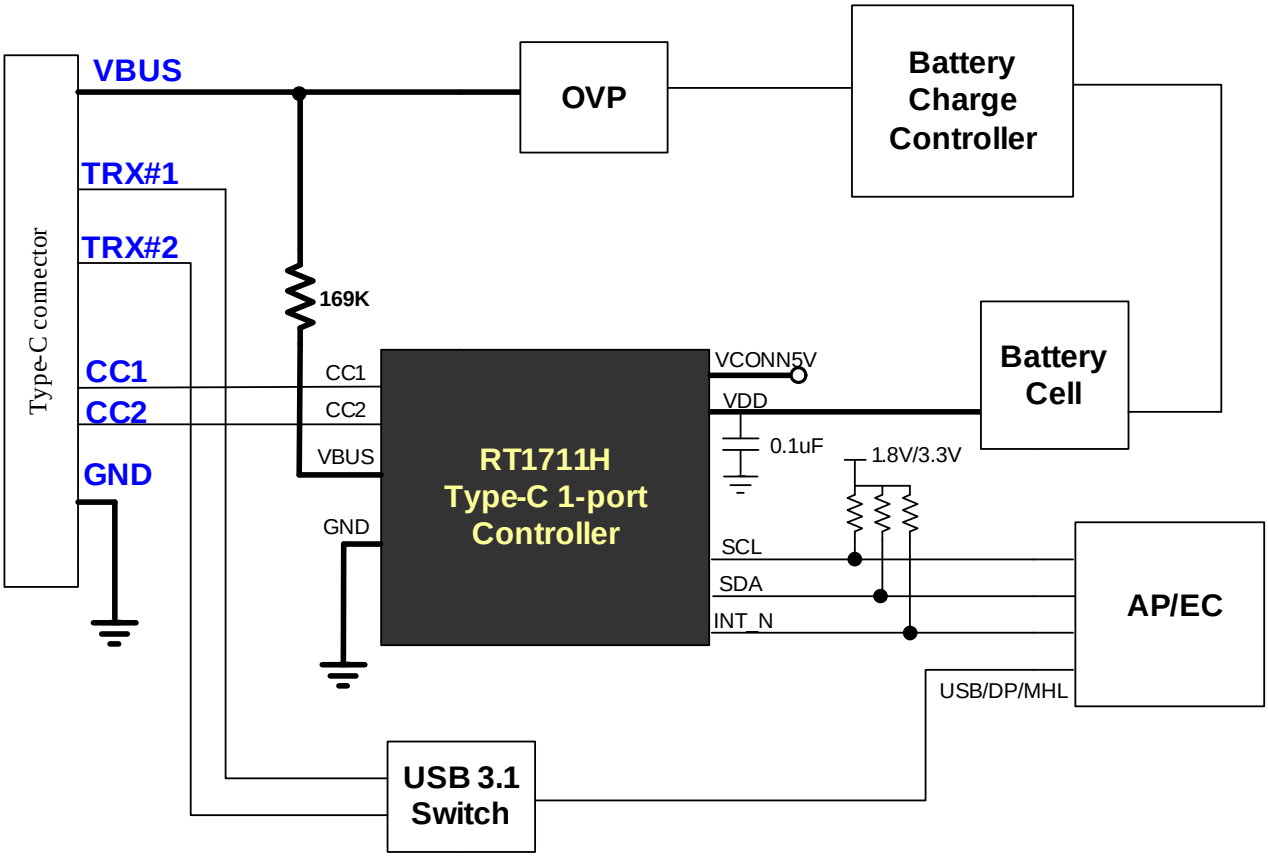
Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

θ_{JA} is measured at T_A= 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ_{JC} is measured at the exposed pad of the package.

Devices are ESD sensitive. Handling precaution recommended.

The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

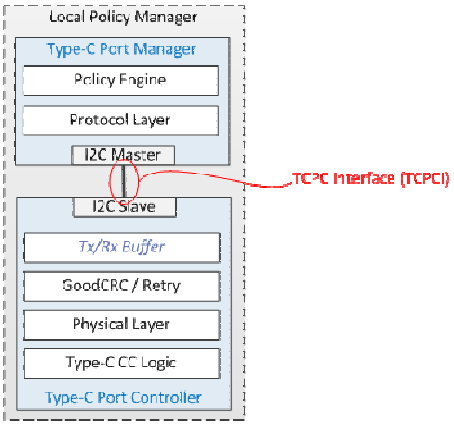


Application Information

Abbreviations:

Term	Description
BMC	Biphase Mark Coding
TCPC	Type-C Port Controller
TCPCI	Type-C Port Controller Interface
TCPM	Type-C Port Manager

Type-C Port Controller (TCPC) Interface:



The Type-C Port Controller Interface, TCPCI, is the interface between a Type-C Port Manager and a Type-C Port Controller.

The Controller Interface uses the I2C protocol:

- The TCPM is the only master on this I2C bus
- The TCPC is a slave device on this I2C bus
- Each Type-C port has its own unique I2C slave address. The TCPC shall have equal numbers of unique I2C slave addresses and supported Type-C ports
- The TCPC supports Fast-mode bus speed
- The TCPC has an open drain output, active low INT_N Pin. This pin is used to indicate change of state, where INT_N pin is asserted when any Alert Bits are set
- The TCPCI supports an I/O nominal voltage range of 1.8V and 3.3V
- The TCPC can auto-increment the I2C internal register address of the last byte transferred during a read independent of an ACK/NACK from the master

Register Map:

Address	Register Name	Bit	BitName	Default	Type	Description
0x00	**VENDOR_ID**	7:0	**VID[7:0]**	0	R	A unique 16-bit unsigned integer. Assigned by the USB-IF to the Vendor.
0x01		7:0	**VID[15:8]**	0	R	
0x02	**PRODUCT_ID**	7:0	**PID[7:0]**	0	R	A unique 16-bit unsigned integer. Assigned uniquely by the Vendor to identify the TCPC.
0x03		7:0	**PID[15:8]**	0	R	
0x04	**DEVICE_ID**	7:0	**DID[7:0]**	0	R	A unique 16-bit unsigned integer. Assigned by the Vendor to identify the version of the TCPC.
0x05		7:0	**DID[15:8]**	0	R	
0x06	**USBTYPEC_REV**	7:0	**USBTYPEC_REV**	0	R	Version number assigned by USB-IF (Currently at Revision 1.1 – 0001 0001)
0x07		7:0	**Reserved**	0	R	
0x08	**USBPD_REV_VER**	7:0	**USBPD_VER**	0	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x09		7:0	**USBPD_REV**	0	R	0010 0000 – Revision 2.0
0x0A	**PD_INTERFACE_REV**	7:0	**PDIF_VER**	0	R	0001 0000 – Version 1.0 0001 0001 – Version 1.1 Etc.
0x0B		7:0	**PDIF_REV**	0	R	0010 0000 – Revision 2.0
0x0C	**DEVICE_CAPABILITIES_1**	7:6	**SOURCE_RP_SUPPORT**	10	R	00b: Rp default only 01b: Rp 1.5A and default 10b: Rp 3.0A, 1.5A, and default 11b: Reserved Rp values which may be configured by the TCPM via the ROLE_CONTROL register
		5:3	**ROLES_SUPPORT**	110	R	000b: Type-C Port Manager can configure the Port as Source only or Sink only (not DRP) 001b: Source only 010b: Sink only 011b: Sink with accessory support (optional) 100b: DRP only 101b: Adapter or Cable (Ra) only 110b: Source, Sink, DRP, Adapter/Cable all supported 111b: Not valid

		2	**SOURCE_VCONN**	1	R	0b: TCPC is not capable of switching VCONN 1b: TCPC is capable of switching VCONN
		1	**SINK_VBUS**	0	R	0b: TCPC is not capable controlling the sink path to the system load 1b: TCPC is capable of controlling the sink path to the system load
		0	**SOURCE_VBUS**	0	R	0b: TCPC is not capable of controlling the source path to VBUS 1b: TCPC is capable of controlling the source path to VBUS
0x0D	**DEVICE_CAPABILITIES_2**	7:5	**Reserved**	0	R	
		4	**VBUS_MEASURE**	1	R	0b: No VBUS voltage measurement 1b; VBUS voltage measurement Reported in VBUS_VOLTAGE Register
		3	**SINK_VOL_H**	0	R	0b: No Separate high voltage VBUS sink path 1b; Separate high voltage VBUS sink path
		2	**SOURCE_VOL_H**	0	R	0b: No Separate high voltage VBUS source path 1b; Separate high voltage VBUS source path
		1	**Reserved**	0	R	
		0	**ALL_SOP_SUPPORT**	1	R	0b: All SOP* except SOP'_DBG/SOP"_DBG 1b: All SOP* messages are supported
0x0E	**DEVICE_CAPABILITIES_3**	7:6	**GPIO_OUT_3**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		5:4	**GPIO_OUT_2**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		3:2	**GPIO_OUT_1**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		1:0	**GPIO_OUT_0**	11	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output

0x0F	**DEVICE_CAPABILITIES_4**	7:6	**GPIO_OUT_7**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		5:4	**GPIO_OUT_6**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		3:2	**GPIO_OUT_5**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
		1:0	**GPIO_OUT_4**	0	R	00b: Not available 01b: Open drain output 10b: Push-pull output 11b: Three-state output
0x10	**ALERT**	7	**WAKEUP**	0	RW	0b: Cleared, 1b: Sleep Mode Exited
		6	**TX_SUCCESS**	0	RW	0b: Cleared, 1b: Reset or SOP* message transmission successful.
		5	**TX_DISCARD**	0	RW	0b: Cleared, 1b: Reset or SOP* message transmission not sent due to incoming receive message.
		4	**TX_FAIL**	0	RW	0b: Cleared, 1b: SOP* message transmission not successful, no GoodCRC response received on SOP* message transmission.
		3	**RX_HARD_RESET**	0	RW	0b: Cleared, 1b: Received Hard Reset message
		2	**RX_STATUS**	0	RW	0b: Cleared, 1b: Receive status register changed
		1	**PORT_STATUS**	0	RW	0b: Cleared, 1b: Port status changed
		0	**CC_STATUS**	0	RW	0b: Cleared, 1b: CC status changed
0x11	**ALERT**	7:6	**Reserved**	0	R	
		5	**Reserved**	0	R	
		4	**GPIO_CHANGE**	0	RW	0b: Cleared 1b: GPIO_STATUS has changed
		3	**Reserved**	0	R	

		2	**Reserved**	0	R	
		1	**Reserved**	0	R	
		0	**Reserved**	0	R	
0x12	**ALERT_MASK**	7	**M_WAKEUP**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		6	**M_TX_SUCCESS**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		5	**M_TX_DISCARD**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		4	**M_TX_FAIL**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		3	**M_RX_HARD_RESET**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		2	**M_RX_STATUS**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		1	**M_PORT_STATUS**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		0	**M_CC_STATUS**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
0x13	**ALERT_MASK**	7:6	**Reserved**	0	R	
		5	**Reserved**	0	R	
		4	**M_GPIO_CHANGE**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		3	**Reserved**	0	R	
		2	**Reserved**	0	R	
		1	**Reserved**	0	R	
		0	**Reserved**	0	R	
0x14	**POWER_STATUS_MASK**	7	**Reserved**	0	R	
		6	**Reserved**	0	R	
		5	**M_VBUS_PRESENT**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		4	**M_VCON_OCP**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		3	**M_VCON_OVP**	0	RW	0b: Interrupt masked, 1b: Interrupt unmasked
		2	**Reserved**	0	R	
		1	**Reserved**	0	R	
		0	**Reserved**	0	R	
0x18	**CC_STATUS**	7:6	**Reserved**	0	R	
		5	**DRP_STATUS**	0	R	0b: the TCPC has stopped toggling or (ROLE_CONTROL.DRP=00) 1b: the TCPC is toggling
		4	**DRP_RESULT**	0	R	0b: the TCPC is presenting Rp 1b: the TCPC is presenting Rd

		3:2	**CC2_STATUS**	0	R	If (ROLE_CONTROL.CC2=Rp) or (DrpResult=0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC2=Rd) or (DrpResult=1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp 1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp 3.0A
						
						If ROLE_CONTROL.CC2=Ra, this field is set to 00b
						If ROLE_CONTROL.CC2=Open, this field is set to 00b
						
						This field always returns 00b if (DrpStatus=1) or (POWER_CONTROL.EnableVconn=1 and POWER_CONTROL.PlugOrientation=0). Otherwise, the returned value depends upon ROLE_CONTROL.CC2.

		1:0	**CC1_STATUS**	0	R	If (ROLE_CONTROL.CC1 = Rp) or (DrpResult=0)
						00b: SRC.Open (Open, Rp)
						01b: SRC.Ra (below maximum vRa)
						10b: SRC.Rd (within the vRd range)
						11b: reserved
						
						If (ROLE_CONTROL.CC1 = Rd) or DrpResult=1)
						00b: SNK.Open (Below maximum vRa)
						01b: SNK.Default (Above minimum vRd-Connect)
						10b: SNK.Power1.5 (Above minimum vRd-Connect) Detects Rp-1.5A
						11b: SNK.Power3.0 (Above minimum vRd-Connect) Detects Rp-3.0A
						
						If ROLE_CONTROL.CC1=Ra, this field is set to 00b
						If ROLE_CONTROL.CC1=Open, this field is set to 00b
						
						This field always returns 00b if (DrpStatus=1) or (POWER_CONTROL.EnableVconn=1 and POWER_CONTROL.PlugOrientation=0). Otherwise, the returned value depends upon ROLE_CONTROL.CC1.

0x19	**POWER_STATUS**	7	**Reserved**	0	R	
		6	**Reserved**	0	R	
		5	**VBUS_PRESENT**	0	R	0b: VBUS Disconnected 1b: VBUS Connected
		4	**VCON_OCP**	0	R	0b: Not in an over-current protection state 1b: Over-current fault latched
		3	**VCON_OVP**	0	R	0b: Not in an over-voltage protection state 1b: Over-voltage fault latched.
		2	**VCONN_FAULT**	0	R	0b: No Fault detected 1b: Over current/voltage VCONN fault latched
		1	**Reserved**	0	R	
		0	**Reserved**	0	R	
0x1A	**ROLE_CONTROL**	7:6	**DRP**	0	RW	00b: No DRP. Bits B3..0 determine Rp/Rd/Ra settings 01b: DRP
		5:4	**RP_VALUE**	0	RW	00b: Rp default 01b: Rp 1.5A 10b: Rp 3.0A 11b: Reserved
		3:2	**CC2**	11	RW	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (dDisconnect or don't care) Set to 11b if enabling DRP in B7..6
		1:0	**CC1**	11	RW	00b: Ra 01b: Rp (Use Rp definition in B5..4) 10b: Rd 11b: Open (dDisconnect or don't care) Set to 11b if enabling DRP in B7..6
0x1B	**POWER_PATH_CONTROL**	7:4	**Reserved**	0	R	
		3	**Reserved**	0	R	
		2	**Reserved**	0	R	
		1	**Reserved**	0	R	
		0	**Reserved**	0	R	
0x1C	**POWER_CONTROL**	7:6	**Reserved**	0	R	
		5	**Reserved**	0	R	

		4	**PLUG_ORIENT**	0	RW	0b: When Vconn is enabled, apply it to the CC2 pin. Monitor the CC1 pin for BMC communications if PD messaging is enabled. 1b: When Vconn is enabled, apply it to the CC1 pin. Monitor the CC2 pin for BMC communications if PD messaging is enabled. Required
		3	**Reserved**	0	R	
		2	**Reserved**	0	R	
		1	**Reserved**	0	R	
		0	**EN_VCONN**	0	RW	0b: Disable VCONN Source (default) 1b: Enable VCONN Source to CC Required
0x20		7:0	**Reserved**	0	R	
0x21		7:0	**Reserved**	0	R	
0x22		7:0	**Reserved**	0	R	
0x23	**COMMAND**	7:0	**Reserved**	0	R	
0x2E	**MESSAGE_HEADER_INFO**	7:5	**Reserved**	0	R	
		4	**CABLE_PLUG**	0	RW	0b: Message originated from Source, Sink, or DRP 1b: Message originated from a Cable Plug
		3	**DATA_ROLE**	0	RW	0b: Sink 1b: Source
		2:1	**USBPD_SPECREV**	10	RW	00b: Revision 1.0 01b: Revision 2.0 10b – 11b: Reserved
		0	**POWER_ROLE**	0	RW	0b: Sink 1b: Source
0x2F	**RECEIVE_DETECT**	7	**Reserved**	0	R	
		6	**EN_CABLE_RST**	0	RW	0b: TCPC does not detect Cable Reset signaling (default) 1b: TCPC detects Cable Reset signaling
		5	**EN_HARD_RST**	0	RW	0b: TCPC does not detect Hard Reset signaling (default) 1b: TCPC detects Hard Reset signaling
		4	**EN_SOP2DB**	0	RW	0b: TCPC does not detect SOP_DBG'' message (default) 1b: TCPC detects SOP_DBG'' message
		3	**EN_SOP1DB**	0	RW	0b: TCPC does not detect SOP_DBG' message (default) 1b: TCPC detects SOP_DBG' message
		2	**EN_SOP2**	0	RW	0b: TCPC does not detect SOP'' message (default) 1b: TCPC detects SOP'' message

		1	**EN_SOP1**	0	RW	0b: TCPC does not detect SOP' message (default) 1b: TCPC detects SOP' message
		0	**EN_SOP**	0	RW	0b: TCPC does not detect SOP message (default) 1b: TCPC detects SOP message
0x30	**RX_BYTE_COUNT**	7:0	**RX_BYTE_COUNT**	0	RW	Indicates number of bytes in this register that are not stale. The TCPM should read the first RECEIVE_BYTE_COUNT bytes in this register.
0x31	**RX_BUF_FRAME_TYPE**	7:3	**Reserved**	0	R	
		2:0	**RX_FRAME_TYPE**	0	R	Type of received frame 000b: Received SOP 001b: Received SOP' 010b: Received SOP'' 011b: Received SOP_DBG' 100b: Received SOP_DBG'' 110b: Received Cable Reset All others are reserved.
0x32	**RX_BUF_HEADER_BYTE_0**	7:0	**RX_HEAD_0**	0	R	Byte 0 (bits 7..0) of message header
0x33	**RX_BUF_HEADER_BYTE_1**	7:0	**RX_HEAD_1**	0	R	Byte 1 (bits 15..8) of message header
0x34	**RX_BUF_OBJ1_BYTE_0**	7:0	**RX_OBJ1_0**	0	R	Byte 0 (bits 7..0) of 1st data object
0x35	**RX_BUF_OBJ1_BYTE_1**	7:0	**RX_OBJ1_1**	0	R	Byte 1 (bits 15..8) of 1st data object
0x36	**RX_BUF_OBJ1_BYTE_2**	7:0	**RX_OBJ1_2**	0	R	Byte 2 (bits 23..16) of 1st data object
0x37	**RX_BUF_OBJ1_BYTE_3**	7:0	**RX_OBJ1_3**	0	R	Byte 3 (bits 31..24) of 1st data object
0x38	**RX_BUF_OBJ2_BYTE_0**	7:0	**RX_OBJ2_0**	0	R	Byte 0 (bits 7..0) of 2st data object
0x39	**RX_BUF_OBJ2_BYTE_1**	7:0	**RX_OBJ2_1**	0	R	Byte 1 (bits 15..8) of 2st data object
0x3A	**RX_BUF_OBJ2_BYTE_2**	7:0	**RX_OBJ2_2**	0	R	Byte 2 (bits 23..16) of 2st data object
0x3B	**RX_BUF_OBJ2_BYTE_3**	7:0	**RX_OBJ2_3**	0	R	Byte 3 (bits 31..24) of 2st data object
0x3C	**RX_BUF_OBJ3_BYTE_0**	7:0	**RX_OBJ3_0**	0	R	Byte 0 (bits 7..0) of 3st data object
0x3D	**RX_BUF_OBJ3_BYTE_1**	7:0	**RX_OBJ3_1**	0	R	Byte 1 (bits 15..8) of 3st data object
0x3E	**RX_BUF_OBJ3_BYTE_2**	7:0	**RX_OBJ3_2**	0	R	Byte 2 (bits 23..16) of 3st data object
0x3F	**RX_BUF_OBJ3_BYTE_3**	7:0	**RX_OBJ3_3**	0	R	Byte 3 (bits 31..24) of 3st data object
0x40	**RX_BUF_OBJ4_BYTE_0**	7:0	**RX_OBJ4_0**	0	R	Byte 0 (bits 7..0) of 4st data object
0x41	**RX_BUF_OBJ4_BYTE_1**	7:0	**RX_OBJ4_1**	0	R	Byte 1 (bits 15..8) of 4st data object
0x42	**RX_BUF_OBJ4_BYTE_2**	7:0	**RX_OBJ4_2**	0	R	Byte 2 (bits 23..16) of 4st data object
0x43	**RX_BUF_OBJ4_BYTE_3**	7:0	**RX_OBJ4_3**	0	R	Byte 3 (bits 31..24) of 4st data object
0x44	**RX_BUF_OBJ5_BYTE_0**	7:0	**RX_OBJ5_0**	0	R	Byte 0 (bits 7..0) of 5st data object
0x45	**RX_BUF_OBJ5_BYTE_1**	7:0	**RX_OBJ5_1**	0	R	Byte 1 (bits 15..8) of 5st data object

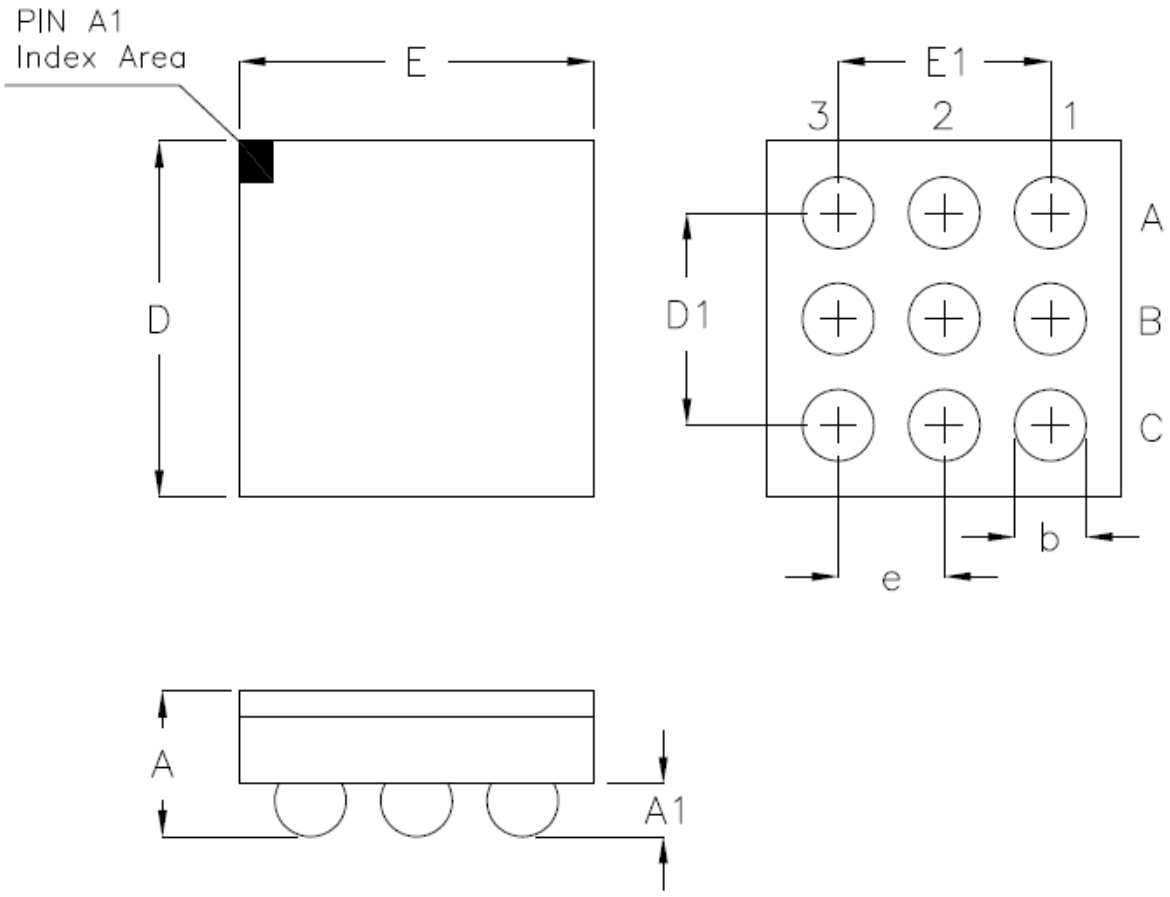
0x46	RX_BUF_OBJ5_BYTE_2	7:0	RX_OBJ5_2	0	R	Byte 2 (bits 23..16) of 5st data object
0x47	RX_BUF_OBJ5_BYTE_3	7:0	RX_OBJ5_3	0	R	Byte 3 (bits 31..24) of 5st data object
0x48	RX_BUF_OBJ6_BYTE_0	7:0	RX_OBJ6_0	0	R	Byte 0 (bits 7..0) of 6st data object
0x49	RX_BUF_OBJ6_BYTE_1	7:0	RX_OBJ6_1	0	R	Byte 1 (bits 15..8) of 6st data object
0x4A	RX_BUF_OBJ6_BYTE_2	7:0	RX_OBJ6_2	0	R	Byte 2 (bits 23..16) of 6st data object
0x4B	RX_BUF_OBJ6_BYTE_3	7:0	RX_OBJ6_3	0	R	Byte 3 (bits 31..24) of 6st data object
0x4C	RX_BUF_OBJ7_BYTE_0	7:0	RX_OBJ7_0	0	R	Byte 0 (bits 7..0) of 7st data object
0x4D	RX_BUF_OBJ7_BYTE_1	7:0	RX_OBJ7_1	0	R	Byte 1 (bits 15..8) of 7st data object
0x4E	RX_BUF_OBJ7_BYTE_2	7:0	RX_OBJ7_2	0	R	Byte 2 (bits 23..16) of 7st data object
0x4F	RX_BUF_OBJ7_BYTE_3	7:0	RX_OBJ7_3	0	R	Byte 3 (bits 31..24) of 7st data object
0x50	TX_BUF_FRAME_TYPE	7:6	Reserved	0	R	
		5:4	TX_RETRY_CNT	0	RW	00b: No message retry is required 01b: Automatically retry message transmission once 10b: Automatically retry message transmission twice 11b: Automatically retry message transmission three times
		3	Reserved	0	R	
		2:0	TX_FRAME_TYPE	0	RW	000b: Transmit SOP 001b: Transmit SOP' 010b: Transmit SOP" 011b: Transmit SOP_DBG' 100b: Transmit SOP_DBG'' 101b: Transmit Hard Reset 110b: Transmit Cable Reset 111b: Transmit BIST Carrier Mode 2 (TCPC shall exit the BIST mode no later than tBISTContMode max)
0x51	TX_BYTE_COUNT	7:0	TX_BYTE_COUNT	0	RW	The number of bytes the TCPM will write
0x52	TX_BUF_HEADER_BYTE_0	7:0	TX_HEAD_0	0	RW	Byte 0 (bits 7..0) of message header
0x53	TX_BUF_HEADER_BYTE_1	7:0	TX_HEAD_1	0	RW	Byte 1 (bits 15..8) of message header
0x54	TX_BUF_OBJ1_BYTE_0	7:0	TX_OBJ1_0	0	RW	Byte 0 (bits 7..0) of 1st data object
0x55	TX_BUF_OBJ1_BYTE_1	7:0	TX_OBJ1_1	0	RW	Byte 1 (bits 15..8) of 1st data object
0x56	TX_BUF_OBJ1_BYTE_2	7:0	TX_OBJ1_2	0	RW	Byte 2 (bits 23..16) of 1st data object
0x57	TX_BUF_OBJ1_BYTE_3	7:0	TX_OBJ1_3	0	RW	Byte 3 (bits 31..24) of 1st data object
0x58	TX_BUF_OBJ2_BYTE_0	7:0	TX_OBJ2_0	0	RW	Byte 0 (bits 7..0) of 2st data object
0x59	TX_BUF_OBJ2_BYTE_1	7:0	TX_OBJ2_1	0	RW	Byte 1 (bits 15..8) of 2st data object
0x5A	TX_BUF_OBJ2_BYTE_2	7:0	TX_OBJ2_2	0	RW	Byte 2 (bits 23..16) of 2st data object

0x5B	**TX_BUF_OBJ2_BYTE_3**	7:0	**TX_OBJ2_3**	0	RW	Byte 3 (bits 31..24) of 2st data object
0x5C	**TX_BUF_OBJ3_BYTE_0**	7:0	**TX_OBJ3_0**	0	RW	Byte 0 (bits 7..0) of 3st data object
0x5D	**TX_BUF_OBJ3_BYTE_1**	7:0	**TX_OBJ3_1**	0	RW	Byte 1 (bits 15..8) of 3st data object
0x5E	**TX_BUF_OBJ3_BYTE_2**	7:0	**TX_OBJ3_2**	0	RW	Byte 2 (bits 23..16) of 3st data object
0x5F	**TX_BUF_OBJ3_BYTE_3**	7:0	**TX_OBJ3_3**	0	RW	Byte 3 (bits 31..24) of 3st data object
0x60	**TX_BUF_OBJ4_BYTE_0**	7:0	**TX_OBJ4_0**	0	RW	Byte 0 (bits 7..0) of 4st data object
0x61	**TX_BUF_OBJ4_BYTE_1**	7:0	**TX_OBJ4_1**	0	RW	Byte 1 (bits 15..8) of 4st data object
0x62	**TX_BUF_OBJ4_BYTE_2**	7:0	**TX_OBJ4_2**	0	RW	Byte 2 (bits 23..16) of 4st data object
0x63	**TX_BUF_OBJ4_BYTE_3**	7:0	**TX_OBJ4_3**	0	RW	Byte 3 (bits 31..24) of 4st data object
0x64	**TX_BUF_OBJ5_BYTE_0**	7:0	**TX_OBJ5_0**	0	RW	Byte 0 (bits 7..0) of 5st data object
0x65	**TX_BUF_OBJ5_BYTE_1**	7:0	**TX_OBJ5_1**	0	RW	Byte 1 (bits 15..8) of 5st data object
0x66	**TX_BUF_OBJ5_BYTE_2**	7:0	**TX_OBJ5_2**	0	RW	Byte 2 (bits 23..16) of 5st data object
0x67	**TX_BUF_OBJ5_BYTE_3**	7:0	**TX_OBJ5_3**	0	RW	Byte 3 (bits 31..24) of 5st data object
0x68	**TX_BUF_OBJ6_BYTE_0**	7:0	**TX_OBJ6_0**	0	RW	Byte 0 (bits 7..0) of 6st data object
0x69	**TX_BUF_OBJ6_BYTE_1**	7:0	**TX_OBJ6_1**	0	RW	Byte 1 (bits 15..8) of 6st data object
0x6A	**TX_BUF_OBJ6_BYTE_2**	7:0	**TX_OBJ6_2**	0	RW	Byte 2 (bits 23..16) of 6st data object
0x6B	**TX_BUF_OBJ6_BYTE_3**	7:0	**TX_OBJ6_3**	0	RW	Byte 3 (bits 31..24) of 6st data object
0x6C	**TX_BUF_OBJ7_BYTE_0**	7:0	**TX_OBJ7_0**	0	RW	Byte 0 (bits 7..0) of 7st data object
0x6D	**TX_BUF_OBJ7_BYTE_1**	7:0	**TX_OBJ7_1**	0	RW	Byte 1 (bits 15..8) of 7st data object
0x6E	**TX_BUF_OBJ7_BYTE_2**	7:0	**TX_OBJ7_2**	0	RW	Byte 2 (bits 23..16) of 7st data object
0x6F	**TX_BUF_OBJ7_BYTE_3**	7:0	**TX_OBJ7_3**	0	RW	Byte 3 (bits 31..24) of 7st data object
0x70	**GPIO_STATUS**	7:1	**Reserved**	0	R	
		0	**GPIO0_I**	0	R	GPIO input (for DFN 10-pin package only)
0x71	**CONFIG_GPIO0**	7	**GPIO0_PU_EN**	0	RW	1: pull-up enable (for DFN 10-pin package only)
		6	**Reserved**	0	R	
		5	**GPIO0_F_ALERT**	0	RW	1: Enable falling interrupt (for DFN 10-pin package only)
		4	**GPIO0_R_ALERT**	0	RW	1: Enable rising interrupt (for DFN 10-pin package only)
		3	**GPIO0_O**	0	RW	GPIO output (for DFN 10-pin package only)
		2	**GPIO0_DS**	0	RW	0: Low-drive, 1: High-drive. (for DFN 10-pin package only)
		1	**GPIO0_OE**	0	RW	output enable (for DFN 10-pin package only)
		0	**GPIO0_OD_N**	0	RW	0:open-drain, 1:push-pull (for DFN 10-pin package only)
0x90		7:6	**LIGHT_LOAD[1:0]**	00	RW	OVP occurs and discharge strength control 2'b00-> no discharge 2'b01-> discharge 5mA 2'b10-> discharge 10mA 2'b11-> discharge 15mA

		5	**DISCHARGE_EN**	0	RW	OVP occurs and discharge path turn-on 1'b1-> no discharge 1'b1-> discharge
		4	**BMCIO_LPRPRD**	0	RW	low power mode enable 1'b0 -> fake RD 1'b1 -> fake RP
		3	**BMCIO_LPEN**	0	RW	low power mode enable 1'b0 -> normal 1'b1 -> low power
		2	**BMCIO_BG_EN**	1	RW	BMCIO BG & V2I enable
		1	**VBUS_DETEN**	1	RW	VBUS detection enable 1'b0 -> Measure off 1'b1 -> operation
		0	**BMCIO_OSC_EN**	1	RW	1: Enable OSC
0x91		7	**VBUS_MEASURE_EN**	0	RW	VBUS detection enable 1'b0 -> Measure off 1'b1 -> operation
		6	**VBUS_BAND**	0	RW	VBUS voltage range selection 1'b0 -> 5V < VBUS detection range < 10V 1'b1 -> 10V < VBUS detection range < 20V
		5	**VBUS_MEASURE_TIME**	0	RW	0: 26us/step 1: 52us/step
		4	**VBUS_COMP**	0	R	VBUS measurement flag 1'b0 -> VBUS over specified voltage 1'b1 -> VBUS under specified voltage

		3:0	**VBUS_CON[3:0]**	0	R	VBUS reference voltage selection VBUS=Vref_VBUS*10*(VBUS_BAND+1) 4'b0000 -> Vref_VBUS=0.5V 4'b0001 -> Vref_VBUS=0.55V 4'b0010 -> Vref_VBUS=0.6V 4'b0011 -> Vref_VBUS=0.65V 4'b0100 -> Vref_VBUS=0.7V 4'b0101 -> Vref_VBUS=0.75V 4'b0110 -> Vref_VBUS=0.8V 4'b0111 -> Vref_VBUS=0.85V 4'b1000 -> Vref_VBUS=0.9V 4'b1001 -> Vref_VBUS=0.95V 4'b1010 -> Vref_VBUS=1.0V 4'b1011 -> Vref_VBUS=1.05V 4'b1100 -> Vref_VBUS=1.1V 4'b1101 -> Vref_VBUS=1.15V 4'b1110 -> Vref_VBUS=1.2V 4'b1111 -> Vref_VBUS=1.25V
0x92		7:0	**Reserved**	0	R	
0x93		7:5	**BMCIO_VCONOCP[2:0]**	100	RW	Over-current control selection 3'b000 -> Current level=200mA 3'b001 -> Current level=300mA 3'b010 -> Current level=400mA 3'b011 -> Current level=500mA 3'b100 -> Current level=600mA 3'b101 -> Current level=700mA 3'b110 -> Current level=800mA 3'b111 -> Current level=VCONN source limiting (Un-bounded)
		4:1	**Reserved**	0	R	
		0	**BMCIO_RXDZSEL**	0	RW	RX data decision threshold selection 1'b0 -> 0.5~0.6 1'b1 -> 0.55

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.500	0.600	0.020	0.024
A1	0.170	0.230	0.007	0.009
b	0.240	0.300	0.009	0.012
D	1.290	1.390	0.051	0.055
D1	0.800		0.031	
E	1.290	1.390	0.051	0.055
E1	0.800		0.031	
e	0.400		0.016	

Datasheet Revision History

Version	Date	Item	Description
P00			First Edition