# PCB Layout guidelines for HDFIFO CYF00**V

**Question:** What are the PCB layout guidelines to be followed for HDFIFO?

**Answer:** HDFIFO is a high speed device which can be operated up to 133MHz. The following layout guidelines have to be followed while designing the PCB to achieve good SI and to avoid costly layout changes late in the design cycle.

The recommendations are given for power, data and control, clock and JTAG pins.

1) All the Data input pins (D) should have a 50 ohm series termination close to the FPGA side.

2) All the data output pins(Q) should have a 50ohm series resistor close to HDFIFO. The series termination at the source end basically helps to reduce the ringing effect due to improper impedance matching at the source end. In general, all input control signals should have a source termination at the FPGA side.

3) WCLK/RCLK, being high speed inputs to the HDFIFO, should have a 50 ohm series termination close to the FPGA side. An optional capacitor to ground can be put to control clock delay, rise and fall times on board. The capacitor value can be selected depending on the how much delay has to be added to compensate board flight time to match both the read and write clocks.

3) Flag outputs being outputs from HDFIFO, have to be terminated using 50 ohm termination close to FPGA.

4)JTAG pins:
TMS/TRST -Point-to-Point connection with a pull-down resistor on the line.(R=?). TCK, TDI, TDO should be point to point connections.

5) Power pins.
Power supply pins should have enough decoupling capacitors to bypass the high frequency coupled noise. Bulk capacitors are needd on the power pins to source the extra charge required during high speed switching of the device outputs.

VCCIO - place two 47uF bulk close to the device and a .01uF de-coupling one for each pin. Place decoupling capacitors as close to the power pins as possible - recommended right on the power pin.

VCC1- 47uF bulk close to the device and a .01uF de-coupling one for each pin.

VCC2- connect to 1.5V. Special care has to be taken for this supply to ensue these power pins are as noise free as possible.

Vref - Use 10uF and 0.1uF de-coupling capacitors. Place .1uF de-coupling close to the pin. If common supply used, have a common 10uF and individual 0.1uF decoupling capacitors

6) Pin U6- DNU -Connect a weak pull down.