Advantages of 65 nm Technology over 90 nm Technology QDR® Family of SRAMs

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Application Note Abstract

This application note outlines the advantages of the 65 nm technology QDR® SRAMs over the 90 nm technology SRAM devices.

Introduction

The 65 nm technology QDR family of devices offers significant advantages over the 90 nm technology family. This application note describes these advantages and provides guidelines to migrate from 90 nm to 65 nm devices.

Overview

The following table highlights the features and differences between the 65 nm and 90 nm QDR device families.

Table 1. Features of 65 nm and 90 nm QDR Devices

		QDR II	DDRII	DDRII SIO	QDRII+	QDRII+	DDRII+	DDRII+	DDRII+ SIO	DDRII+ SIO
Read Latency- 90 nm and 65 nm		1.5	1.5	1.5	2	2.5	2	2.5	2	2.5
Write Latency-90 nm and 65 nm		1	1	1	1	1	1	1	1	1
Frequency (Burst of 4)	65 nm	333 MHz	333 MHz	N/A	450 MHz	550 MHz	450 MHz	550 MHz	N/A	N/A
	90 nm	300 MHz	300 MHz	N/A	400 MHz	450 MHz	400 MHz	450 MHz	N/A	N/A
Frequency (Burst of 2)	65 nm	333 MHz	333 MHz	333 MHz	333 MHz	333 MHz	450 MHz	550 MHz	450 MHz	550 MHz
	90 nm	300 MHz	300 MHz	300 MHz	300 MHz	300 MHz	400 MHz	450 MHz	400 MHz	450 MHz
Density	65 nm	18Mb, 36Mb, 72Mb, & 144Mb								
	90 nm	18Mb, 36Mb, 72Mb								
Organization (Bus Width) - 90 nm and 65 nm		X9, X18, X36								
VDD (Core) - 90 nm and 65 nm		1.8V +/-0.1V								
VDDQ (I/O) - 90 nm and 65 nm		1.8V+/-0.1V or 1.5V+/-0.1V								
SER (FIT/Mb) (Refer to *Note*]	Logical Single Bit Upset (LSBU) -65 nm	216 @ 85 degree celsius								
	Logical Single Bit Upset (LSBU) -90 nm	368 @ 85 degree celsius								
	Logical Multi Bit Upset (LMBU) -90 nm and 65 nm	0.01@ 85 degree celsius								
SEL (FIT/Dev) -90 nm and 65 nm		0.1 @ 85 degree celsius								
Clock generation and Lock Time	Phase Locked Loop (PLL) -65 nm	Yes (PLL Lock time) :20us								
	Delay Locked Loop (DLL) -90 nm	Yes(DLL lock time) : 1024 clock cycles for QDRII/DDRII and 2048 clock cycles for the QDRII+/DDRII+								
Input Clocks for Output Data (C,C#)--90 nm and 65 nm		Yes				No				
Echo Clocks (CQ, CQ#)		Yes								
PKG--90 nm and 65 nm		165 Ball FBGA								
QVLD--90 nm and 65 nm		No				Yes				
ODT-- Applicable in 65 nm only. Not supported in 90 nm		No				Yes				

Note: For more details refer to Application Note AN54908, *Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates*

Advantages of 65 nm Technology Devices

Faster Operating Frequencies

The 65 nm technology devices are capable of operating at higher operating frequencies of 550 MHz and total data rates up to 80 Gbps. This results in significant bandwidth improvement (~23%) over the 90 nm QDR family of devices, which can operate upto a maximum frequency of 450 MHz. This improvement in operating frequency satisfies the higher banwidth requirements in networking application.

Lower Power Consumption

The 65 nm technology QDR devices have lower power consumption than the equivalent 90 nm technology QDR devices. The power saving is ~30% at worst case condition.

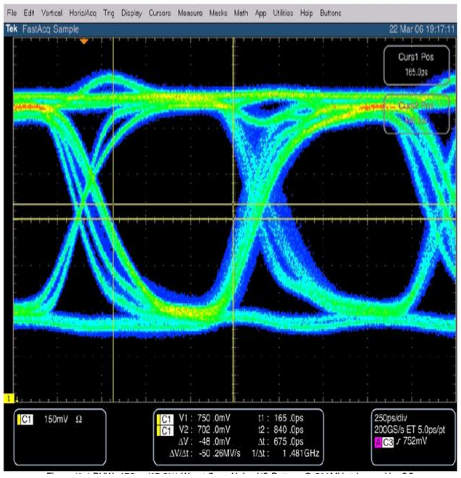
Improved Data Valid Window

The data valid window for the outputs of 65 nm QDR devices is about 21% wider than the 90 nm QDR devices. This improvement is achieved using a low jitter clock generating PLL (Phase Locked Loop) as opposed to a DLL (Delay Locked Loop) in the 90 nm technology device. The PLL filters the incoming jitter and corrects any duty cycle distortion for the inputs. The improved data valid window helps achieve better timing margins for the 65 nm technology device.

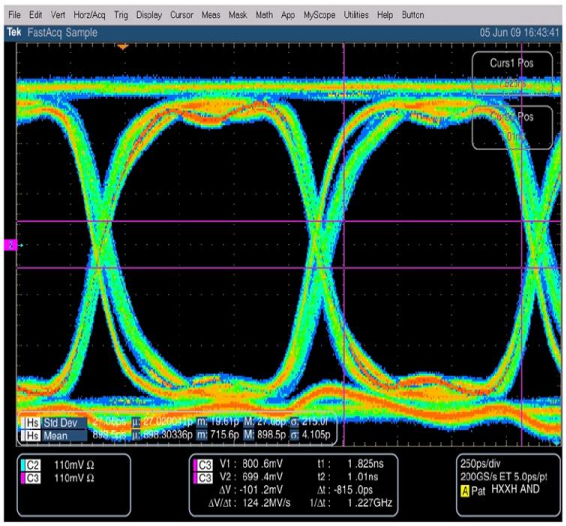
Figure 1 compares the data valid window of a 90 nm QDRII+ and a 65 nm QDRII+ device at 500 MHz. As shown in the figure, there is a significant improvement (~21%) in the data window for the 65nm QDRII+ devices.

Figure 1. Comparison of Data Valid Window

Ram 9 (90nm) QDRII+
DVW=675ps Worst Case Noise I/O Pattern @ 500MHz triggered by CQ



65nm QDRII+
DVW=815ps Worst Case Noise I/O Pattern @ 500MHz triggered by CQ



Improved Signal Integrity

The 65 nm technology QDRII+/DDRII+ devices have on-die termination for inputs such as data inputs, byte write signals, and input clocks (K/Kb). This feature is not present in the 90 nm technology QDRII+/DDRII+ devices. On-die termination eliminates the need for external termination resistors thereby reducing the cost and power consumed by external resistors. It also improves signal integrity, simplifies board routing, and reduces the board area. For more details on on-die termination, refer to application note AN42468, *On-Die Termination for QDRII+/DDRII+ SRAMs.*

Lower Input and Output Capcitances

Compared with the 90 nm predecessors, the 65 nm QDR family of SRAMs has lower input and output capacitance by 60 percent. This translates to lower return loss and therefore lower reflections or discontinuity at the inputs. A lower capacitance also results in lower AC power consumption at the input.

Design Changes to Migrate from 90 nm to 65 nm Family

The 65 nm QDR family of devices provides higher speed path for most applications. You can implement certain design changes in your existing designs to enable seamless transition from 90 nm to 65 nm QDR devices.

Board Changes

For higher performance, the board should be designed to perform at speeds up to 550 MHz.

Host Controller Changes

Echo clocks need to be used to latch the read data. If the existing design uses a K or C clock for the read data capture, then the host controller design must be changed to use echo clocks because this yields better timing margins for higher frequencies.

The memory controller software should also be modified to accommodate the PLL lock time of 20 µs in the 65 nm technology device compared to the DLL lock time of 1024 clock cycles for the QDRII/DDRII and 2048 clock cycles for the QDRII+/DDRII+ devices in the 90 nm family.

Pinout Changes

In the QDRII device, the pins P6 and R6 are used as C and C# clocks. In the 90 nm technology QDRII+ devices, P6 is used as the QVLD pin and R6 is a NC (No connect).

In the 65 nm technology node, the QDRII+ devices are offered in two flavors: ODT enabled and ODT disabled devices. No change needs to be made when migrating from a 90 nm QDRII+ device to a 65 nm technology ODT disabled QDRII+ device as the pinouts are identical.

However, when migrating from a 90 nm technology QDRII+ device to a 65 nm technology ODT enabled device, the Ball R6 is an ODT pin instead of a NC (No Connect).

The ODT pin is used to select high range or low range of impedance for the inputs.

Summary

The 65 nm technology QDR family of devices provides the ability to achieve high performance and bandwidth with few changes to existing boards. It also has the capability to create new designs. This is possible by designing boards and host controllers to meet both support high performance of up to 550 MHz and 80 Gbps bandwidth in the next generations without any changes to the existing boards or host controllers.

Document History

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