Reference Schematic Design Recommendation for QDR®-DDR II/II+/Xtreme SRAMs – KBA84386

Question: Where can I get a recommended reference schematic design for QDR-DDR II/II+/Xtreme products?

Answer: This article provides reference schematics for QDR-DDR II/II+/Xtreme devices. You can use these schematics, which are derived from an internal characterization board, as examples for your designs. However, you must perform signal integrity simulations before doing so.

Refer to the application note *AN4065 - QDR™-II, QDR-II+, DDR-II, and DDR-II+ Design Guide* for different termination schemes, designs, and signal integrity guidelines. For more information on the QDR-DDR II/II+/Xtreme SRAMs, refer to the respective datasheets in the Sync SRAM category.

Reference Schematic for QDR-DDR II/II+/Xtreme SRAMs (from internal characterization board)

Figure 1. (a) QDRII/II+/II+Xtreme-DDRII/II+/II+Xtreme (Non ODT) Reference Schematic

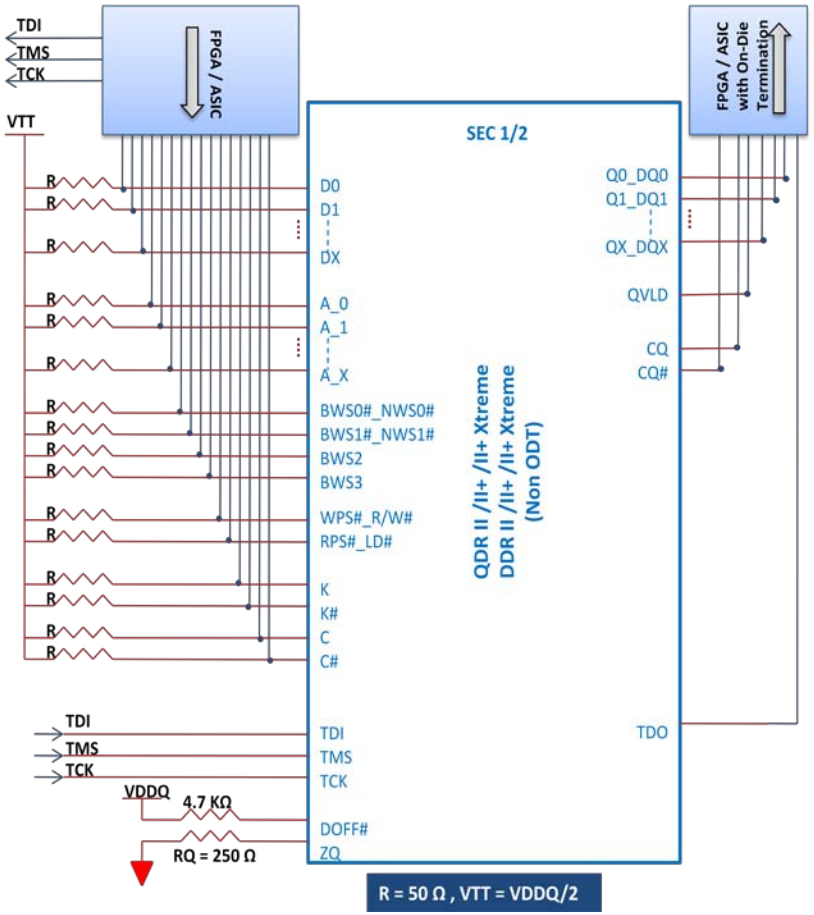


Figure 1. (b) QDRII/II+/II+Xtreme-DDRII/II+/II+Xtreme (ODT) Reference Schematic

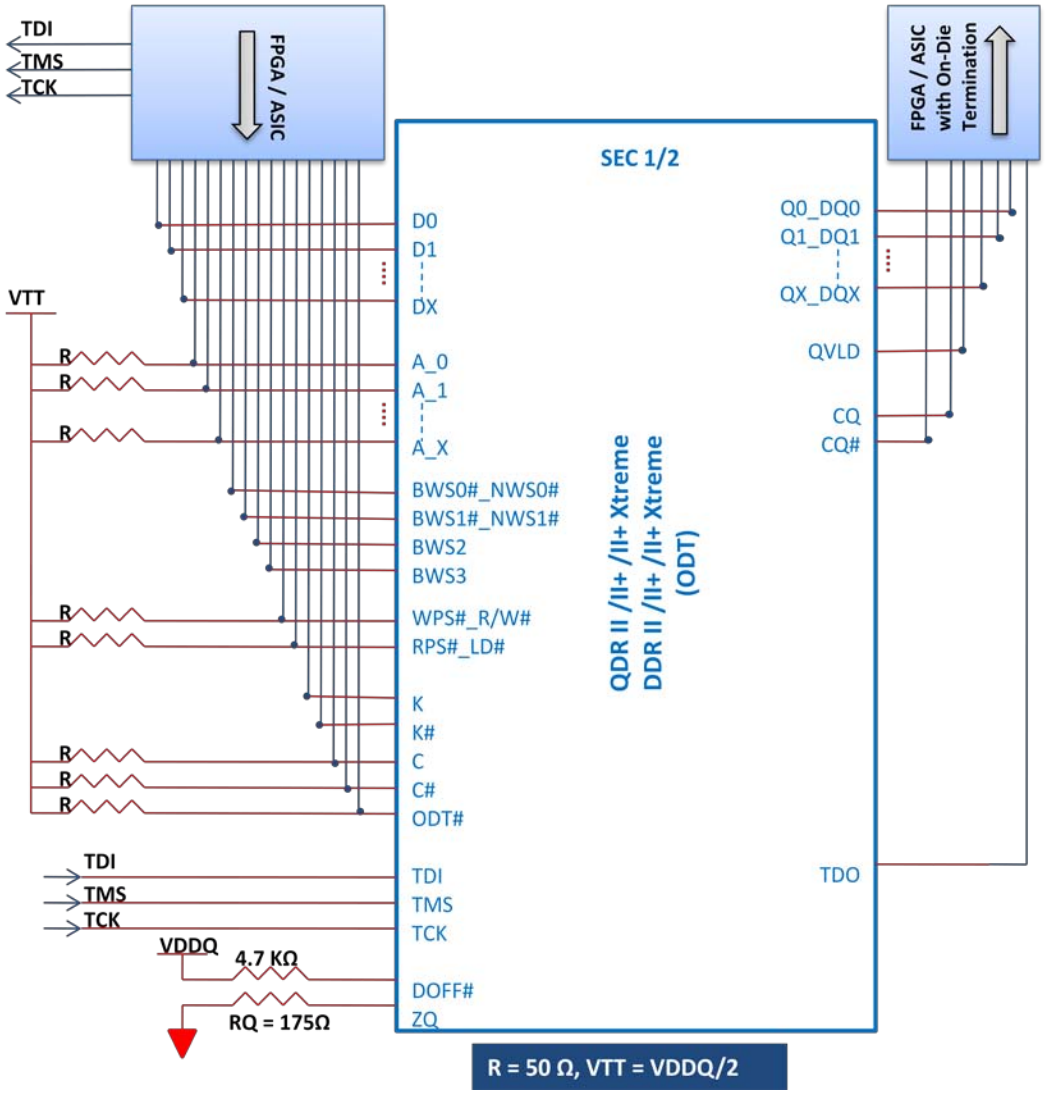
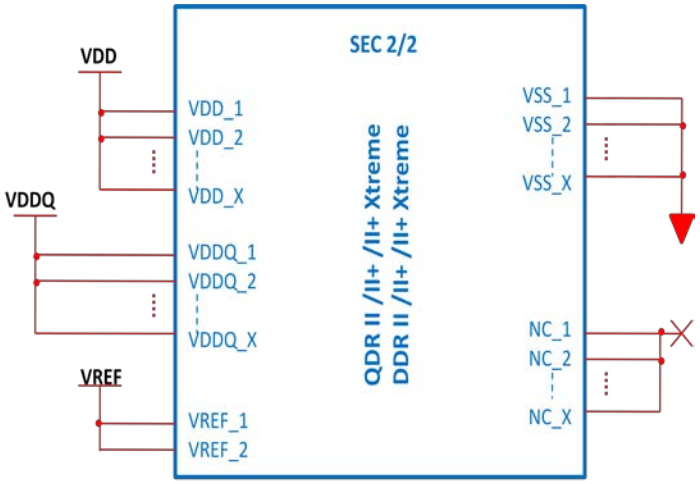


Figure 2. QDRII/II+/II+Xtreme-DDRII/II+/II+Xtreme (Supply Pins) Reference Schematic



Assumptions

- The reference schematics provided in the previous section are from an internal characterization board. Cypress recommends that you perform signal integrity simulations with specific board conditions before finalizing your design.
- Figure 1 (a) and (b) are the reference schematics for all Non on-die termination (ODT) and ODT QDR-DDR II/II+/Xtreme SRAMs respectively. For example, if the part is an x18 device, then the data pin notation $D_{[x:0]}$ will be interpreted as $D_{[17:0]}$.
- QDRII+/II+Xtreme-DDRII+/II+Xtreme devices do not have the input clocks C and C#.
- Non ODT QDRII+/II+Xtreme-DDRII/II+/II+Xtreme devices do not contain the ODT pin.
- ODT devices have an ODT feature for Data inputs ($D_{[x:0]}$), Byte Write Selects ($BWS_{[x:0]}$), and Input Clocks (K and K#). Hence, there is no termination for the $D_{[x:0]}$, $BWS_{[x:0]}$, K, and K# pins shown in Figure 1 (b). Refer to the application note *AN42468 - On-Die Termination for QDR™II+/DDRII+ SRAMs* that discusses the ODT scheme, implementation, advantages, and power calculation for the QDRII+ and DDRII+ family of Synchronous SRAMs on 65-nm technology devices.
- Data output ($Q_{[x:0]}$) and Echo clock (CQ/CQ#) signals drive FPGA/ASIC without termination, considering the inputs of the FPGA/ASIC that supports ODT. In the case of FPGA/ASIC without ODT, Cypress recommends that you terminate (pull-up to V_{TT}) Data output ($Q_{[x:0]}$) and Echo clock (CQ/CQ#) signals to reduce signal integrity issues.
- The value of the termination resistor (R) is 50 Ω, because most designs have a trace characteristic impedance of 50 Ω. The termination resistor value must be equal to the characteristic impedance of the trace.
- An external resistor, RQ, must be connected between the ZQ pin on the SRAM and V_{SS} to allow the SRAM to adjust its output driver impedance. The value of RQ must be five times the value of the intended line impedance driven by the SRAM. As a result, the value of RQ is 250 Ω to match the output impedance of 50 Ω in Figure 1 (a). The acceptable range of RQ that guarantees impedance matching with a tolerance of ±15% is between 175 Ω and 350 Ω, with V_{DDQ} = 1.5V. The output impedance is adjusted every 1024 cycles upon power-up to account for drifts in supply voltage and temperature.
- The RQ is 175Ω in Figure 1 (b) considering the input impedance and ODT value of memory is 50Ω, ODT pin is LOW and output impedance is 35Ω. If the output impedance is 50Ω then it is recommended to use a 15Ω resistor in series with the output driver to match the trace impedance of 50Ω.
- Keep termination resistors as close to the device as possible to reduce the stub length, and thereby, reduce reflections.

Decoupling Capacitor Recommendations for Power Supply Pins

- Decoupling capacitors on power-supply pins play a significant role in filtering noise in the power supply.
- Cypress recommends that you place the decoupling capacitors close to the memory devices for best results.
- The following decoupling capacitor recommendations are from an internal characterization board:

Figure 3. Decoupling Capacitor Recommendation for V_{DD}

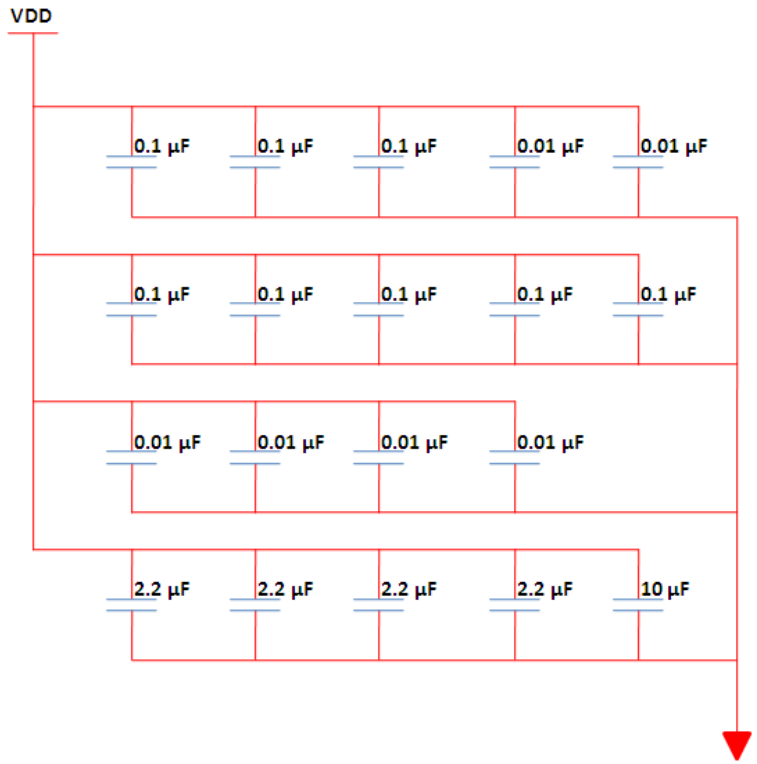
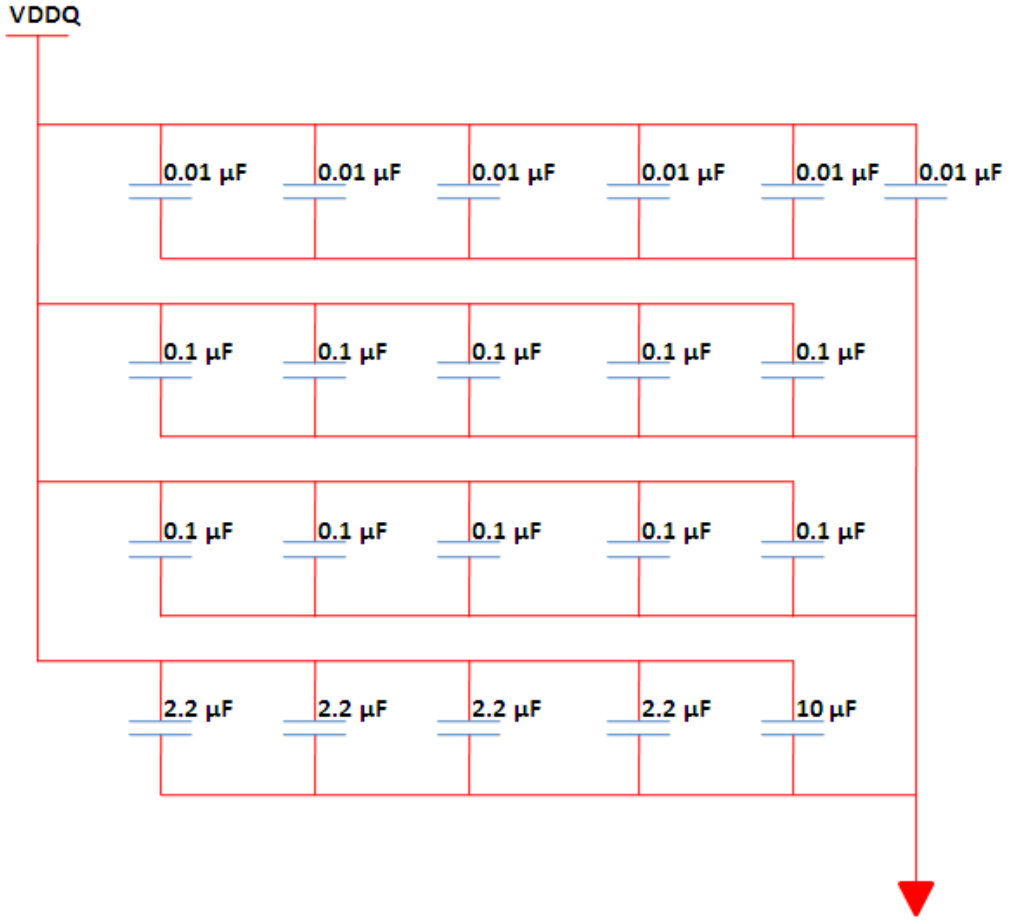


Figure 4. Decoupling Capacitor Recommendation for V_{DDQ}



Note Refer to the datasheets for V_{DDQ} value.

Figure 5. Decoupling Capacitor Recommendation for V_{TT}

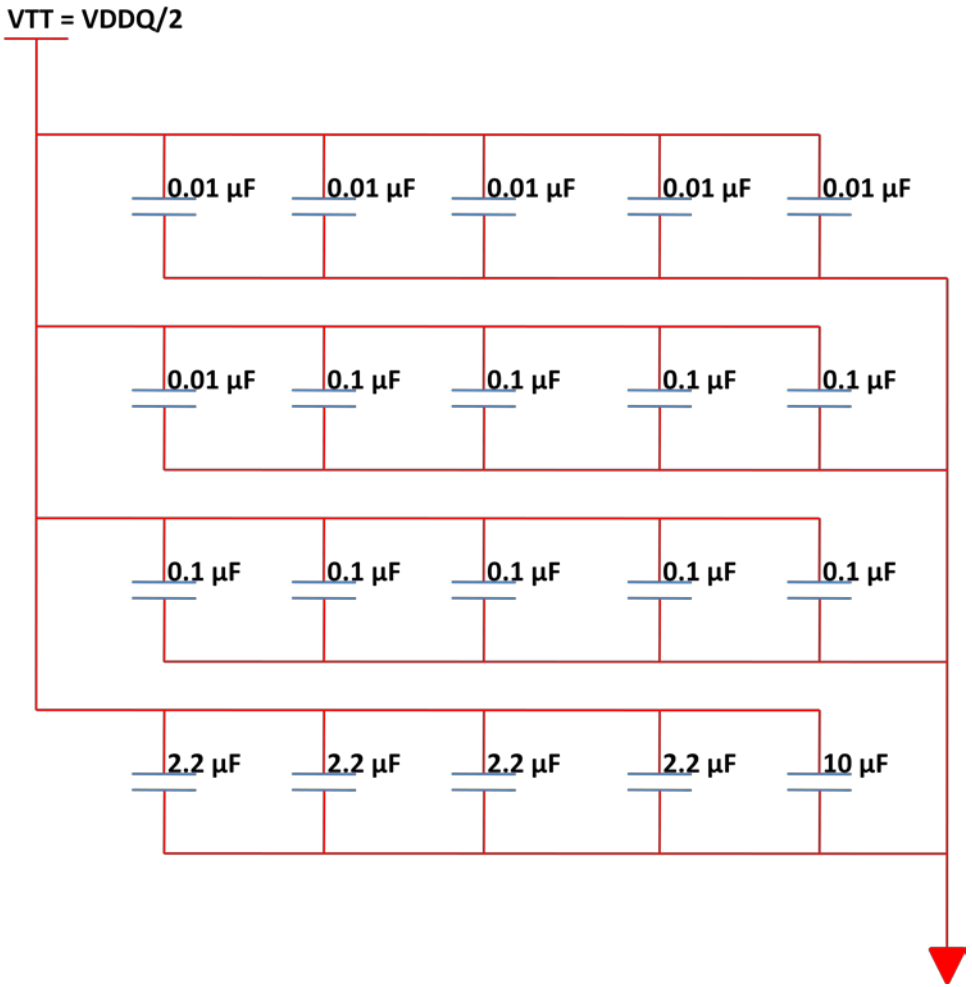
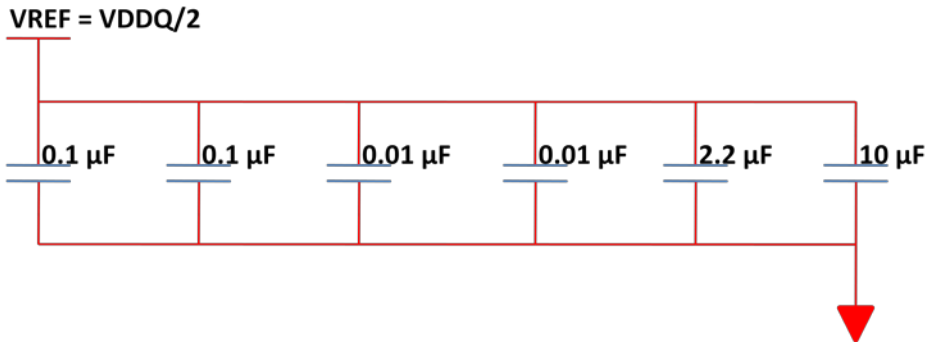


Figure 6. Decoupling Capacitor Recommendation for V_{REF}



If you face any issue while creating your design or if you would like Cypress to do a schematic review, create a technical support case at www.cypress.com.