AN6081

Interfacing 90-nm Cypress Asynchronous SRAMs in Legacy Systems

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Associated Project: No
Related Application Notes: None

AN6081 describes the potential issues faced when using the new-generation 90-nm Cypress SRAMs in applications that rely on legacy 5-V processors. This application note also discusses the troubleshooting methods on output voltage issues when migrating to the new devices. Usage recommendations when you opt to use Cypress SRAMs in such applications are also provided.

Introduction

Applications have evolved from using 5-V power supply to using 3-V and 1.8-V supply. Cypress's Asynchronous SRAM devices operate over all of these voltage ranges. This application note discusses a case of incompatibility between output voltage thresholds of 90-nm SRAM devices and input voltage thresholds of processors or controllers that are interfaced with these SRAMs in legacy 5-V systems. A recommendation to use an old generation Cypress SRAM is given to match the requirements in such cases.

Note: The terms "Processor(s)" and "Controller(s)" are used interchangeably in this document.

Logic Levels and Noise Margin

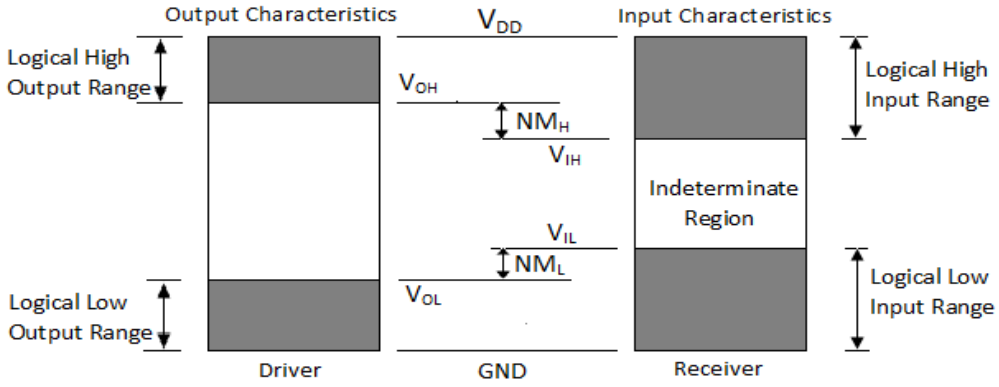
In digital electronics, a logic level is one of two possible signal states. Four parameters define the logic levels for a digital logic family: V_{IL}, V_{IH}, V_{OL}, and V_{OH}.

- V_{IL} defines the maximum voltage level that will be interpreted as a '0' by a digital input.
- V_{IH} defines the minimum voltage level that will be interpreted as a '1' by a digital input.
- V_{OL} defines the guaranteed maximum voltage level that will appear on a digital output set to '0'.
- V_{OH} defines the guaranteed minimum voltage level that will appear on a digital output set to '1'.

Noise margin (NM) is defined as the difference between the valid logic output voltage of the driver IC and the valid logic input voltage of the receiver IC. These are the expressions for NM of devices.

- NM_H (Output high) = V_{OH} [driver] - V_{IH} [receiver]
- NM_L (Output low) = V_{IL} [receiver] - V_{OL} [driver]

Figure 1: Noise Margin



The noise tolerance of a circuit is proportional to the NM. A higher margin translates to better noise immunity. Negative NM numbers indicate incompatibility.

Logic levels and noise margin numbers for some commonly used I/O standards are shown in the following table.

Table 1: Logic-Level Voltages of Common I/O Standards and Corresponding Noise Margin

I/O Standard	Logic Levels HIGH (V)		NM_H	Logic Levels LOW (V)		NM_L
	V_{OH}	V_{IH}		V_{OL}	V_{IL}	
TTL 5 V	2.4	2.0	0.4	0.4	0.8	0.4
CMOS 5 V	4.4	3.5	0.9	0.4	0.7	0.3
CMOS 2.5 V	2.0	1.7	0.3	0.4	0.7	0.3
CMOS 1.8 V	1.35	1.2	0.15	0.45	0.63	0.18
TTL 3.3V	2.4	2	0.4	0.4	0.8	0.4
CMOS 3.3V	3.1	2	1.1	0.2	0.8	0.6

The following section discusses the V_{OH} compatibility issues of Cypress asynchronous SRAM devices when they are interfaced with an external processor.

Measured versus Spec V_{OH} of Cypress Asynchronous SRAM

Cypress's new generation asynchronous SRAM devices are manufactured in a 90-nm process technology with high standards for power and speed. These devices, offered in 1.8-V, 3.3-V, and 5-V ranges are pin-compatible with the old-generation (250-nm and 350-nm technology) devices.

Figure 2 shows the difference in actual V_{OH} levels of asynchronous SRAM devices of different generations. While all of them meet the industry-standard transistor-transistor logic (TTL) V_{OH} specification of 2.4 V, the older devices have a higher voltage swing and, therefore, can drive outputs in the range of 4 V to 5 V. As a result, their measured V_{OH} exceeds 4 V. On the other hand, the new-generation Cypress SRAMs have a reduced voltage swing on their outputs of ~3 V to 3.3 V. Some of the 5-V legacy processors require a complementary metal-oxide-semiconductor (CMOS) V_{IH} level of 3.5 V, while others may require a TTL V_{IH} level of 2.0 V. The choice of Cypress SRAM for the application depends on the V_{IH} spec of the processor, which is used to interface the SRAM. Even though the devices are pin-compatible, it is advisable to check for the V_{IH} specification of the processor when choosing the Cypress SRAM.

Table 2 shows the driver and receiver configurations of Cypress's asynchronous SRAM devices and external processors. The NM_H and NM_L values are positive for all the configurations except when Cypress's new-generation SRAM drives a legacy processor. This is shown in Figure 2.

The old generation SRAM devices are suitable for applications using legacy processors with a CMOS V_{IH} requirement of 3.5 V because of their higher V_{OH} swing. If the processor has a TTL V_{IH} requirement of 2 V, the new-generation 90-nm Cypress devices would fit.

Note the incompatibility between 90-nm SRAM devices and 5-V CMOS controllers is present only when the SRAM is in driver mode. There is no interfacing issue when the SRAM is in receiver mode.

Figure 2. Voltage Levels of TTL and Legacy I/O Standards

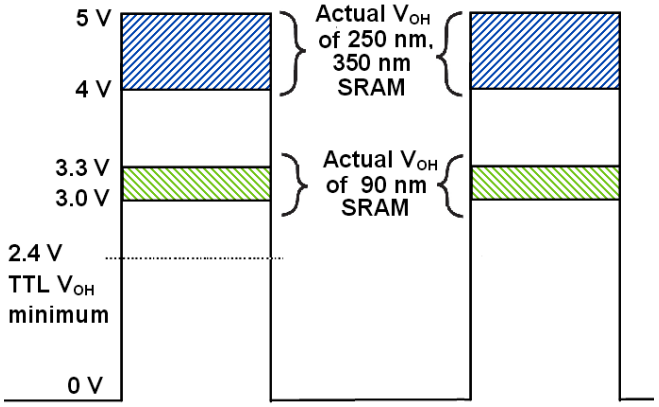
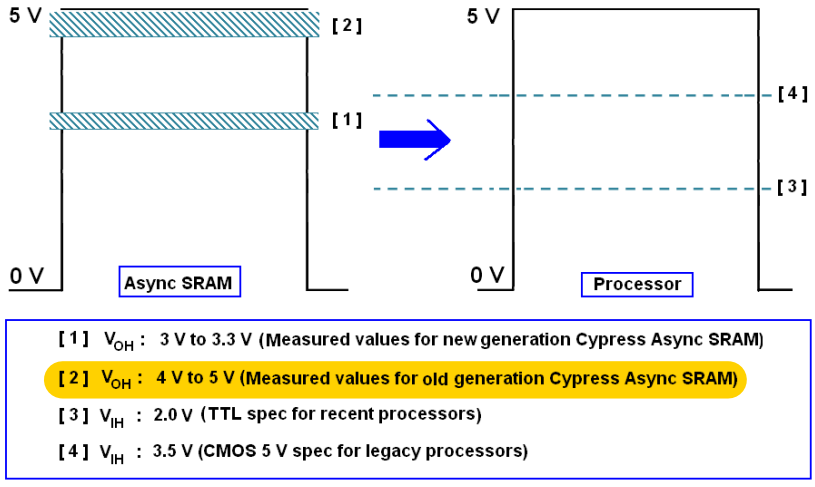


Table 2. NM_H and NM_L Specifications for Four Combinations of Interfacing (Logic-Level in volts)[1]

SL #	Driver Operation			Receiver Operation			NM_H	NM_L	Compatibility
	Driver	$V_{OH\ (MIN)}$	$V_{OL(MAX)}$	Receiver	$V_{IH(MIN)}$	$V_{IL(MAX)}$			
1	Old generation Asynchronous SRAM (250-350 nm TTL compatible)	4.0 (measured value)	0.4	Present-generation processor (TTL compatible)	2.0	0.8	2.0	0.4	✓
				Legacy processor (5 V CMOS compatible)	3.5	1.5	0.5	1.1	✓
2	New generation Asynchronous SRAM (90 nm TTL compatible)	3.0 (measured value)	0.4	Present-generation processor (TTL compatible)	2.0	0.8	1.0	0.4	✓
				Legacy processor (5 V CMOS compatible)	3.5	1.5	-0.5[2]	1.1	×
3	Legacy processor (5 V CMOS compatible)	4.4	0.5	New-generation asynchronous SRAM (90 nm TTL compatible)	2.0[3]	0.8	2.4	0.3	✓
				Old-generation asynchronous SRAM (250-350 nm TTL compatible)					✓
4	Present-generation processor (TTL compatible)	2.4	0.4	New-generation asynchronous SRAM (90 nm TTL compatible)	2.0[3]	0.8	0.4	0.3	✓
				Old-generation asynchronous SRAM (250-350 nm TTL compatible)					✓

Figure 3. V_{OH} and V_{IH} Levels of TTL and 5-V CMOS Legacy Products Respectively (SRAM Acting as a Driving Device)



[1] The measured V_{OH} range of Cypress older generation Asynchronous SRAM devices are in the range of 4 V to 5 V and that of new generation devices is 3 V to 3.3 V. These have been illustrated in Figure 2. The V_{OH} numbers of the Asynchronous SRAM devices used in this table are all actually measured parameters, while all other parameter numbers used in this table are datasheet specified values.

[2] Noise margin is negative, indicating incompatible mode of operation.

[3] In receiver mode, Cypress asynchronous SRAM devices can handle up to 5.5-V input.

Recommendations for System Designers

Carefully observe the datasheet parameters like V_{IH}, V_{IL}, V_{OH} and V_{OL} while choosing devices for legacy systems. Here are recommendations if opting for a Cypress Asynchronous SRAM device.

- Use Cypress 90-nm asynchronous SRAMs with processors that support TTL I/O standards.
- Use older generations of Cypress asynchronous SRAM devices with processors that support 5-V CMOS I/O standards.

Cypress encourages its customers to migrate from older generations of SRAM devices to the new generation of 90-nm SRAM devices in all cases where compatibility is not an issue. However, Cypress will continue to offer and support older-generation products for customers using legacy systems.

The following table lists the part numbers of the 90-nm technology devices and equivalent older technology devices. Kindly check the Product page for currently active parts. If you are unable to find an equivalent part for your application, contact Cypress support.

Table 3. Part Numbers of the 90-nm Technology Devices and Equivalent Older Technology Devices

Density	Memory Organization	90-nm Technology Device	Older Technology Device (250-nm, 350-nm and Older Technology)
Fast Asynchronous SRAMs			
256 Kbit	32 Kb × 8	CY7C199D	CY7C199CN
512 Kbit	32 Kb × 16	CY7C1020D	-
1 Mbit	64 Kb × 16	CY7C1021D	CY7C1021BN
1 Mbit	256 Kb × 4	CY7C106D	CY7C106BN
1 Mbit	256 Kb × 4	CY7C1006D	-
1 Mbit	128 Kb × 8	CY7C109D	-
1 Mbit	128 Kb × 8	CY7C1009D	-
1 Mbit	128 Kb × 8	CY7C1019D	-
1 Mbit	1 Mb × 1	CY7C107D	-
1 Mbit	1 Mb × 1	CY7C1007D	-
4 Mbit	1 Mb × 4	CY7C1046D	-
4 Mbit	256 Kb × 16	CY7C1041D	CY7C1041BN
4 Mbit	512 Kb × 8	CY7C1049D	CY7C1049BN
Micropower Asynchronous SRAMs			
1 Mbit	64 Kb × 16	CY62126ESL	-
1 Mbit	128 Kb × 8	CY62128E	CY62128BN
2 Mbit	128 Kb × 16	CY62136ESL	-
2 Mbit	256 Kb × 8	CY62138F	-
4 Mbit	256 Kb × 16	CY62146E	-
4 Mbit	512 Kb × 8	CY62148E, CY62148ESL	-
8 Mbit	512 Kb × 16	CY62157E, CY62157ESL	-
8 Mbit	1 Mb × 8	CY62158E	-
16 Mbit	1 Mb × 16	CY62167E	-

Document History

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Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	1200303	AJU	06/29/2007	Obtain spec number for application note to be added to spec system. No technical updates.
*A	3104879	AJU	12/07/2010	Updated in new template.
*B	3168780	PRAS	02/10/2011	No technical updates.
*C	3337888	AJU	08/04/2011	Major rewrite. Changed title, added figures, modified table to include density information.
*D	3456705	TAVA	12/06/2011	Updated template. Major rewrite.
*E	3540651	AJU	03/02/2012	Corrected CMOS standard logic levels specs in Table 1 Updated Table 2 with corrected values as in Table 1; added column for 'Compatibility' Major rewrite
*F	3821642	NILE	12/10/2012	Updated Document Title to read as "Interfacing 90-nm Cypress Asynchronous SRAMs in Legacy Systems – AN6081". Added Figure 1 and edited Table 1 under Logic Levels and Noise Margin. Minor Text Edits.
*G	4696959	NILE	03/23/2015	Updated Table 3 to remove pruned devices from the list of Older Technology Device column. Updated template

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