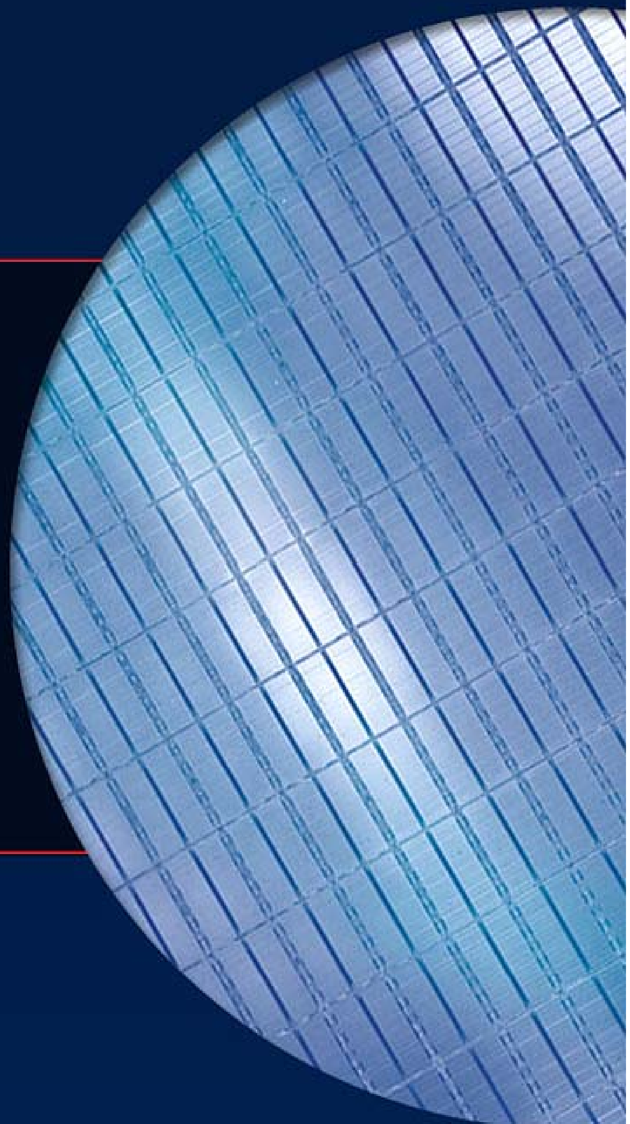
Synchronous SRAMs



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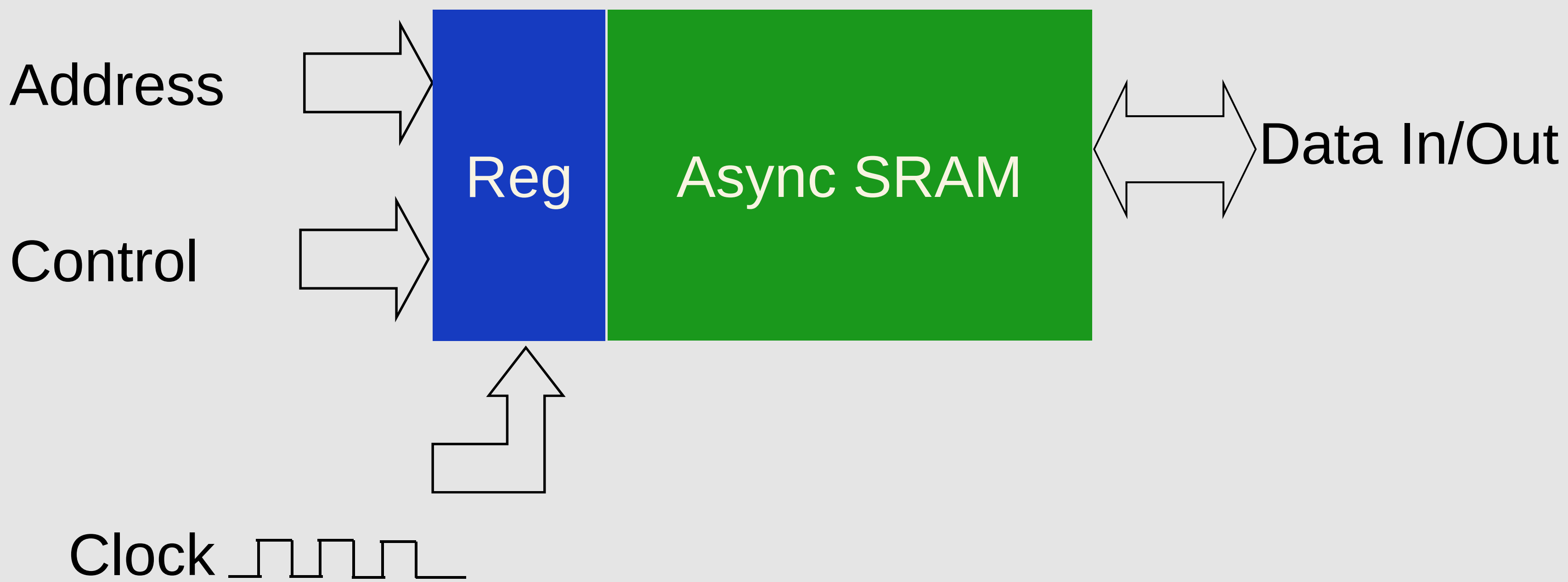
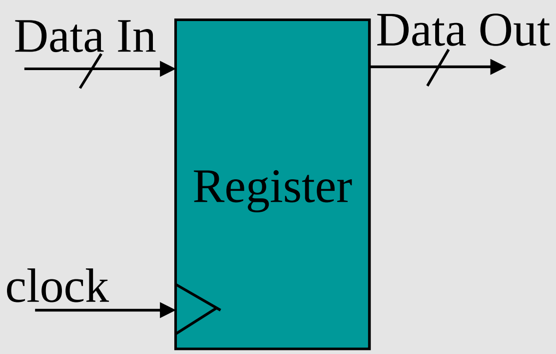
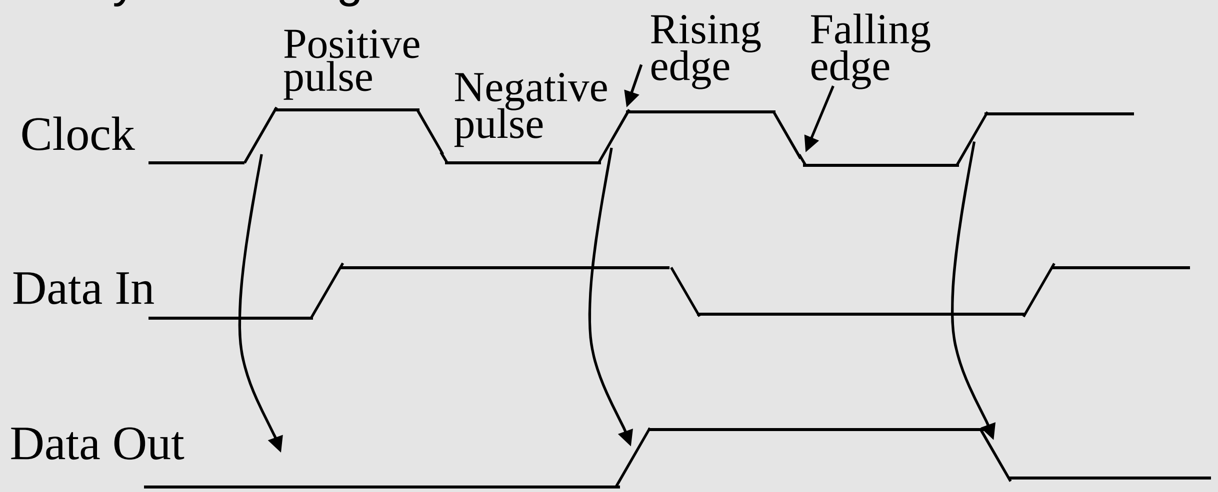
What is an Synchronous SRAM?



Register

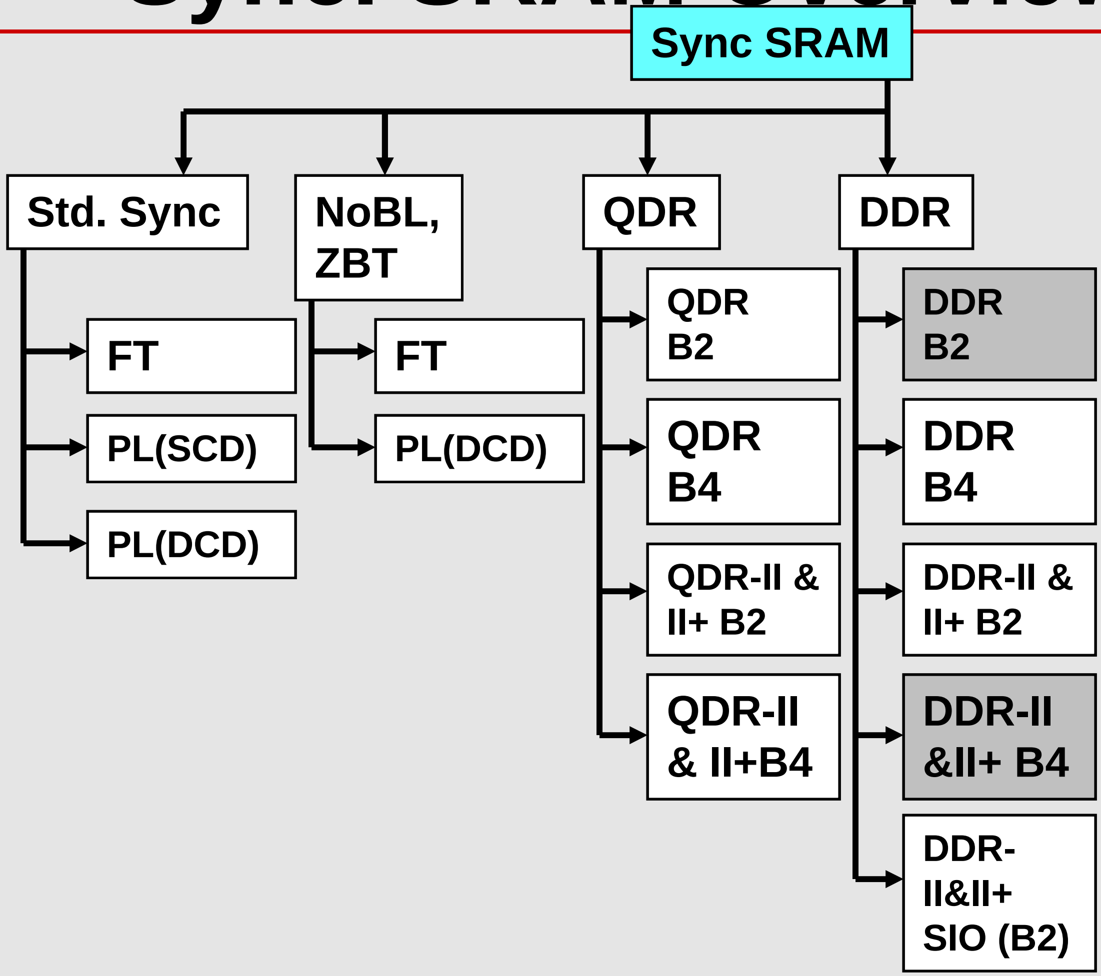
- A Register is an element which is capable of storing binary data.
- A clock is a stream of positive and negative pulses occurring at regular intervals. Positive pulse is always preceded or succeeded by a negative pulse.
- A register can be activated only at the edges of the clock.





- *A combinatorial signal doesn't pass through registers.*
- *A combinatorial logic responds to any change in the inputs. It is not controlled by a clock.*

Sync. SRAM Overview



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Sync. SRAM Overview

•Each Family has numerous options as well:

•**Density & Organization**
- **1 Mb – 72 Mb**
- **X18, X36 (X8, X9, X32, X72)**

• **Speed Grades**
- **400MHz,300MHz,250MHz, 167MHz, …etc.**

• **Timing Options-> eg Read Latency**
- **1.5cycle, 2cycles, 2.5cycles**

• **Burst Options**
- **Interleaved, Linear,Burst 2,Burst4**

• **Core Voltage**
- **3.3V, 2.5V, 1.8V**
-

• **I/O Voltage**
- **LVTTL: 3.3V, 2.5V, 1.8V,1.5V**
- **HSTL, Variable impedance**

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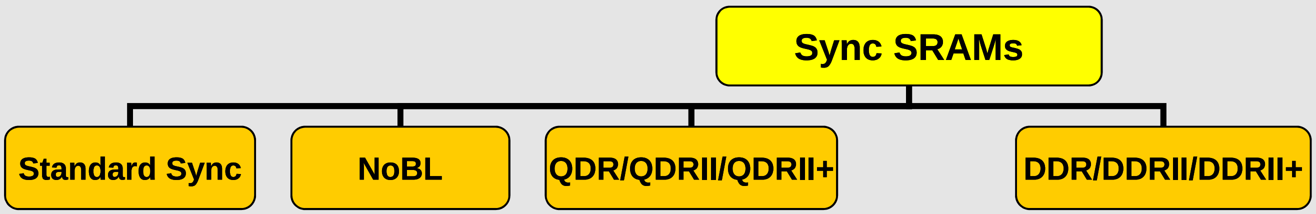
Sync. SRAM Overview

•Each Family has even more options:

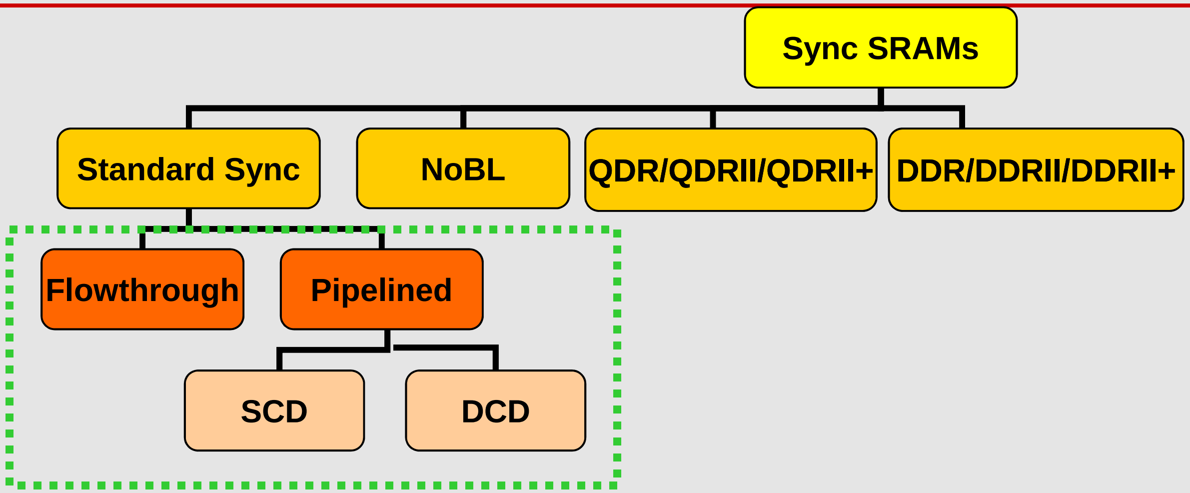
- **Packages**
  - **100 TQFP, 165 fBGA, 119 BGA, 209 BGA**
- **Temperature Ranges**
  - **Commercial, Industrial,Automotive**
- **Chip Enables**
  - **2 CE vs 3 CE options**
  - **Address Locations**
- **JTAG**
  - **With EXTEST, No EXTEST**
- **Names**
  - **NoBL = ZBT = NtRAM = ZBL = ZERO SB = Etc.**
  - **QDR, SigmaRAM**

Sync SRAM Family



- Standard Sync SRAMs
- NoBL SRAMs
- QDR /QDR II/QDRII+
- DDR /DDR II/DDRII+

Standard Sync SRAM



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Synchronous SRAM

Standard Sync SRAM

- Sync SRAM = Async SRAM + (Clock + Registers)
- Common I/O
- Offered in both Pipeline and Flowthrough
  - Single cycle deselect **SCD** (Flowthrough and Pipeline)
  - Double Cycle Deselect **DCD** (Pipeline Only!)
- Best for either dominated Reads **or** Writes

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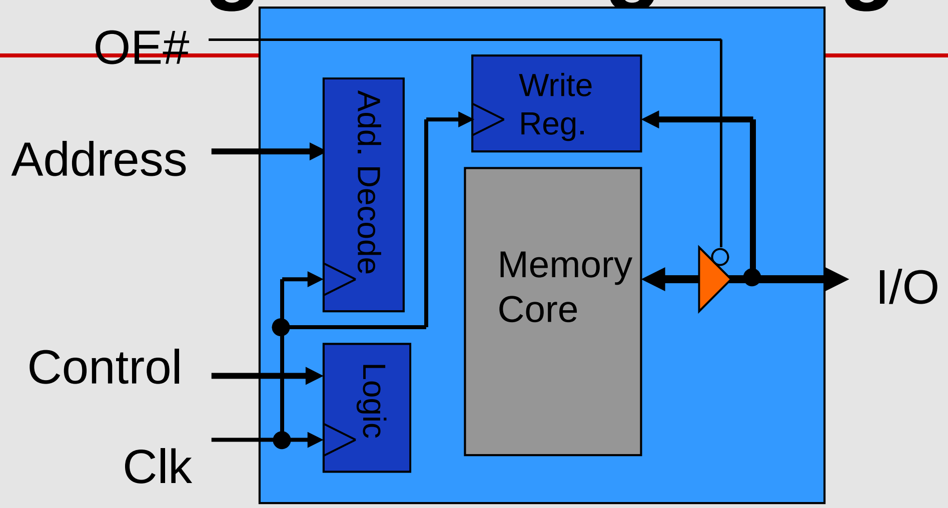
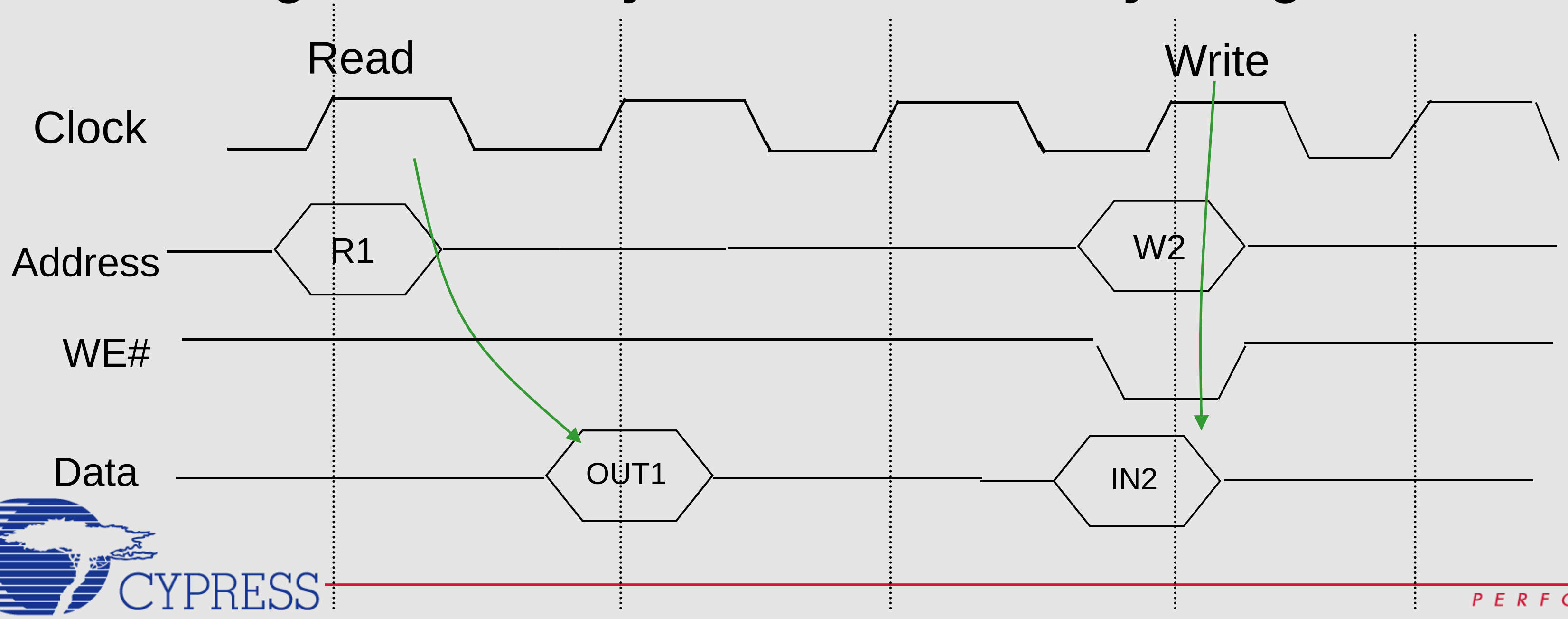
Flowthrough Timing Diagram

•



Flowthrough SRAM = Sync SRAM with only a register on I/P



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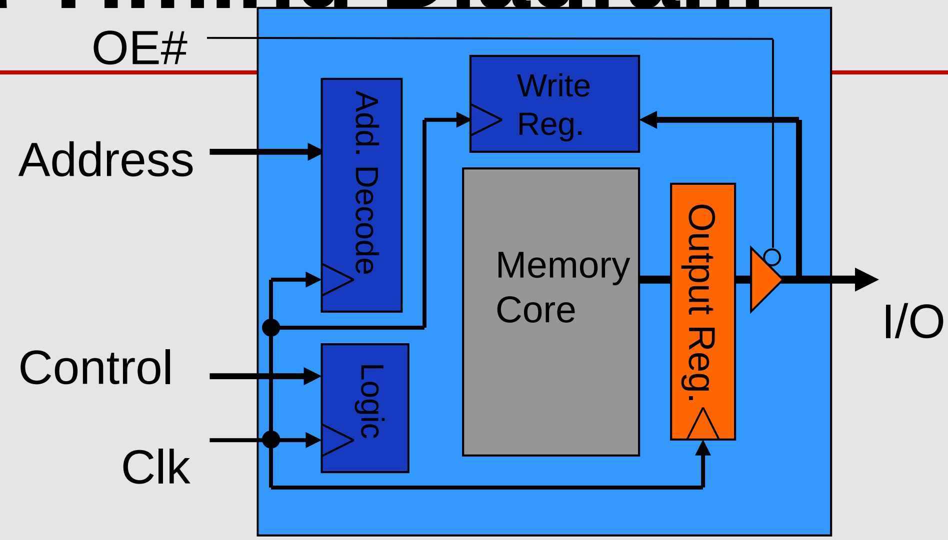
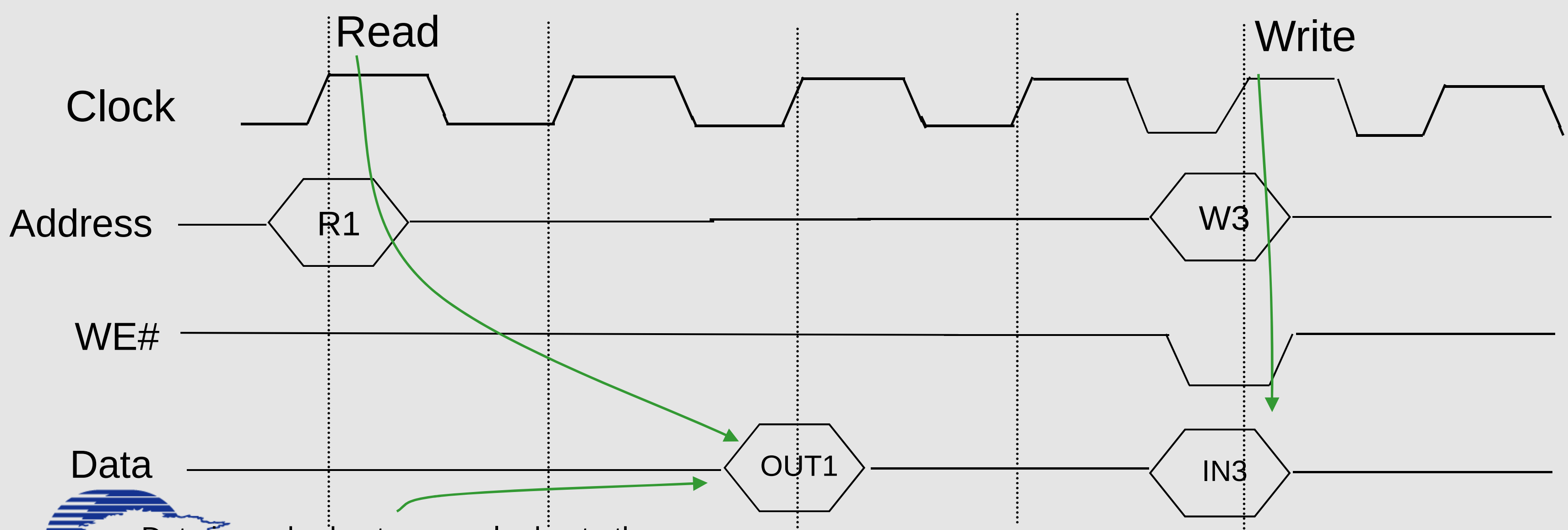
Pipelined Timing Diagram



-

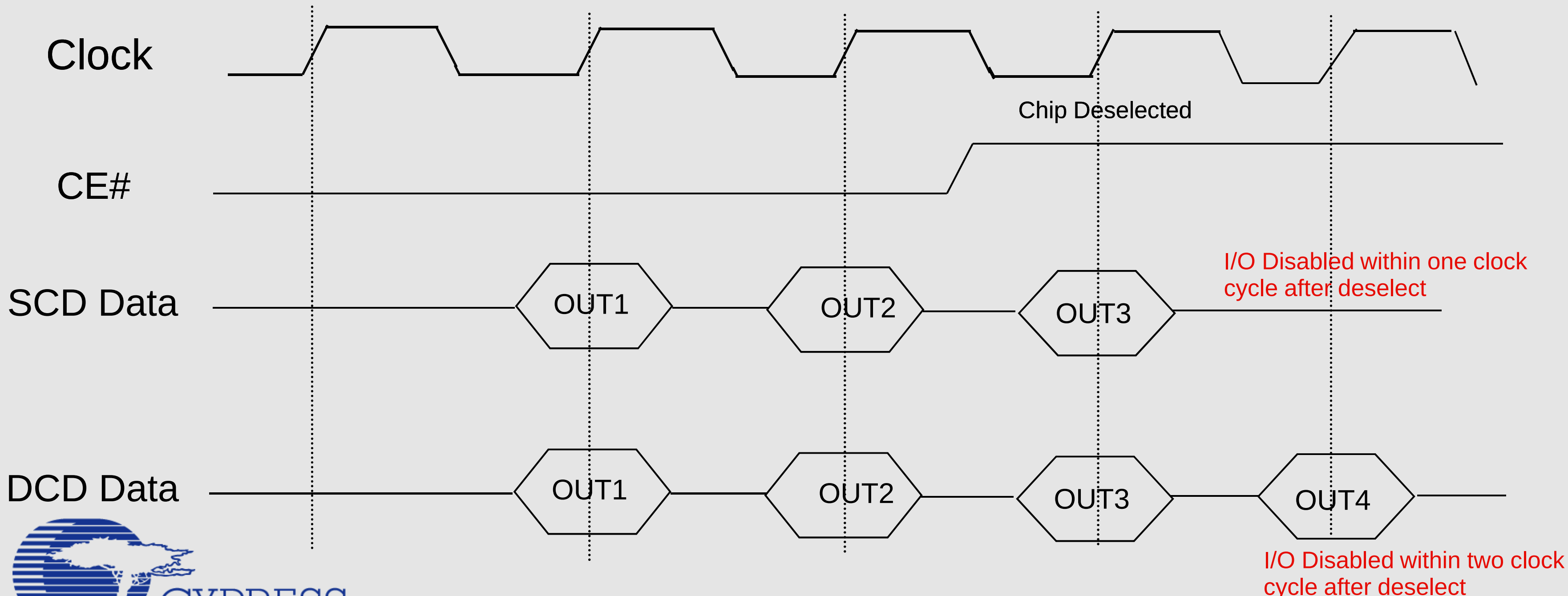
Pipelined SRAM = Flowthrough SRAM + Output register



Data is pushed out one cycle due to the output register.

SCD v/s DCD

- **SCD – Single-Cycle Deselect**
  - One clock cycle until chip deselects
  - Available in Pipelined and Flowthrough
- **DCD – Double-Cycle Deselect**
  - Two clock cycles until chip deselects
  - Available in Pipelined only



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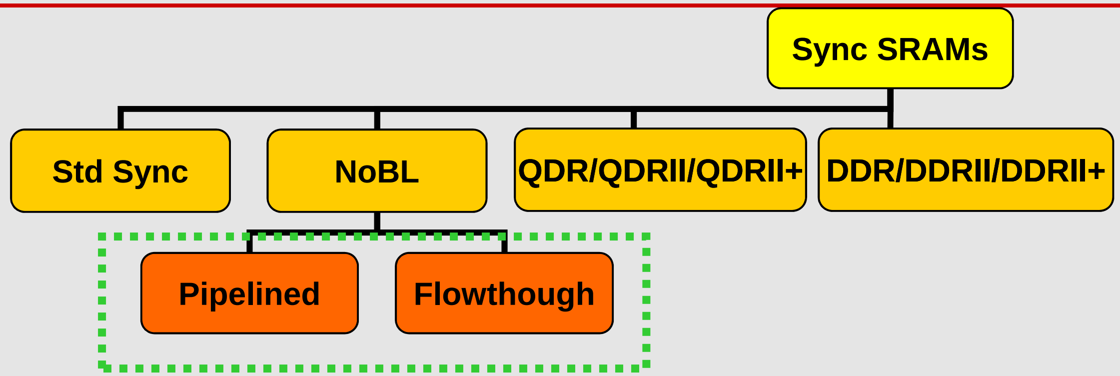
Flowthrough vs. Pipeline

- Pipeline operates at higher frequency than Flowthrough
- Flowthrough is used where the initial latency is a critical issue and a Pipeline SRAM is used where the speed is a critical issue.
- Write operations can take a single clock cycle to complete for both Flowthrough and Pipeline.
- Read operations take 2 clock cycles in flowthrough and 3 clock cycles in Pipeline.
- In networking applications where read/write is balanced (Ratio ~1), both pipeline and flowthrough SRAMs are not as efficient.

NoBL™ SRAMs

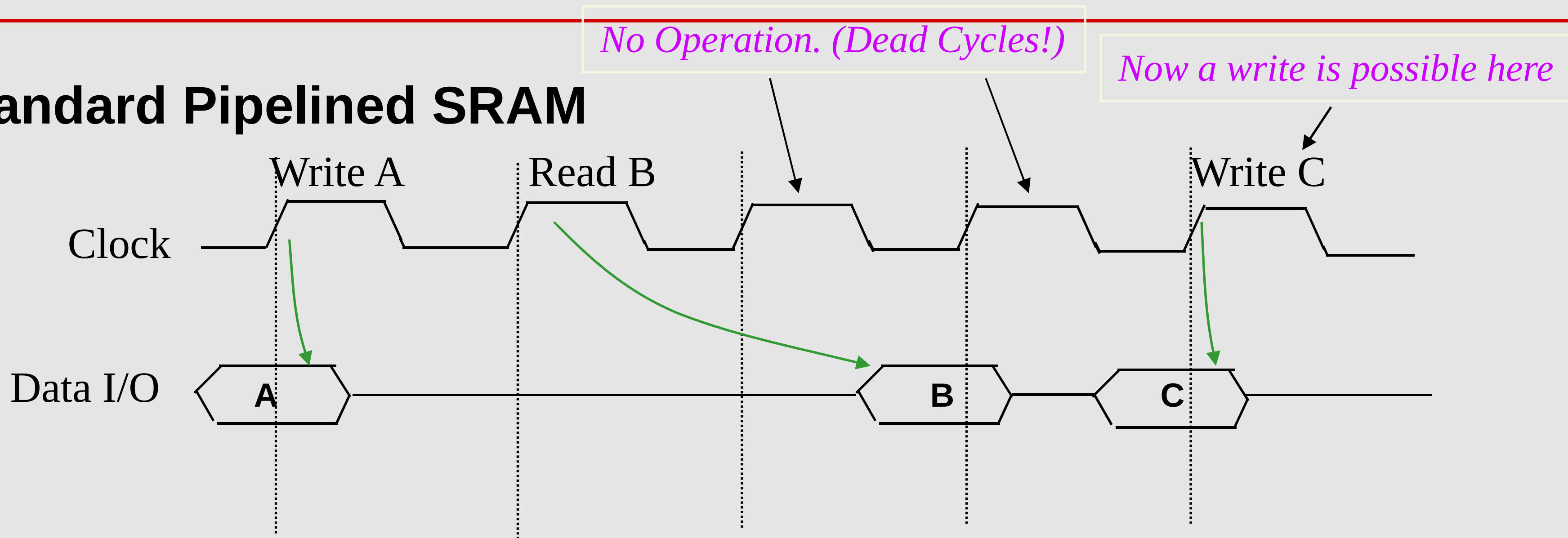


No Bus Latency (NoBL™)

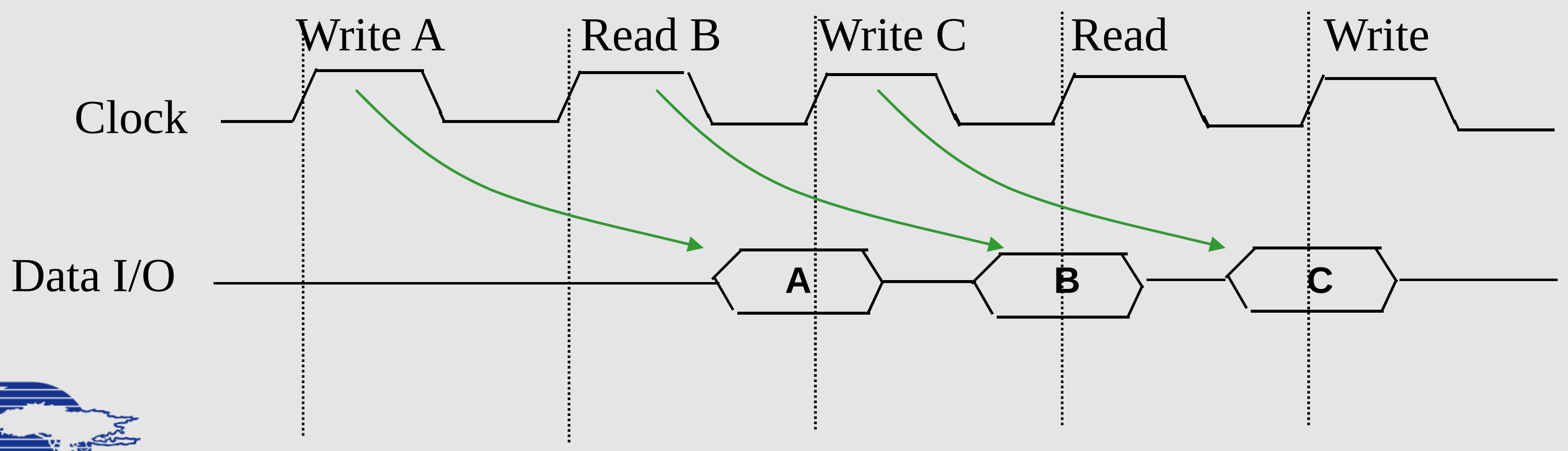
- Also Known as ZBT™
- No dead cycles between reads and writes
- Optimized for 50% reads and 50% writes
- Best for Networking Applications
- Offered in both Pipelined and Flowthrough modes

NoBL™ SRAMs

Standard Pipelined SRAM



NoBL Pipelined SRAM = Read and Write on Every Cycle!



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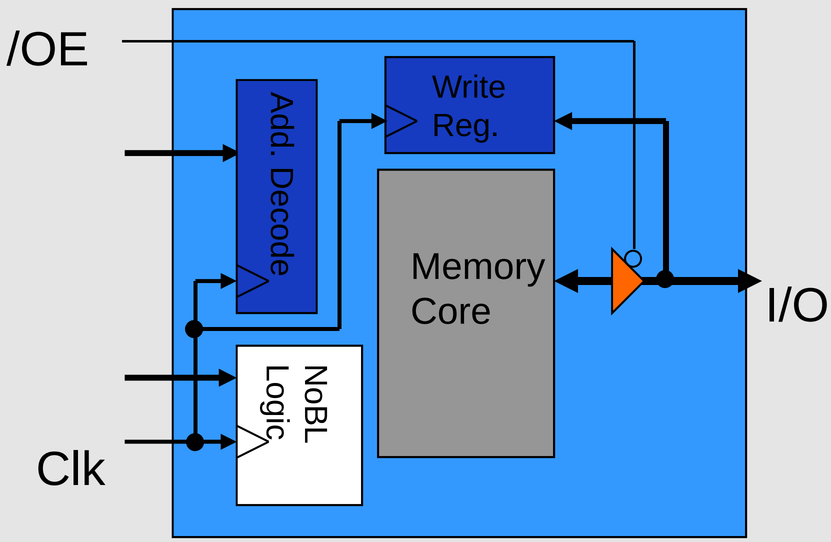
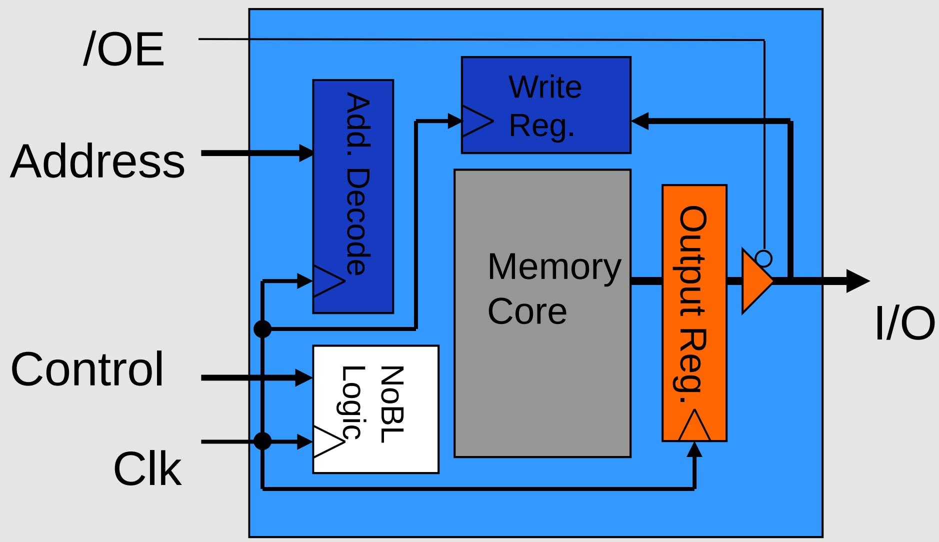
What is NOBL ?

NoBL SRAMs = Stand Sync SRAMs(FL or PL) + NoBL logic



NoBL
“Flow Through”



NoBL
“Pipeline”

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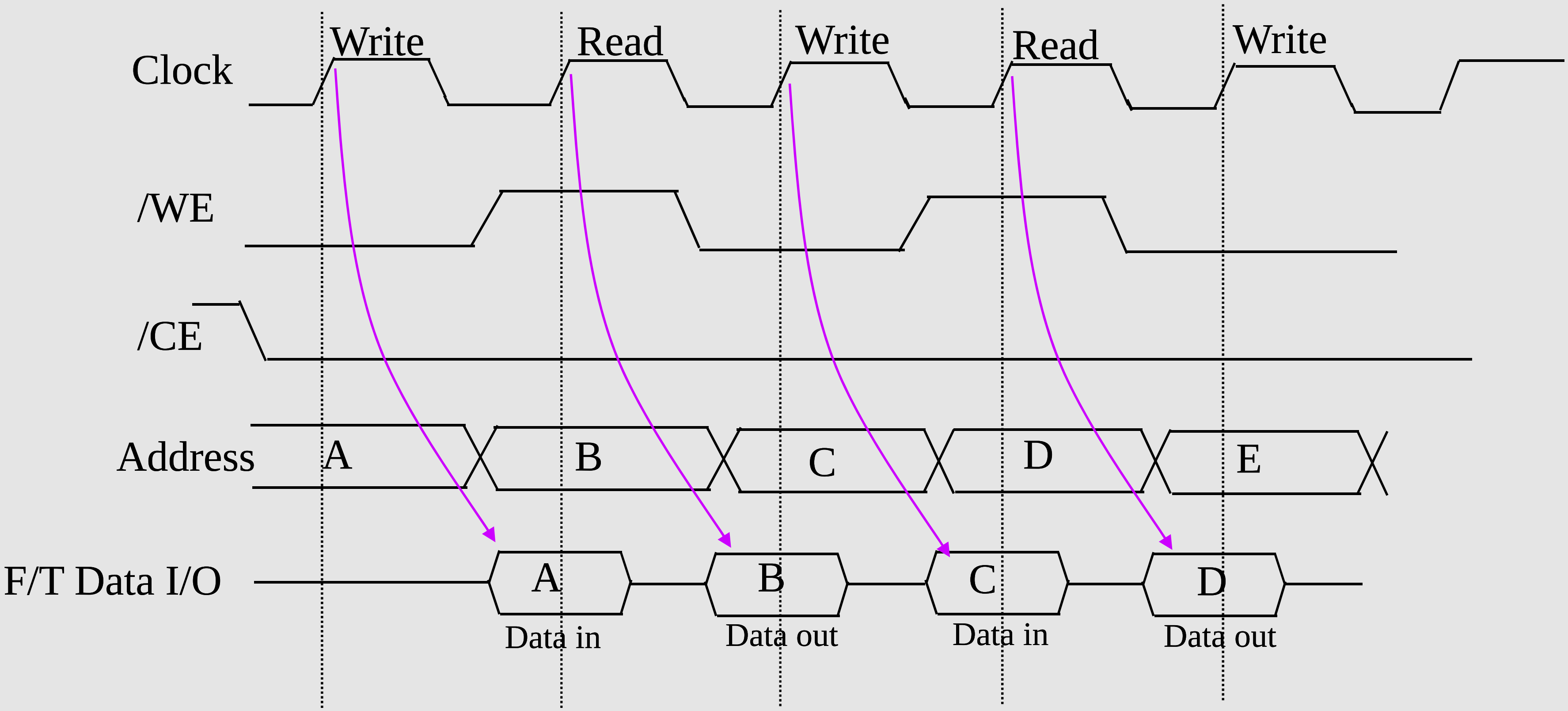
Flowthrough NoBL Operation

No Dead Cycles between Reads and Writes



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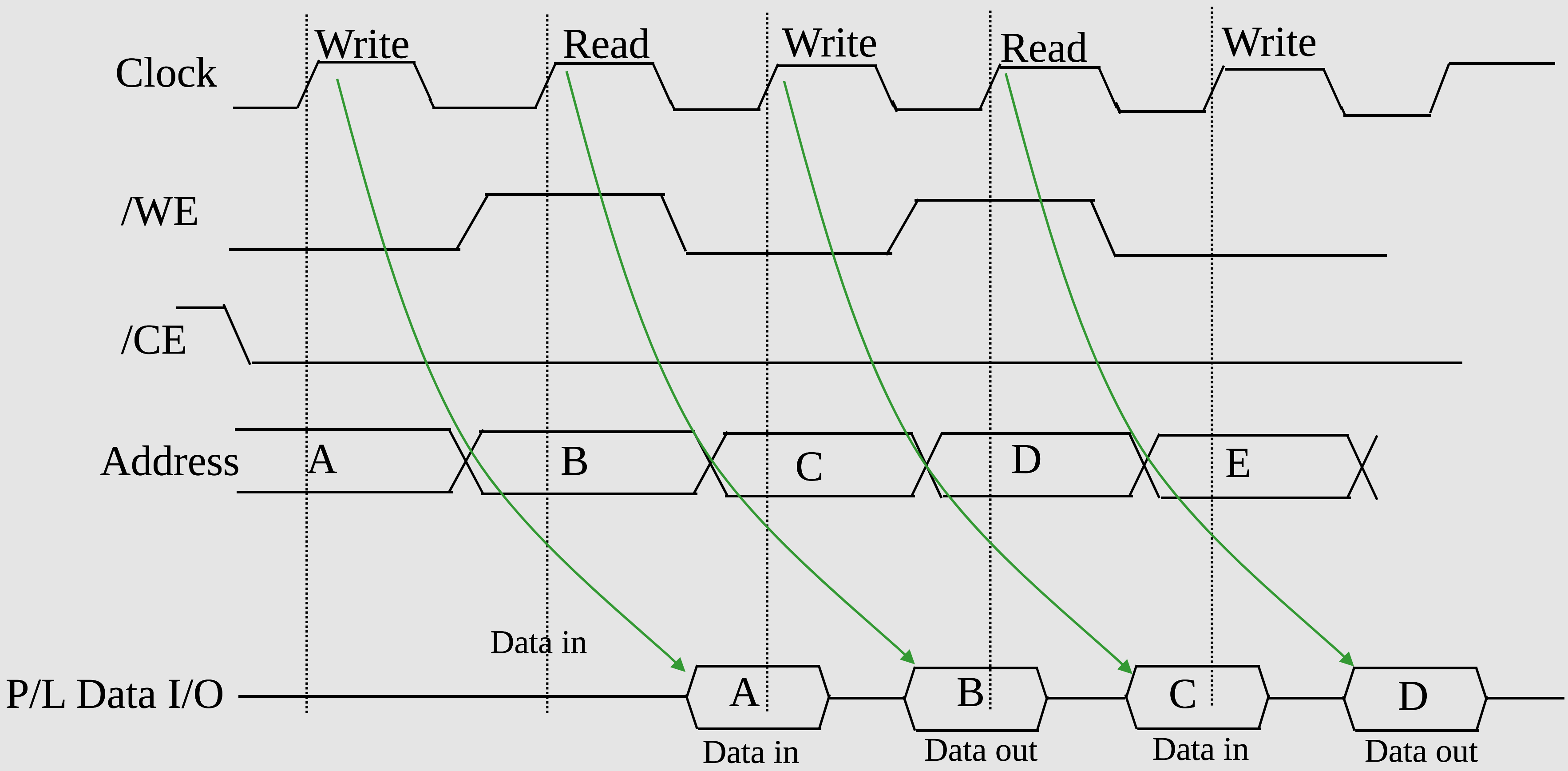
Pipelined NoBL Operation



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Standard Sync Vs NoBL

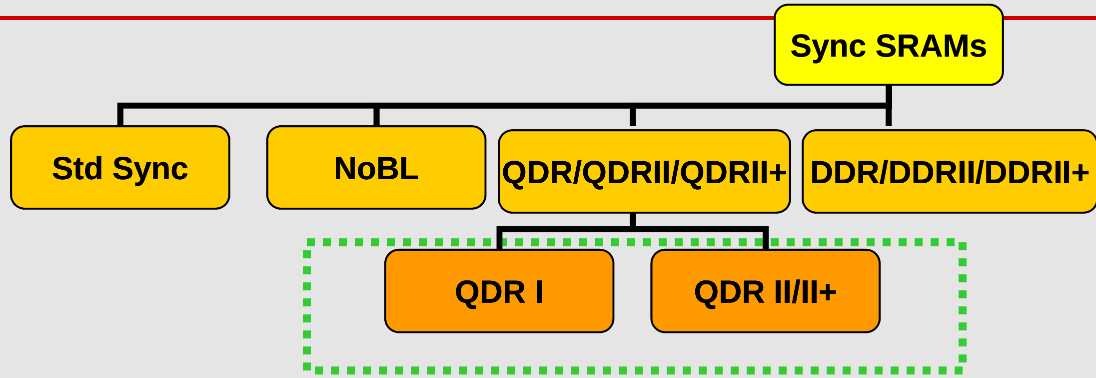
•**STANDARD SYNC**

- MOST EFFECTIVE FOR BURST READS OR WRITES FOR L2 CACHE
- IDEAL FOR DOMINANT READ OR WRITE
- LATENCY OCCURS WHEN SWITCHING FROM WRITE TO READ

•**NOBL**

- IDEAL FOR NETWORK APPLICATIONS
- IDEAL FOR READ/WRITE RATIO OF 1
- ENABLES FASTER MEMORY PERFORMANCE - ELIMINATES THE LATENCY CYCLE
- 2X BANDWIDTH IN HEAVY READ / WRITE APPLICATIONS

QDR

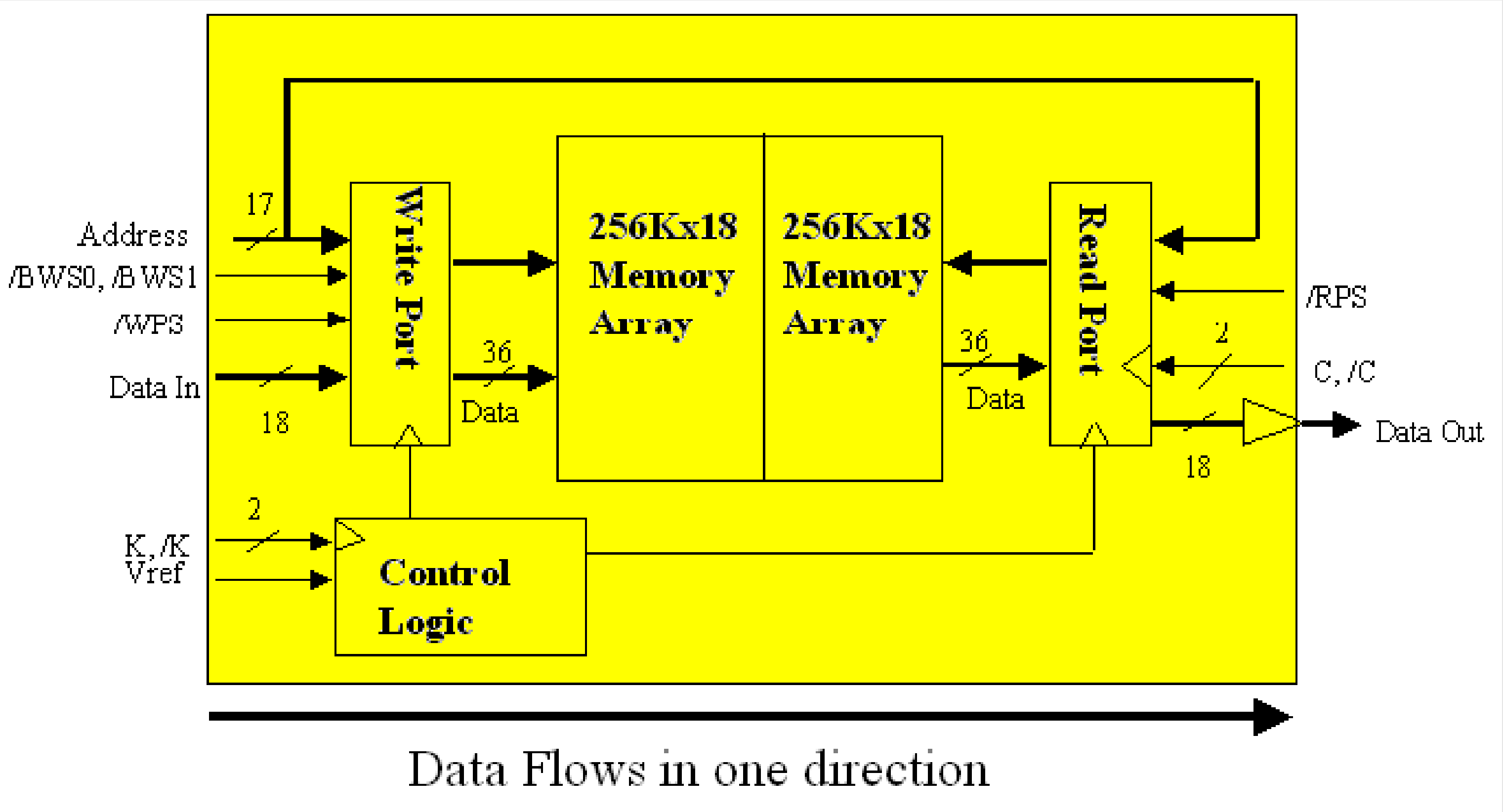


QDR = Quad Data Rate

- Joint effort between Cypress and Other Industry Leaders
- Optimum for balanced Read/ Write Applications
- Separate Input and Output Ports = No bus contention
- Double Data Rate on Separate Ports = 4X Bandwidth
- HSTL(High Speed Transceiver Logic) I/O Levels
- Programmable output Impedance using ZQ pin

QDRI Burst of 2 BLOCK DIAGRAM

- 2 Word Burst QDR SRAM
- Separate Read and Write control signals
- Vref signal due to HSTL I/O



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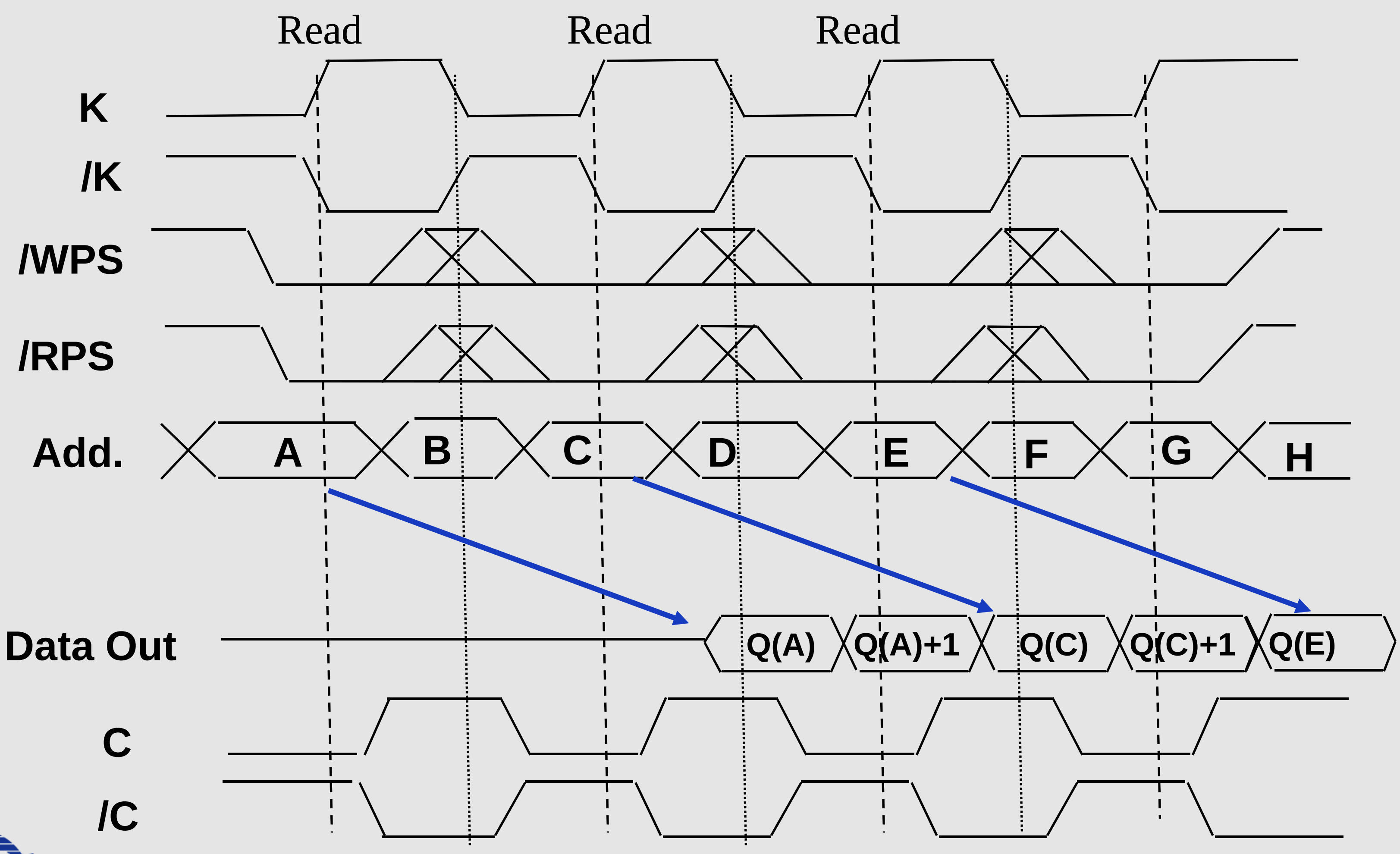
QDRI Burst of 2 Read Operation



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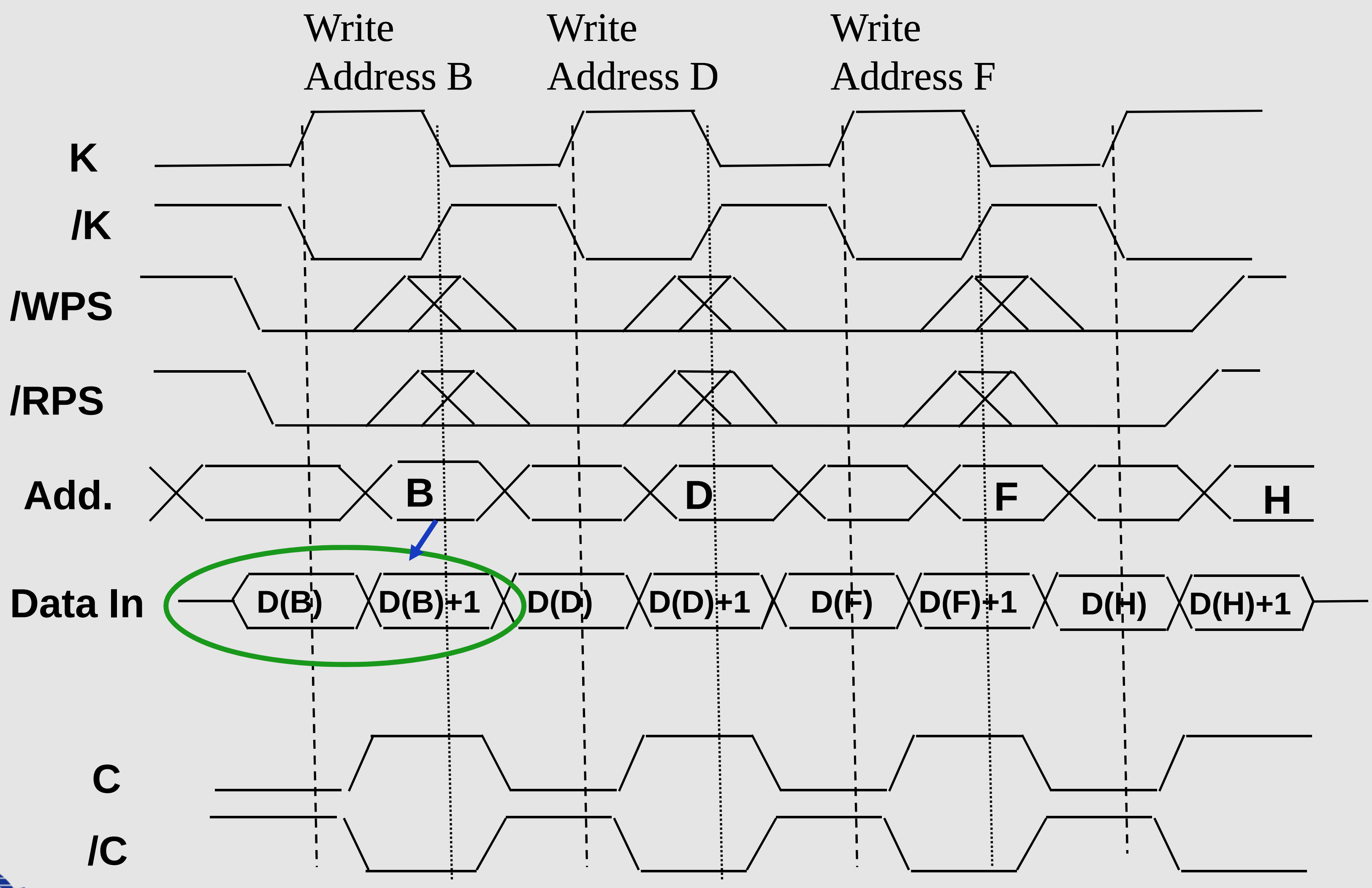
QDRI Burst of 2 Write Operation



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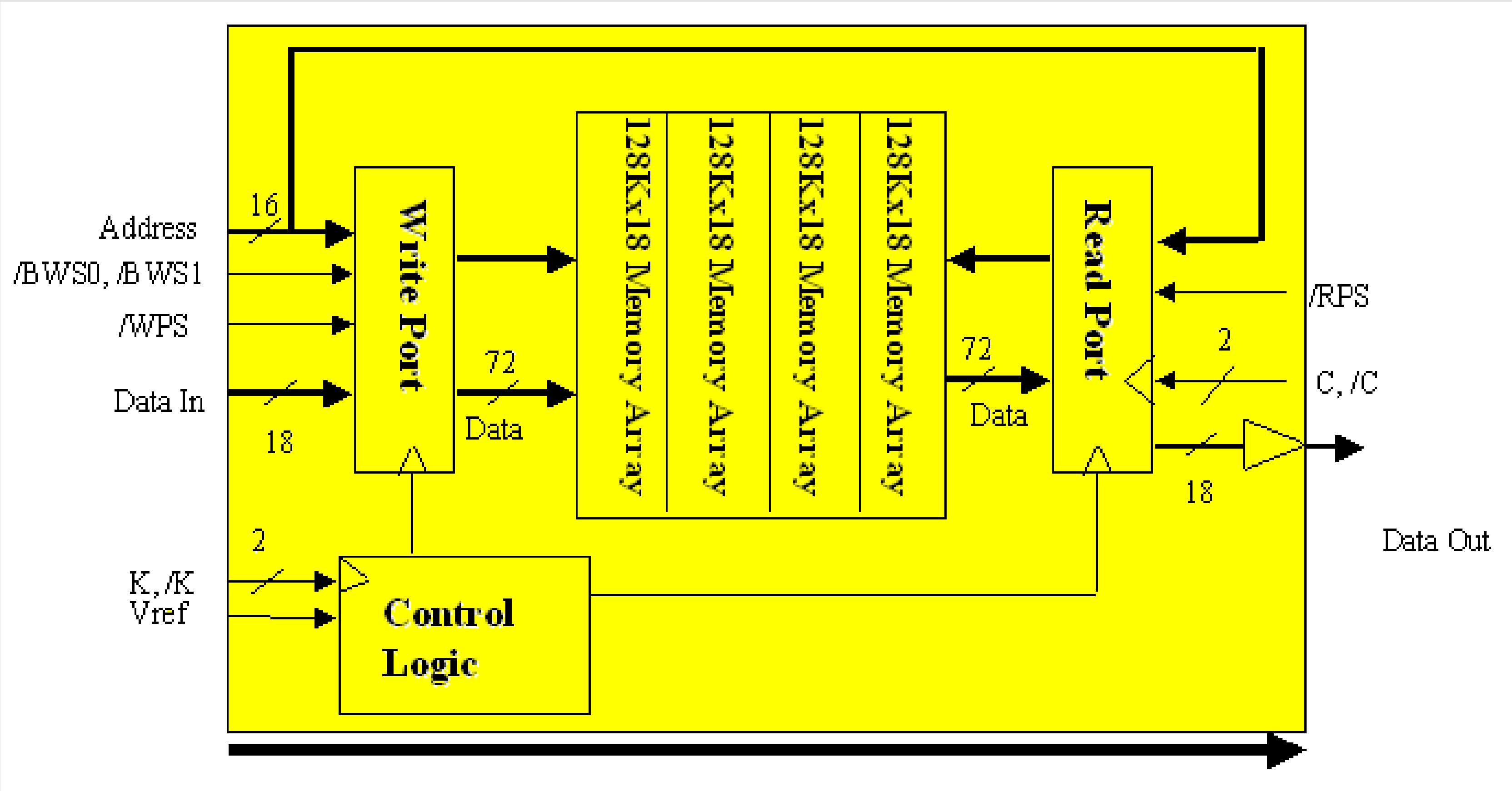
QDRI Burst of 4
BLOCK DIAGRAM

- 4 Word Burst QDR SRAM
- Burst of 2 and 4 are two different parts



Data Flows in one direction

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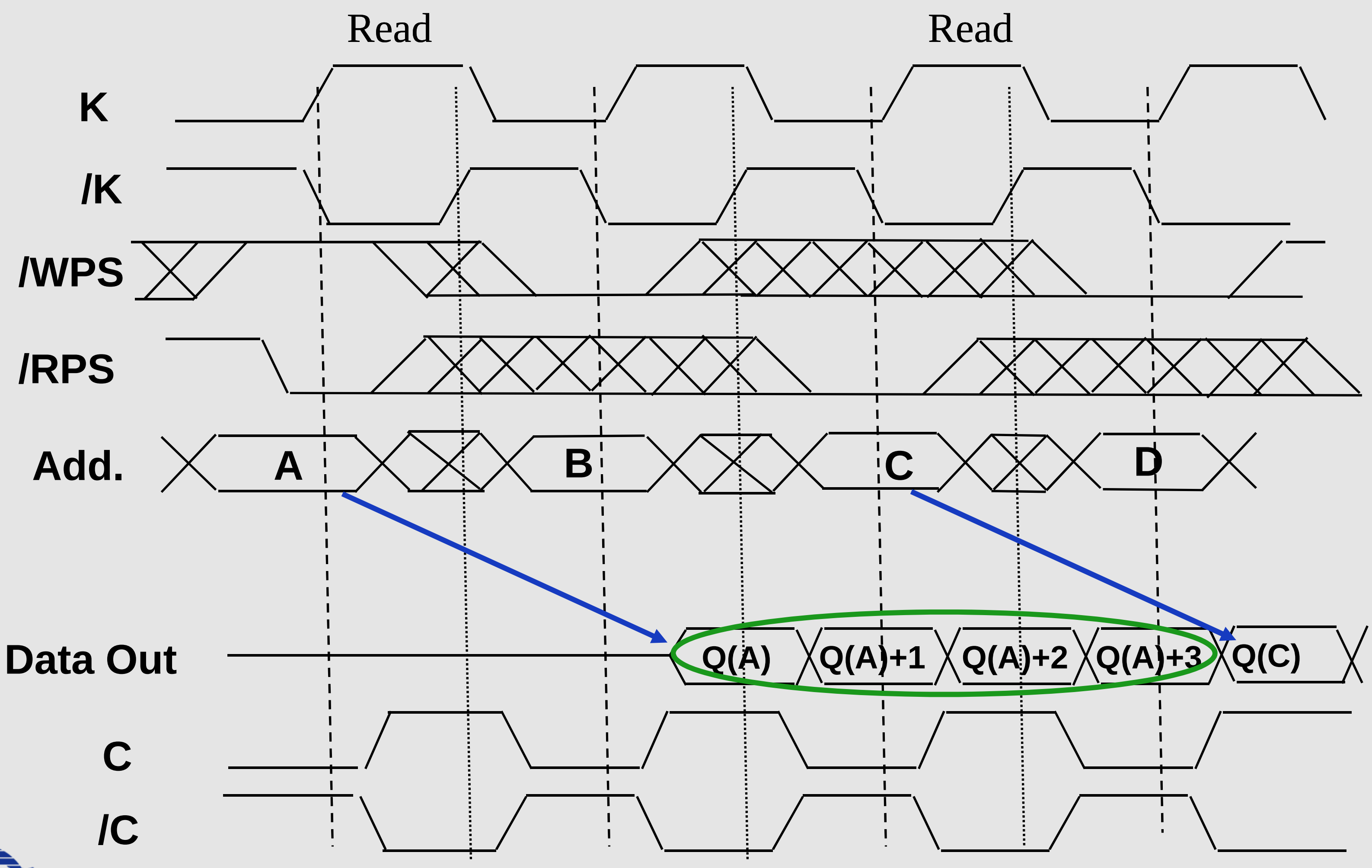
QDRI Burst of 4 Read Operation



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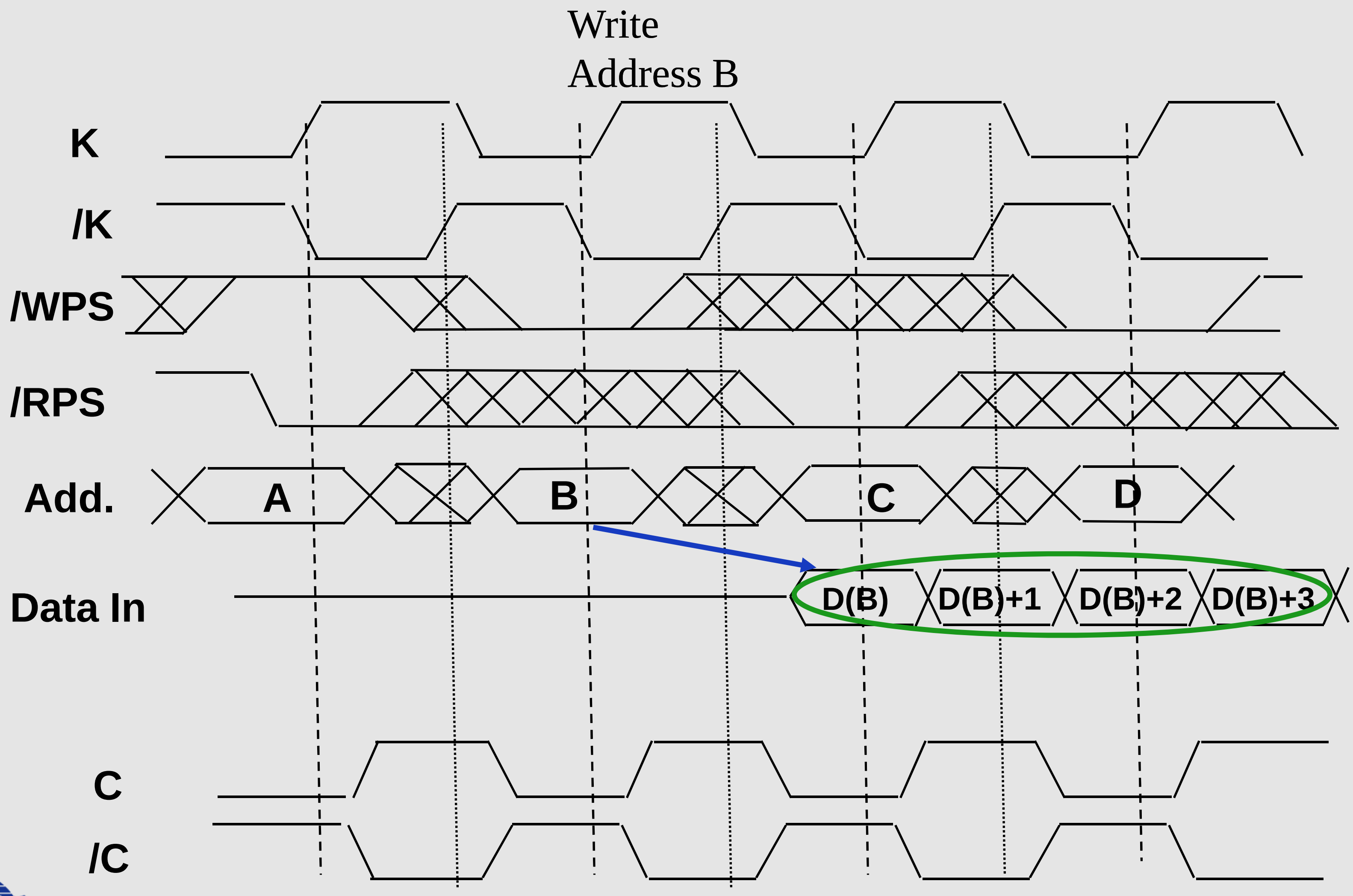
QDRI Burst of 4 Write Operation



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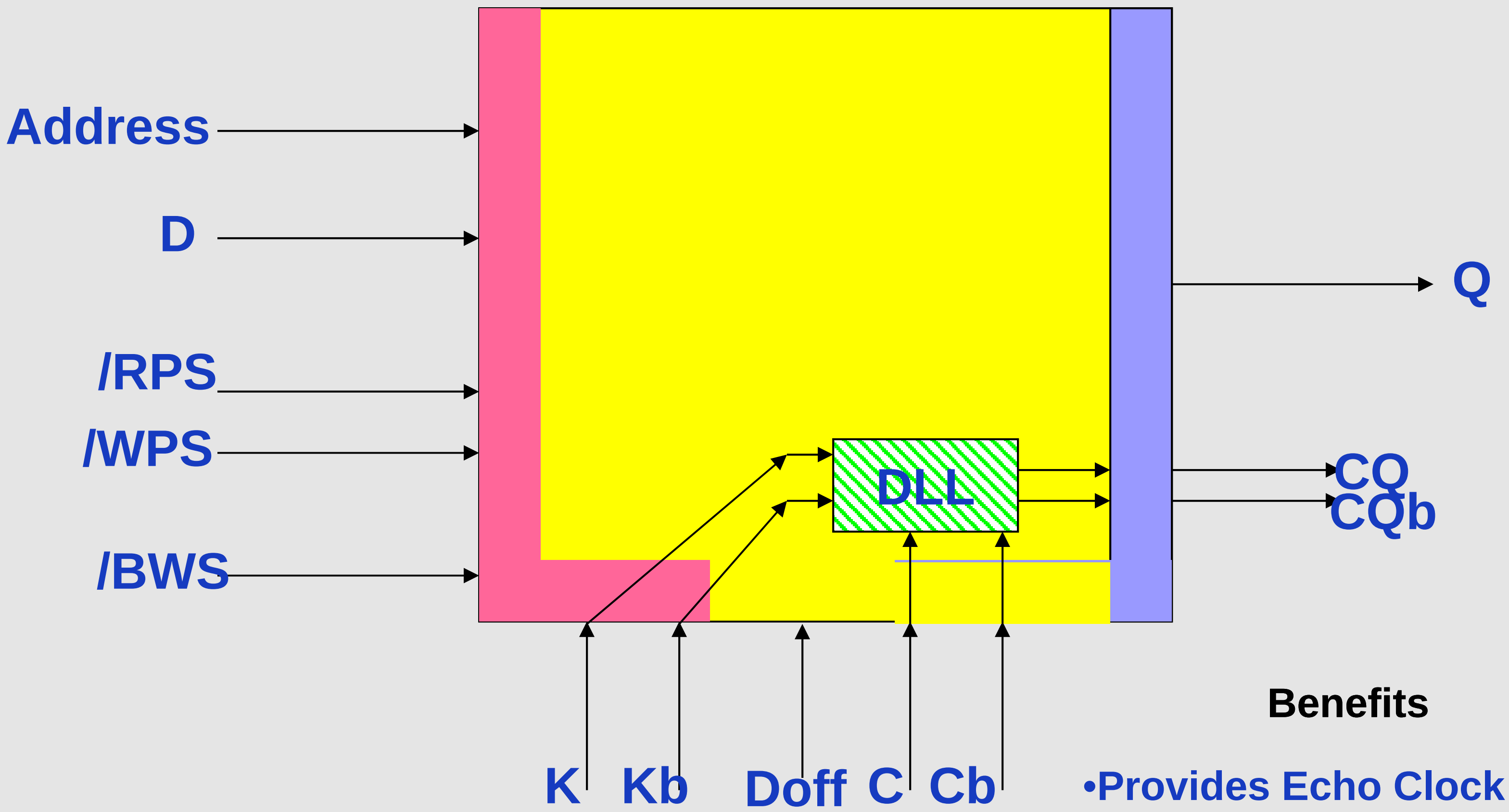
QDR Advantages

- 4x Network Performance

- Features Benefits

- * Simultaneous Accesses * Improved Bandwidth(~2x)
- * DDR Interface on Both Ports * Improved Bandwidth(~2x)
- * Pipeline Output * Low Initial Latency
- * Separate Input/Output Ports * No Bus Contention
- * 165 FBGA Package * Reduced Board Area

QDR to QDR-II Transition



Benefits

- Provides Echo Clock
- Allows higher speed operation

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QDR-II Features

- QDR II Purpose:
  - Extend QDR Solution to 250MHz (From 166MHz)
- QDR-II Has Internal DLL (Delay Lock Loop)
  - Shorten Clock-Valid, Lengthen Data Hold
  - Source Synchronous Clocks (Echo Clock) Added
    - Echo Clock Outputs From SRAM
  - Guaranteed Relationship to Valid Data
- Additional 1/2 Clock of Latency

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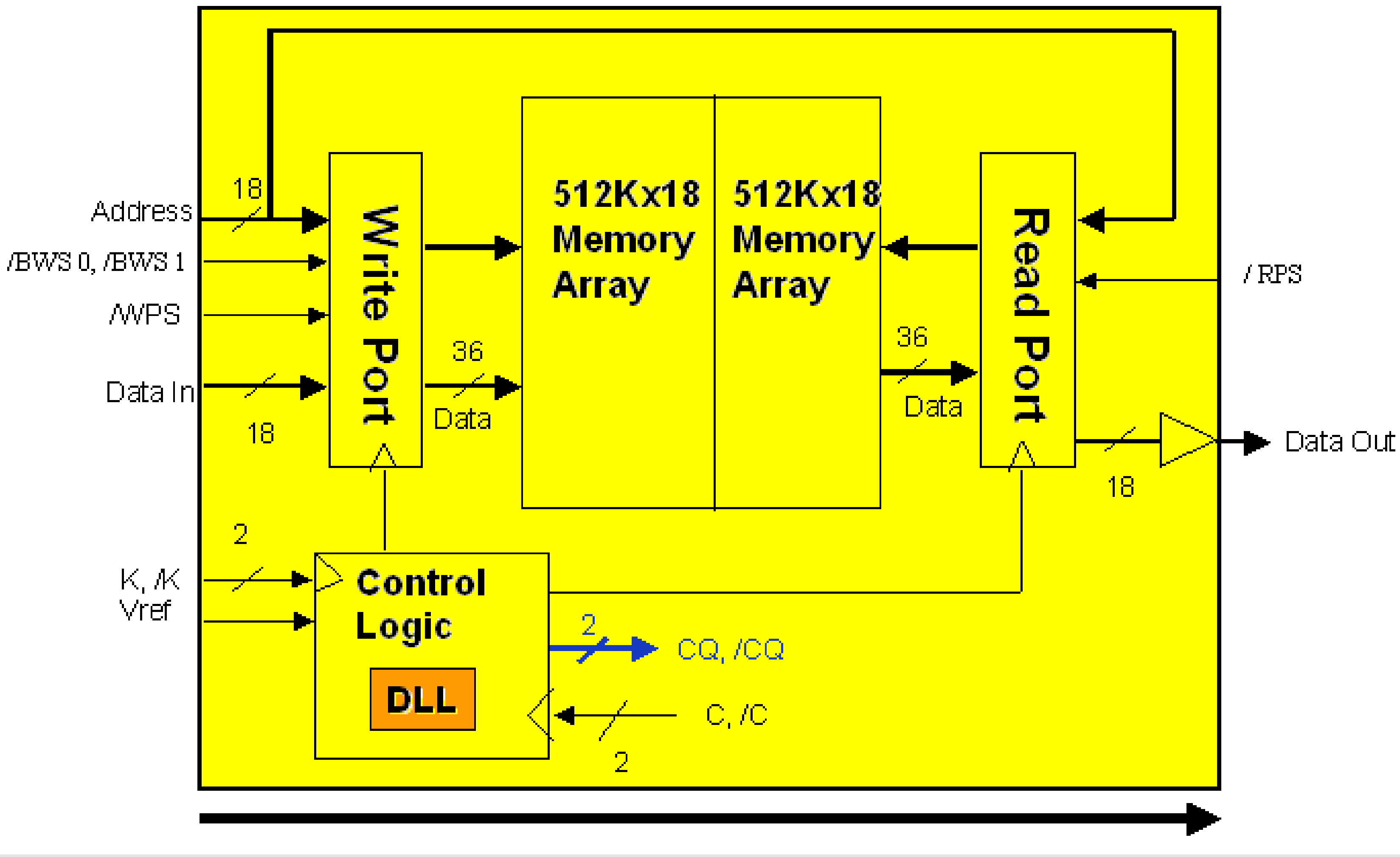
QDR-II Block Diagram



Data Flows in one direction

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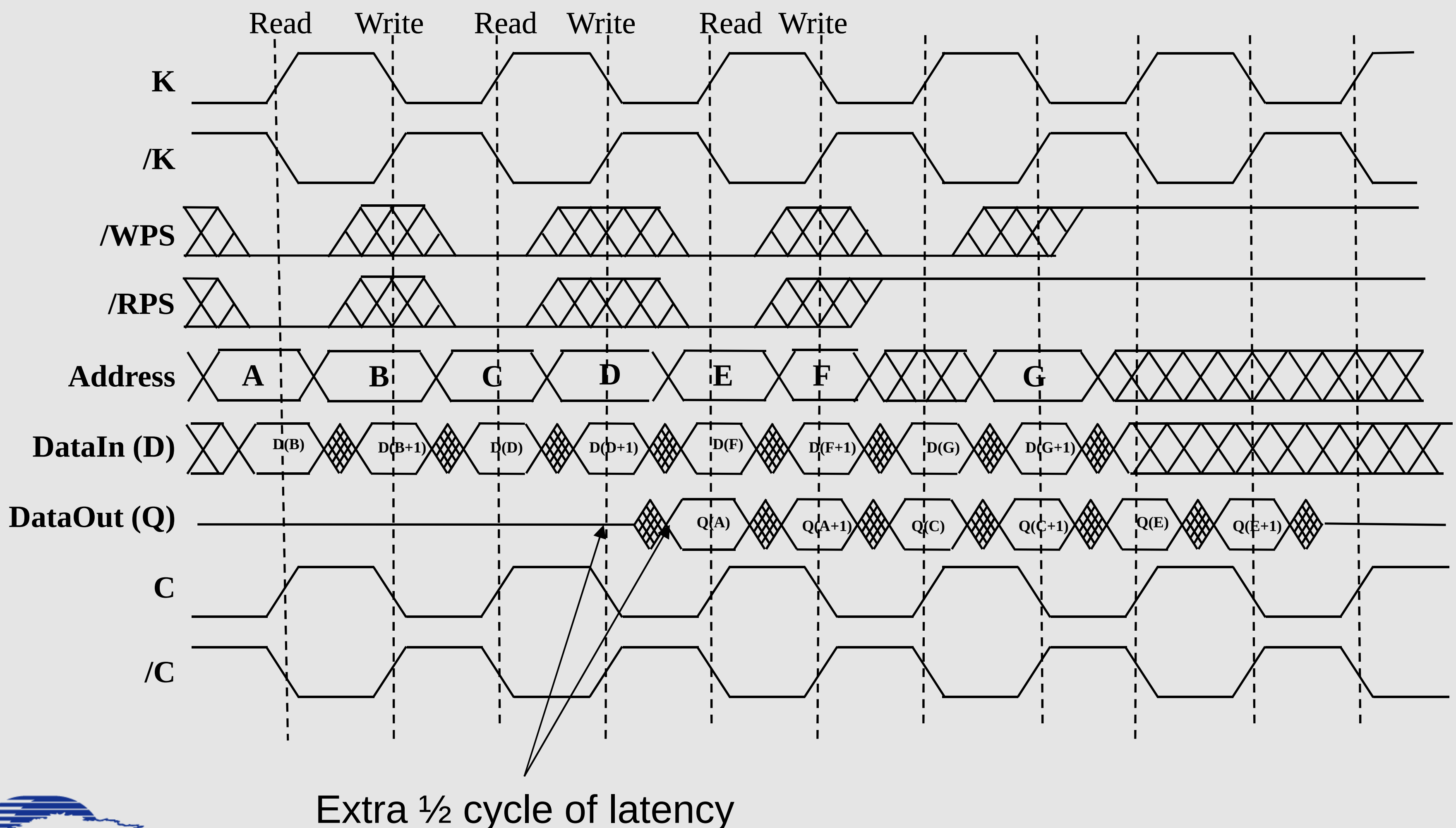
QDRII Burst of 2 Operation

- Read/Write Access



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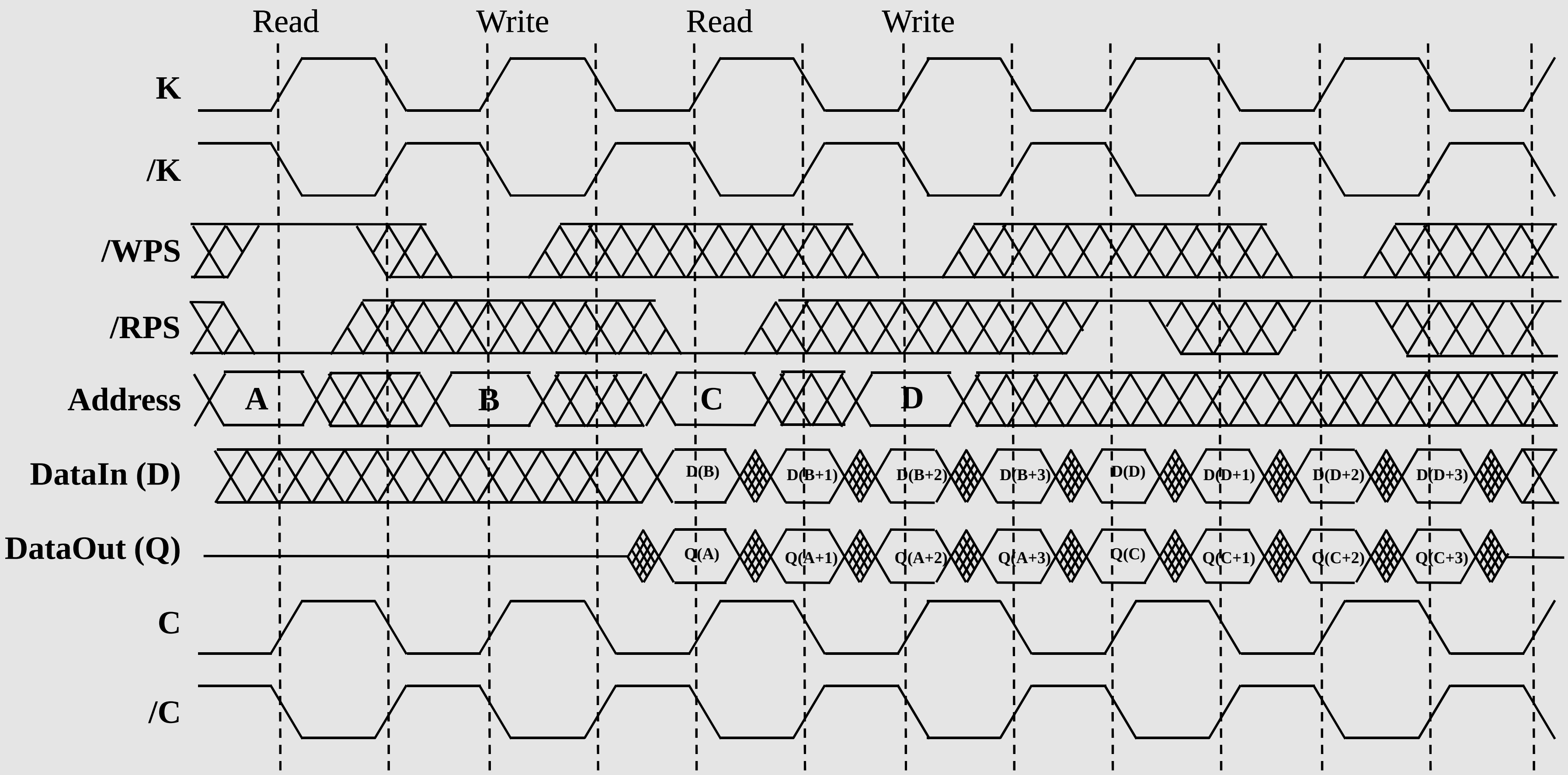
QDRII Burst of 4 Operation

- Read/Write Access



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QDR-II Advantages

The 2nd Generation

Features	Benefits
* 300Mhz Fmax	* Higher Bandwidth
* 1.5 Clock cycle Pipeline	* Low Initial Latency
* 18Mb / 36Mb / 72Mb	* Higher Density
* Echo clocks	* Source-Sync. Output Data
* DLL	* Faster Data Capture
* 1.8V Power Supply	* Lower Power
* Same 165FBGA Package	* Compatibility

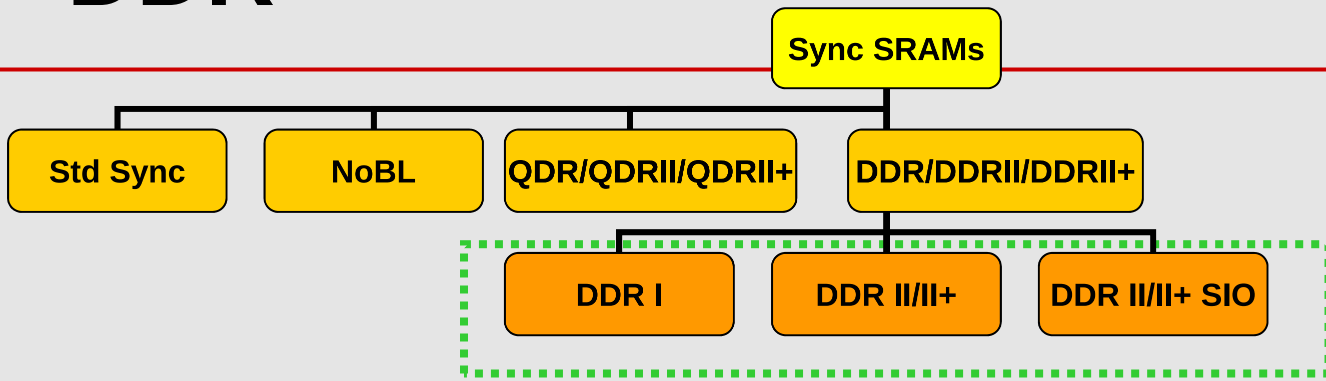
QDR vs QDR-II

Summary of Differences

	QDR	QDR-II
Maximum Frequency	Burst of 2: 167MHz Burst of 4: 200 MHz	Burst of 2: 167 MHz Burst of 4: 300 MHz
Frequency Minimum (DLL Constraint)	N/A	100 MHz
Data Valid Window	1.4ns @ 167MHz	1.9ns @ 167MHz 1.4ns @ 250MHz
Initial Latency	1 clock cycles*	1.5 clock cycles*
Echo Clocks	No echo clocks	Echo clocks
Density	9Mb / 18Mb / 36Mb	18Mb / 36Mb / 72Mb+
Power Supply	2.5V	1.8V

* By adding an ½ clock cycle of latency to QDR-II, the access time is reduced to 0.45ns from QDR's 2.5 ns.

DDR



DDR = “Double Data Rate”

- Shared Input and Output Buses
- Optimized for Dominant Reads OR Writes
- Double Data Rate Interface
- Commonly referred to as “Networking” DDR and DDR-II
- Data transferred on both edges of the clock
- Two and Four Word Burst Devices

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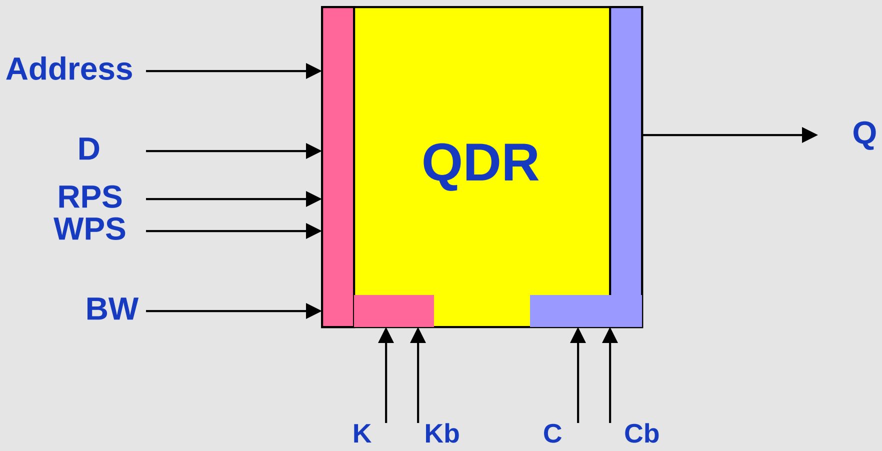
QDR vs. DDR

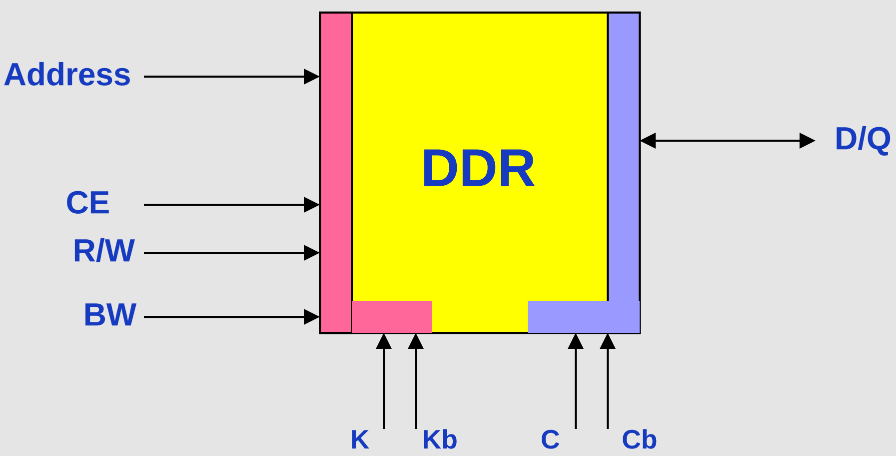


DDR Characteristics

- •Double Data Rate
- •Common I/O

QDR Characteristics

- •Double Data Rate
- •Simultaneous R/W Access possible
- •Separate Input and Output ports



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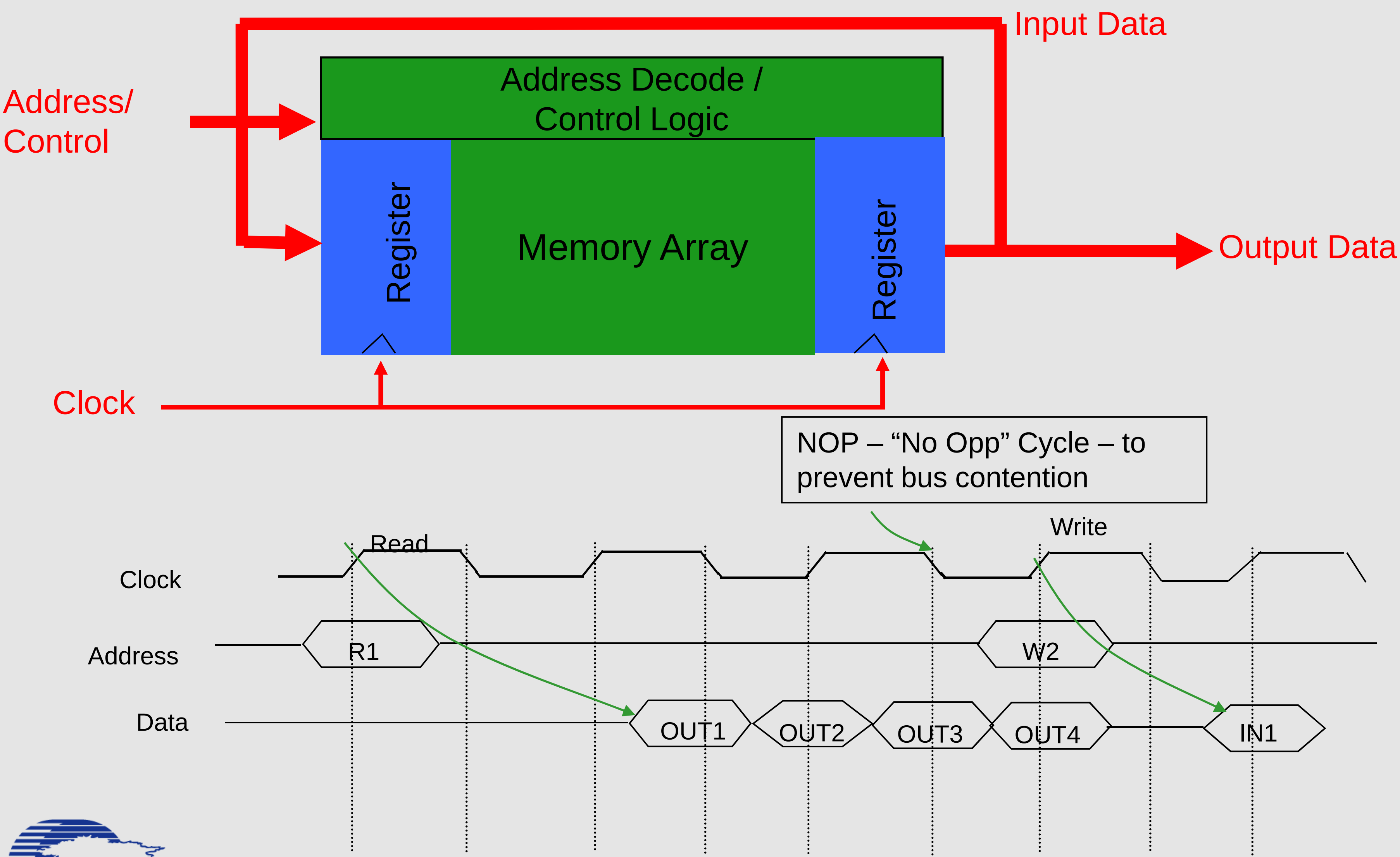
DDR Block Diagram



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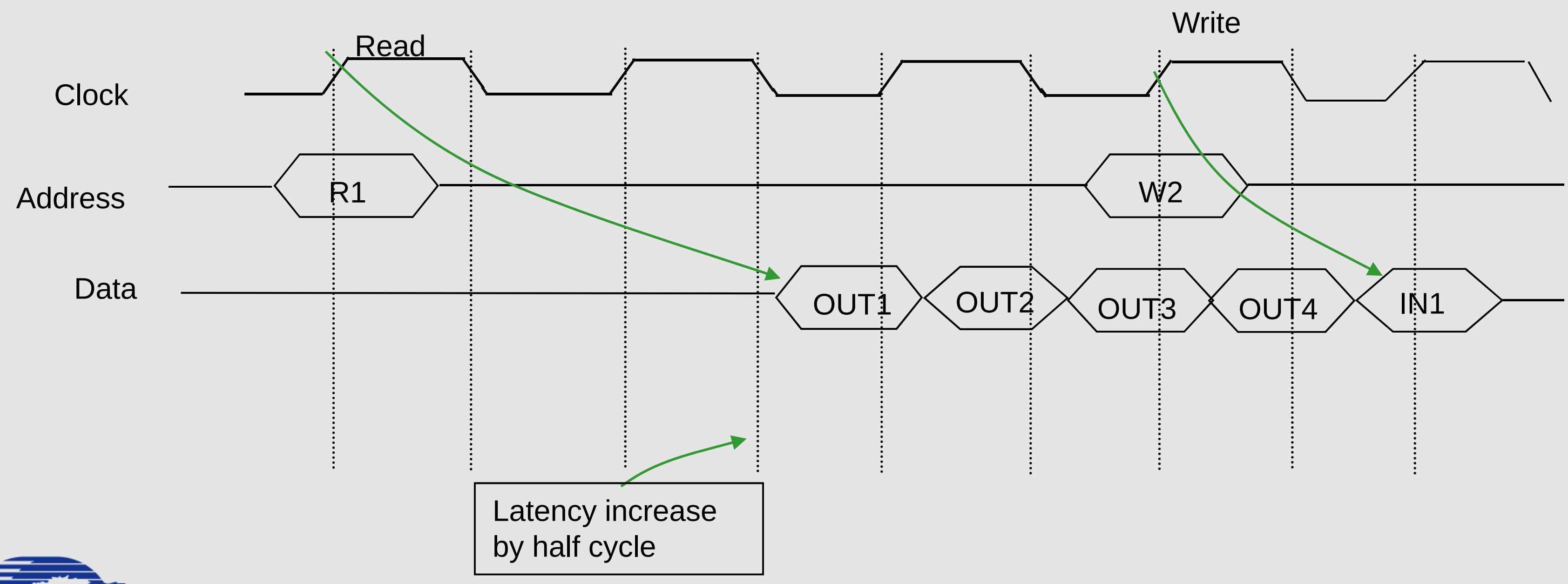
DDR II

- •Changes from DDR
  - Internal DLL
    - Higher clock frequency
    - Latency increased by half a cycle
  - Increase Data Valid Window



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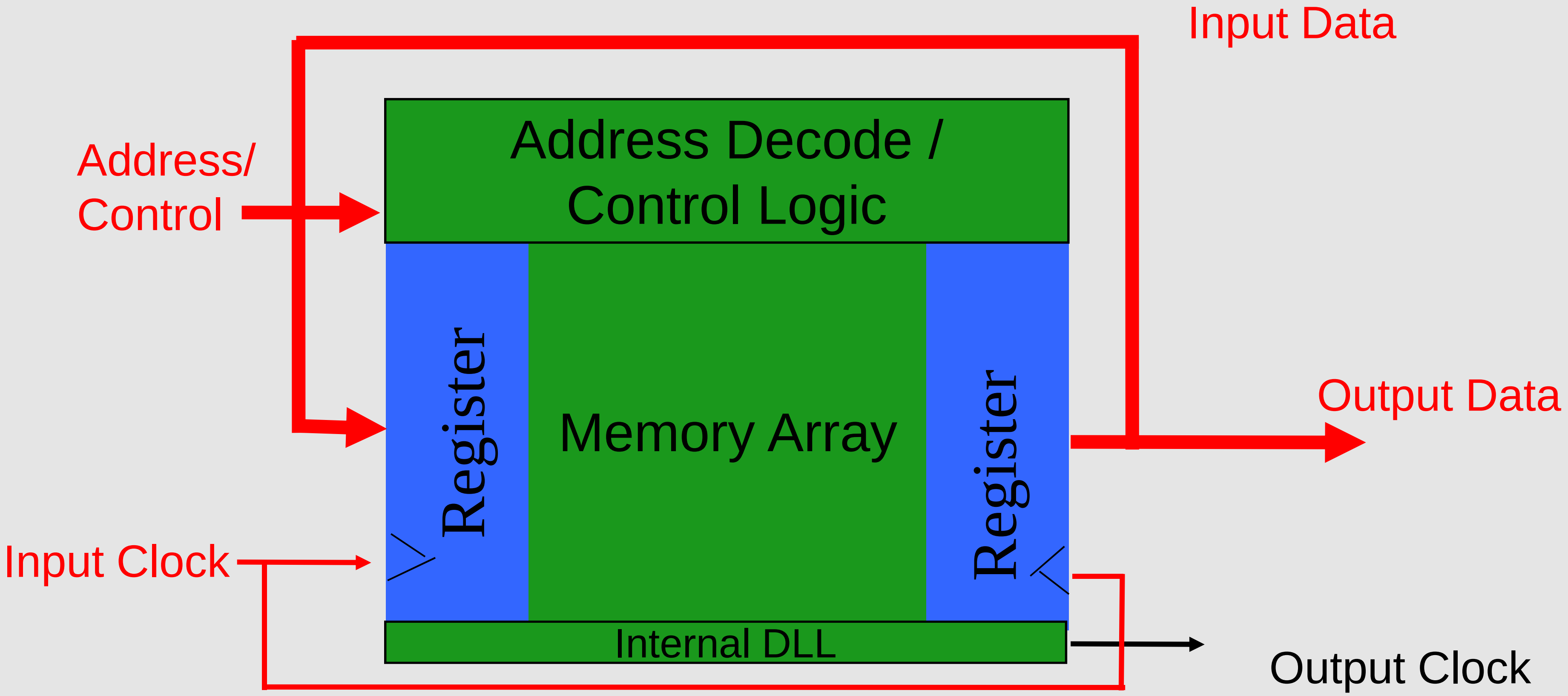
DDR-II Block Diagram



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DDR & DDR-II

2 Reads OR 2 Writes / Clock Cycle = DDR & DDR-II

I/O Bus is the Only Major Difference From QDR & QDR-II

	Feature	Benefit
Bandwidth	DDR Interfaces	Higher Mb/s
	DDR: 200MHz DDR-II: 300MHz	Higher Mb/s
Package Pin/Ball Count	Shared I/O bus (DDR & DDR-II CIO)	Reduces ball count
Bus Contention (B2 @ $\geq$ 200MHz)	Split I/O buses (DDR-II SIO)	Eliminates bus contention
	Single address per clock cycle	Reduced address rate relative to QDR

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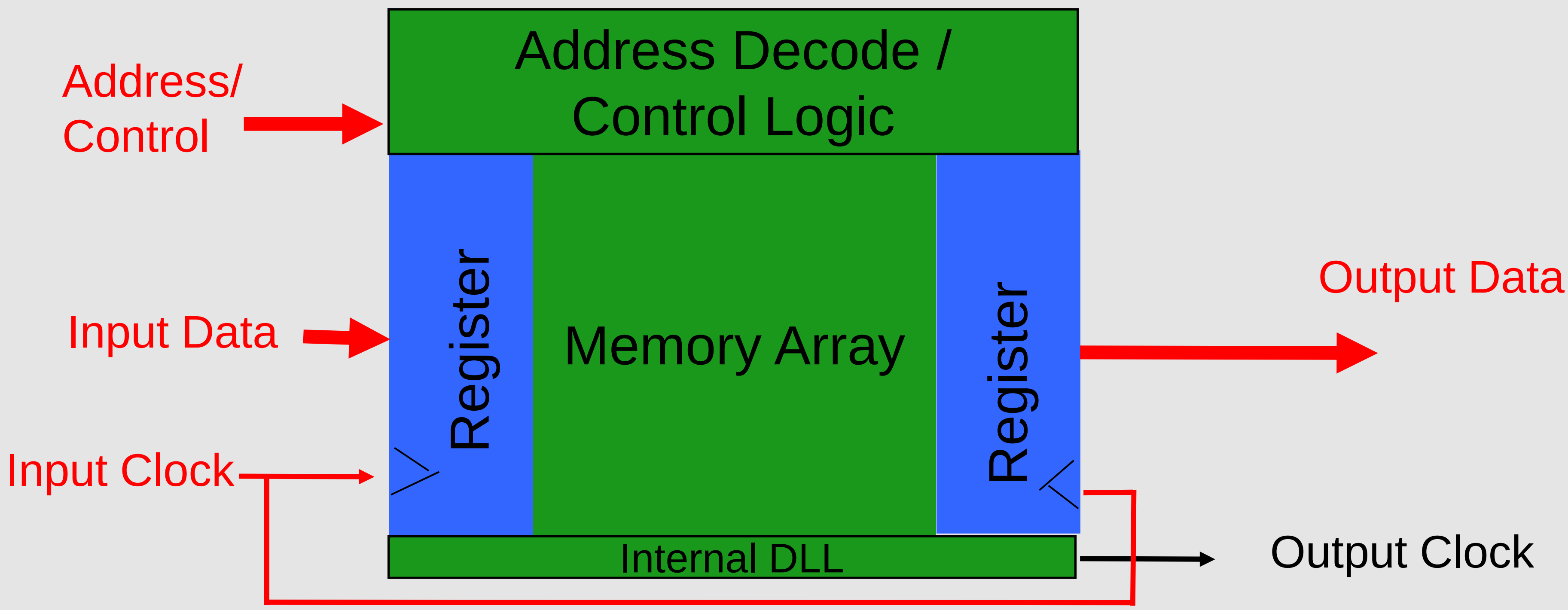
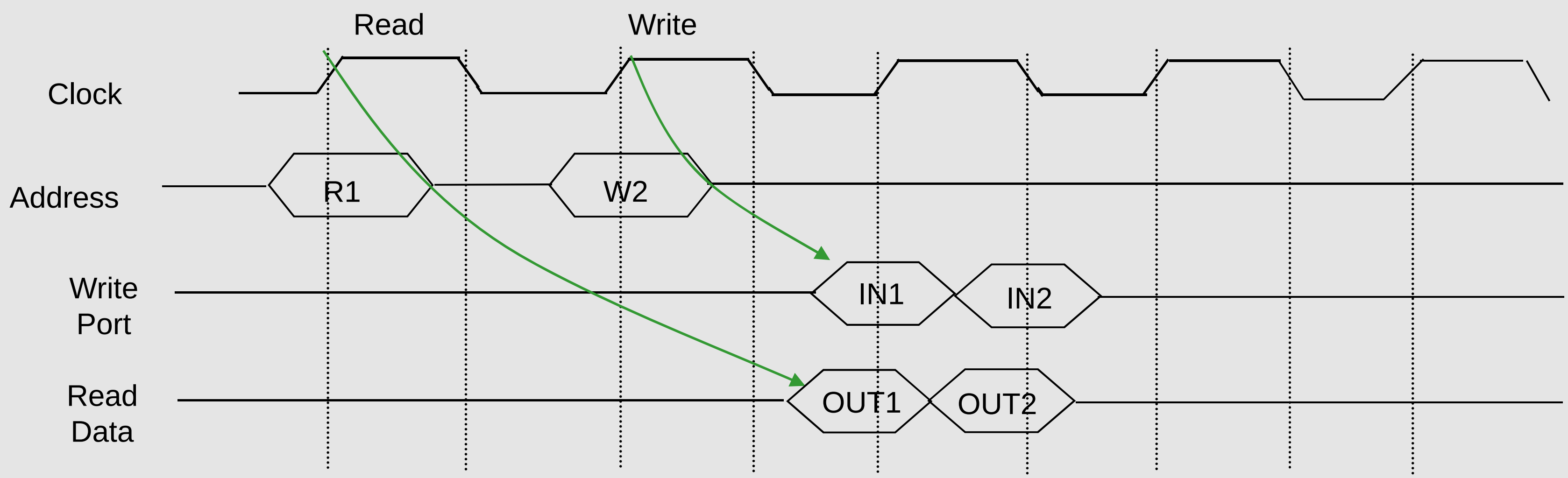
DDR II SIO


Address/
Control
Address Decode /
Control Logic
Input Data
Register
Memory Array
Register
Output Data
Input Clock
Internal DLL
Output Clock

DDR II SIO

- **DDR-Separate I/O (SIO)**
  - Separate Input and Output Buses
  - Only One Operation Per Clock
    - Can Not Perform Data Forwarding Feature
- **Eliminates Bus Contention**
- **Two Word Burst Only**



QDR & DDR SRAM Architectures

- QDR™ / QDRII™
  - Separate Input and Output Buses
  - Double Data Rate Interface on Both Buses
  - 4X Increase in Bandwidth From NoBL™
- DDR™ / DDRII™
  - Single I/O Bus
  - Double Data Rate Interface
  - 2X Increase in Bandwidth, Reduces ASIC/FPGA Pin Count
- DDRII Separate I/O
  - Operates like a QDRII-burst of 2 device with access on only one port per clock cycle
  - Separate Input and Output Buses
  - Double Data Rate Interface on Both Buses
  - 2X Increase in Bandwidth From NoBL™

QDR - DDR Summary

- QDR and QDRII are optimized for systems with Balanced READ and WRITE operations
  - Packet memory
  - Linked-list
  - Lookup Table
  - Statistics Storage
- DDR and DDRII are optimized for data streaming operations or READ/WRITE unbalanced systems
  - L2 Cache
  - Microprocessor, network processor, DSP memory
- DDR Separate I/O optimized for 1 address/clock 2-word burst systems
  - Minimized bus latency, maximized frequency

QDRII+/DDRII+ Overview

What is it?

- Latest QDR Consortium Defined QDR SRAM

Why do you care?

- Frequency Support up to 500MHz
- Simplify Board Design

What are the Main Differences to QDRII?

- Read Latency of 2.0 Offered for Latency Critical Applications
- Read Latency of 2.5 Offered for Frequency Critical Applications
- Data Valid Pin

What Densities? Speeds?

- 18M, 36M, 72M, 144M
-

	Maximum CY Frequency	
Technology	2.0 Cycle Latency	2.5 Cycle Latency
90-nm	375MHz	400MHz
65-nm	400MHz	500MHz

QDRII+/DDRII+ Overview

QDRII+/DDRII+ Differences to QDRII/DDRII

	QDR II / DDRII	QDRII+ / DDRII+	Remark
Frequency (DLL ON)	119MHz~333MHz	300MHz~500MHz	
Organization	x8, x9, x18, x36	x9, x18, x36	
VDD	1.8V +/-0.1V	1.8V +/-0.1V	
VDDQ	1.8V+/-0.1V or 1.5V+/-0.1V	1.5V +/-0.1V	
Read Latency	1.5 clocks	2.0 & 2.5 clocks	QDRII+ read latency is not user selectable. Offered as two different devices.
Input Clocks	Single Ended (K,K#)	Single Ended (K,K#)	
Output Clocks(C,C#)	Yes	No	
A0 (DDR B2)	Yes	No	
Echo Clock Number	1 Pair	1 Pair	Echo Clocks are Single Ended.
PKG	165 ball FBGA	165 ball FBGA	
Individual Byte Write (BWa#,BWb#)	Yes	Yes	
QVLD	No	Yes	Edge Aligned with Echo Clocks

Guide to Support QDRII/DDRII & QDRII+/DDRII+

QDR & DDR Pinout

- P6 – Design to use as C Clock or QVLD
- R6 – Design to use as C# Clock or No Connect

DDR B2 Specific Pinout

- Design Controller to Always Start the Access/Burst with A0 = 0
  - A0 Becomes a No Connect with DDRII+

I/O Voltage

- Use 1.5V HSTL I/O

Host Design

- Design to Support 1.5, 2.0 and 2.5 Cycles for Read Latencies
  - Write Latency Remains 1.0 Cycle for QDRII & QDRII+
- Recommend to use Echo Clocks to Latch Read Data

Board Design

- Design to Take Advantage of QValid Output
- Analyze Timing up to 400MHz

QDRII+ (x18) Pinout Differences

QDRII - B4

CY7C1513V18 (4M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	V_{SS}/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

QDRII+ - B4

CY7C1563V18 (4M × 18)–15 × 17 FBGA

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/144M	A	$\overline{WPS}$	$\overline{BWS_1}$	$\overline{K}$	NC/288M	$\overline{RPS}$	A	A	CQ
B	NC	Q9	D9	A	NC	K	$\overline{BWS_0}$	A	NC	NC	Q8
C	NC	NC	D10	V_{SS}	A	NC	A	V_{SS}	NC	Q7	D8
D	NC	D11	Q10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	D7
E	NC	NC	Q11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	D6	Q6
F	NC	Q12	D12	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	Q5
G	NC	D13	Q13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	D5
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	D14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	Q4	D4
K	NC	NC	Q14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	D3	Q3
L	NC	Q15	D15	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	Q2
M	NC	NC	D16	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	Q1	D2
N	NC	D17	Q16	V_{SS}	A	A	A	V_{SS}	NC	NC	D1
P	NC	NC	Q17	A	A	QVLD	A	A	NC	D0	Q0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

DDRII+ (x18) Pinout Differences

DDRII - B2

CY7C1418AV18 (2M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	A0	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	C	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	$\overline{C}$	A	A	A	TMS	TDI

DDRII+ - B2

CY7C1268AV18 (2M x 18)

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	NC/72M	A	R/$\overline{W}$	$\overline{BWS_1}$	$\overline{K}$	NC/144M	$\overline{LD}$	A	A	CQ
B	NC	DQ9	NC	A	NC/288M	K	$\overline{BWS_0}$	A	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	A	NC	A	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{DOFF}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	A	A	A	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	A	A	QVLD	A	A	NC	NC	DQ0
R	TDO	TCK	A	A	A	NC	A	A	A	TMS	TDI

PERFORM

Architecture Comparison

Parameter	Std. Sync	NoBL™,	DDR / DDR-II/DDRII+	QDR™ / QDR™-II/ QDR™-II+
Data Rate	Single	Single	Double	Double
Data Bus	Common I/O	Common I/O	Common I/O* & Separate I/O**	Separate I/O
Data Bus Utilization	NOP between reads & writes	100%***	NOP between reads* / 50% of Separate I/Os**	100% reading & 100% writing
V_{DD}	3.3V / 2.5V	3.3V / 2.5V	2.5V / 1.8V	2.5V / 1.8V
V_{DDQ}	LVTTL 3.3V / 2.5V	LVTTL 3.3V / 2.5V / 1.8V	HSTL (1.5V / 1.8V)	HSTL (1.5V / 1.8V)
Clock Frequency	250 MHz	250 MHz	200 MHz / 300 MHz/400MHz	200 MHz / 300 MHz/400MHz

* DDR & DDR-II CIO have a common bus and require 1-2 NOP(s) between reads and writes.

** DDR-II SIO has separate input and output buses. Because only one bus can be used at a time, bus utilization is exactly 50%.

*** Applies to clock frequency $\leq$ 166 MHz. Clock frequencies above this typically requires an NOP.