Generated Project Datasheet – PsoC Create 3.1 SP2 14 Apr 2015

CY8C5268AXI-LP047

Hardware Pins / Hardware Ports / Software Pins ALL show:

D- as P15[6] (Pin 35)
D+ as P15[7] (Pin 36)

TRM for PSoC5LP and

2.1 Hardware Pins

34	P5[7]	GPIO [unused]			HiZ Analog Unb
35	P15[6]	USB:D-	Reserved		
36	P15[7]	USB:D+	Reserved		
37	VDDD	VDDD	Power		
38	VSSD	VSSD	Power		
39	VCCD	VCCD	Power		
42	P15[0]	XTAL:Xi	Reserved		
43	P15[1]	XTAL:Xi	Reserved		

2.2 Hardware Ports

P15[4]	93	GPIO [unused]			HiZ Analog Unb
P15[5]	94	\PD:j1HY28B:iTSS\	Dgtl Out	Strong drive	HiZ Analog Unb
P15[6]	35	USB:D-	Reserved		
P15[7]	36	USB:D+	Reserved		
P2[0]	95	GPIO [unused]			HiZ Analog Unb
P2[1]	96	GPIO [unused]			HiZ Analog Unb

2.3 Software Pins

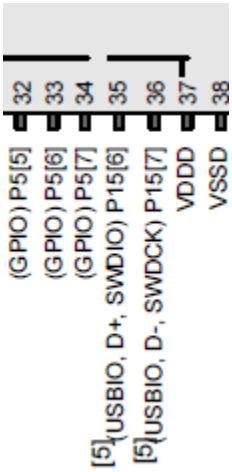
Debug:SWD_CK	P1[1]	Reserved	
Debug:SWD_IO	P1[0]	Reserved	
Debug:SWV	P1[3]	Reserved	
USB:D-	P15[6]	Reserved	
USB:D+	P15[7]	Reserved	
XTAL:Xi	P15[0]	Reserved	
XTAL:Xi	P15[1]	Reserved	

Datasheet for PSoC5LP and CYDRW show:

D- as P15(7) (Pin 36)

D+ as P15(6) (Pin 35)

Datasheet



CYDRW