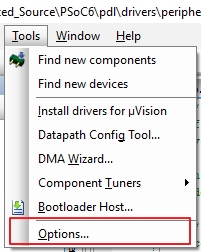
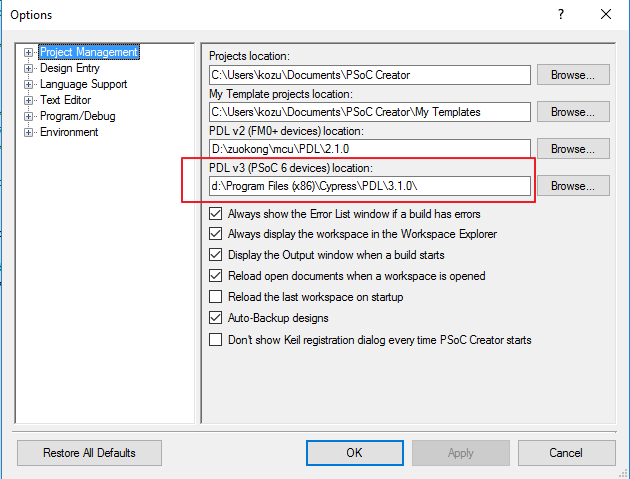
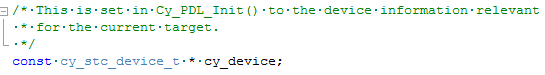
The following steps guide that how to create and modify project. Note: the BLE only use CM0+ core in this example.

1. New BLE upgradable stack project based on CE220960.
2. Modify the PDL v3 location

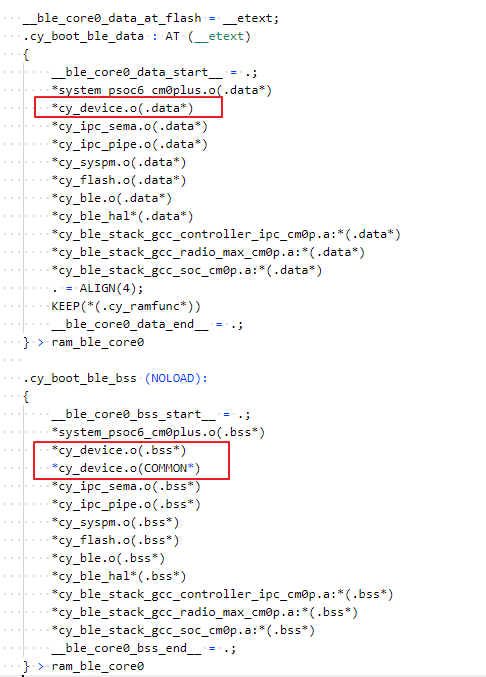
 

1. Modify stack application (APP1) linker file

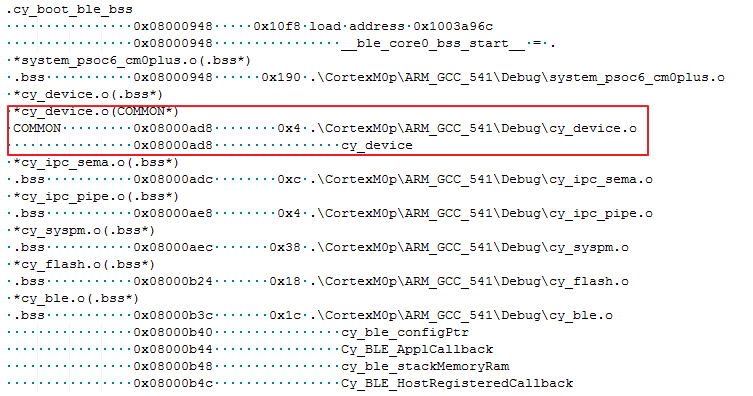
In the PDL 3.1.0, add Cy\_PDL\_Init() function, this function initializes the platform and peripheral block configuration for the given target device, this function will set cy\_device pointer. The SystemInit() function will call Cy\_PDL\_Init() to the device information relevant for the current target.



When user application (APP2) is running, APP2 will call BLE stack function of APP1, BLE stack function still call PDL peripheral driver function of APP1, we need to ensure that the cy\_device pointer is initialized, so we define this pointer to BLE core ram section. The following section is added to dfu\_cm0p.ld file. If you don't modify it, the user application will hard fault on Cy\_BLE\_Start().

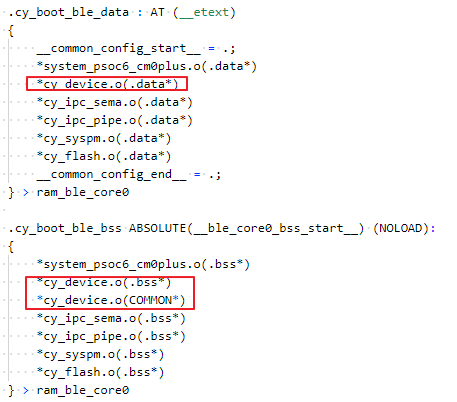


After build, this pointer will location to BLE core ram.

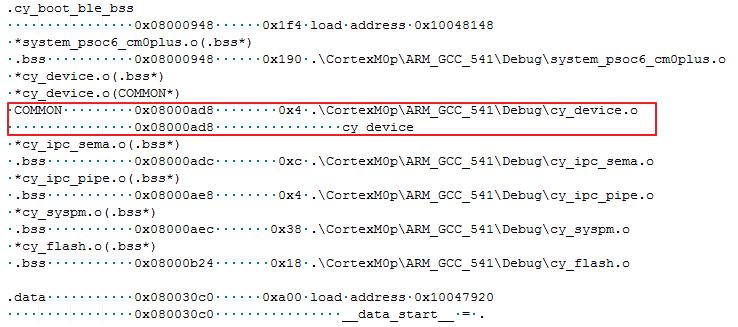


1. Modify user application (APP2) linker file

Similarly, we need to modify the user application linker file to location the cy\_device pointer to same address (BLE core ram).



The following is map file of APP2 project.



According to the above modifications, the CE220960 can running in the PDL 3.1.0.