I2C_SCR register content(ISR Entry Time Value) = 0x11 (ACK bit = 1, BYTE_COMPLETE bit = 1)

Since BYTE_COMPLETE bit= 1 therefore its a data byte, EzI2C user module will write 0x10 to I2C_SCR register to ACK the data byte. Writing 0x10 also clears all other status bits along with BYTE_COMPLETE bit which is essential for the generation of upcoming byte complete interrupts

I2C_SCR register content(ISR Exit Time Value) = 0x10 (ACK bit = 1, BYTE_COMPLETE bit = 0)

I2C_SCR register content(ISR Entry Time Value) = 0x30 (ACK bit = 1, STOP_STATUS bit= 1)

Since STOP_STATUS bit is set therfore EzI2C user module state machine will go through the logic wherein it will try to clear the stop status bit by doing an and operation on SCR register

Clearing STOP_STATUS bit here will not clear the stop status bit since stop status bit can be cleared only if BYTE_COMPLETE bit is set to '1'. Hence ISR exit time I2C_SCR register content will be 0x30 itself.

Writing to I2C_SCR register b/w a start and next byte complete(to be precise writing '0' to address bit of SCR register) will cause the start staus (I2C block internal status bit) to get reset which in turn resulting in 'not' setting the address bit upon reception of the address byte (in other words the received address byte will be misinterpreted as a data byte and therefore PSoC sends an ACK signal)

Solution: Do not do any data write operation to SCR register during the time frame b/w start and immediate byte complete

I2C_SCR register content(ISR Exit Time Value) = 0x30 (ACK bit = 1, STOP_STATUS bit = 1)

Interrupt is not generated here since BYTE_COMPLETE bit set to '1' in the previous ISR , clock is stretched low

I2C_SCR register content(ISR Entry Time Value) = 0x31 (ACK bit = 1, STOP_STATUS bit= 1, BYTE_COMPLETE bit = 1, ADDRESS bit = 0)

Note that ADDRESS bit is not set here, since ADDRESS bit is not set and STOP_STATUS bit is set the EzI2C state machine will go through the logic wherin it will try to clear the STOP_STATUS bit, this time stop status bit will be cleared since BC is set to 1. This operation will also set the ACK bit & BYTE_COMPLETE bit so whatever be the address received the slave will send acknowledgment signal

I2C_SCR register content(ISR Exit Time Value) = 0x11 (ACK bit = 1, STOP_STATUS bit= 0, BYTE_COMPLETE bit = 1, ADDRESS bit = 0)