Converting STK10C68 to STK12C68

Introduction

This document provides guidance on converting a design that is currently using the STK10C68 to the Simtek recommended part STK12C68.

Feature set and limitations of the STK10C68

Function Category	STK10C68	STK12C68
Autostore	no	Yes, but can be disabled
Software store	No, (yes but undocumented)	Yes
Software recall	No, (yes but undocumented)	Yes
Hardware store HSB based	No	Yes
Hardware store NE based	Yes	No

Package Comparison

The 600 mil dip package is available in the STK12C68 and the STK10C68.
Other packages that take less PCB area also exist such as 300 mil CDIP/PDIP and the 350 mil SOIC.

Package	PKG Code	STK10C68	STK12C68	Notes
350 mil SOIC – 28 pin	S	Available	Available	Surface mount – smallest PCB area
600 mil pdip -- 28 pin	W	Not Available	Not Available	Through hole
300 mil pdip -- 28 pin	P	Available	Not Available	Through hole
300 mil cdip -- 28 pin	C	Not Available	Not Available	Through hole

Issues to consider during the conversion

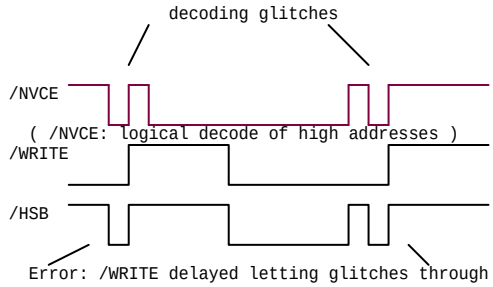
The key difference is that the STK10C68 has a different hardware store mechanism than the STK12C68. STK12C68 will normally autostore so powering via VCAP and having VCCx open will prevent autostore. Logic explained here creates a signal to activate /HSB(hardware store) by combining the /G, /NE, /E, and /W signals used with the STK10C68. This will activate the same feature as in the STK12C68 (NE based hardware store) by instead activating /HSB.

It is essential that the logic output be glitch free. In many implementations, /NE and /E signal is usually a logic decode of uppermost addresses and any decode from multiple address lines can glitch. /W signal is usually falling later in the cycle glitch-free strobe from the MPU. Please check that there is sufficient time from address change to /W falling to gate out /E and /NE glitches. This will ensure glitch free leading edge. Also, be sure that /W rises before the address changes. (Delay in the /W signal can cause problems for the rising edge.) This is the normal situation for most MPUs (check your MPU datasheet). The /HSB signal should go low only when /G is high and /E, /NE, and /W are all low. This low going pulse will activate the /HSB input which initiates a hardware store when low just like the STK10C68 does in response to /G being high, /NE, /E, and /W being low.

Hardware recall is not supported in this conversion. There is no external pin on the STK12C68 to support hardware recall. Recall is automatic on power up so is in most cases not needed or used. If needed, contact Simtek applications engineering for recommendations.

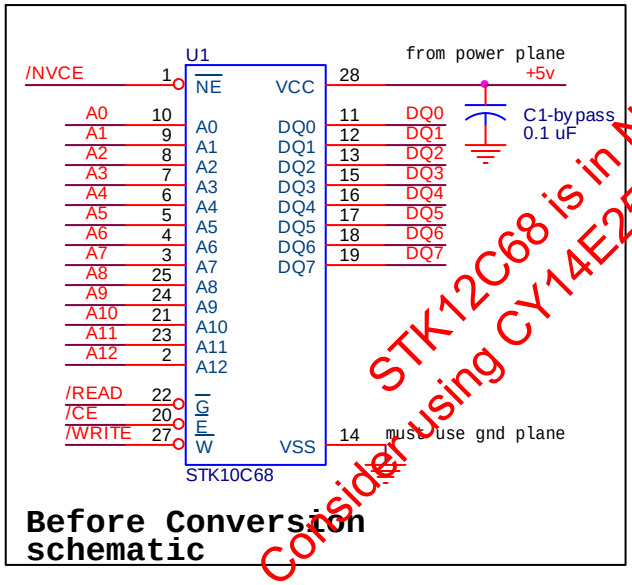
Improper Timing example

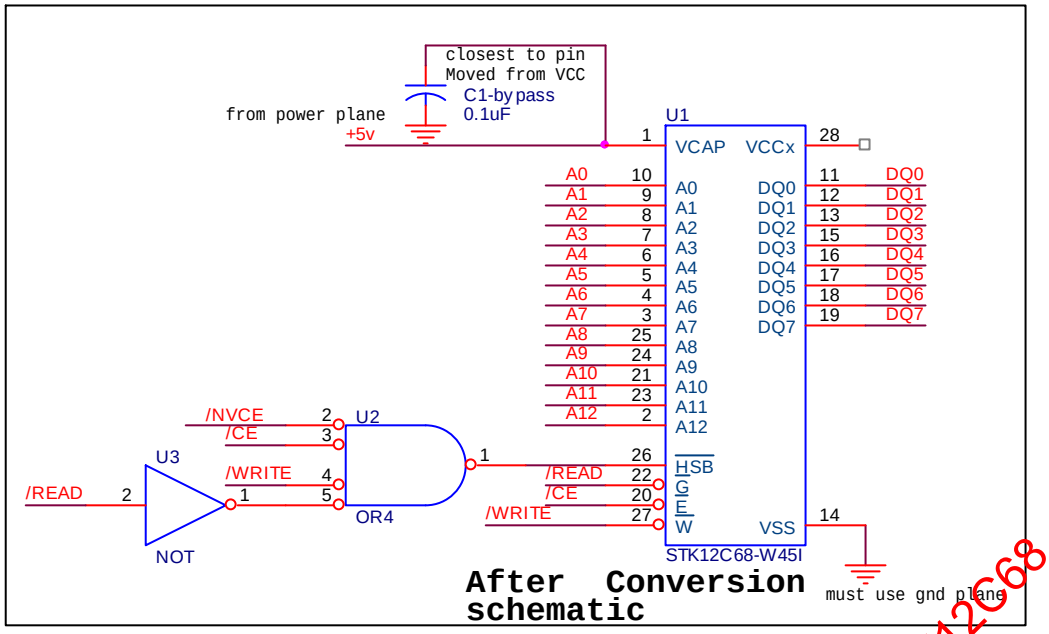
The following timing diagram shows an unwanted situation just before the low going write pulse. /HSB output from the OR gate should not glitch by having /WRITE extend into the next cycle. This can occur if there are too much delay in the /WRITE signal. Normally, /WRITE output from an MPU will terminate well before any address change. Be sure to check the timing of address changes to /WRITE rising. This time should always be negative and any positive values risk activating /HSB inadvertently.



Schematic changes for conversion:

The larger memory is used with identical function but with two high order address bits tied inactive. The choice of package is open with the “S” package being the most area efficient surface mount choice.





On the next page, pin by pin comparisons of the two show all pins are the same except for the two additional address lines.

Corresponding pin Connection

Pin for pin comparison of the two parts is given in the table below:

STK10C68 NAME	STK12C68 NAME	Pin	Comments
/NE	VCAP	1	Hook VCAP to system VCC Unhook /NE and connect to OR gate input (see schematic)
A12	A12	2	No change
A7	A7	3	“
A6	A6	4	“
A5	A5	5	“
A4	A4	6	“
A3	A3	7	“
A2	A2	8	“
A1	A1	9	“
A0	A0	10	“
DQ0	DQ0	11	“
DQ1	DQ1	12	“
DQ2	DQ2	13	“
VSS	VSS	14	“
DQ3	DQ3	15	“
DQ4	DQ4	16	“
DQ5	DQ5	17	“
DQ6	DQ6	18	“
DQ7	DQ7	19	“
E#	E#	20	Connect to OR gate input (See schematic)
A10	A10	21	“
G#	G#	22	Connect to OR gate input (See schematic)
NC	A11	23	No change
A9	A9	24	No change
A8	A8	25	“
HSB	HSB	26	Connect to OR gate output (see schematic above)
W#	W#	27	Also connect to OR gate input
VCC	VCCX	28	12C68 VCCx should be open