Voltage Controlled Oscillator in PSoC® 3 / PSoC 5

Objective

This project demonstrates how to create a voltage controlled oscillator in PSoC® 3 / PSoC 5.

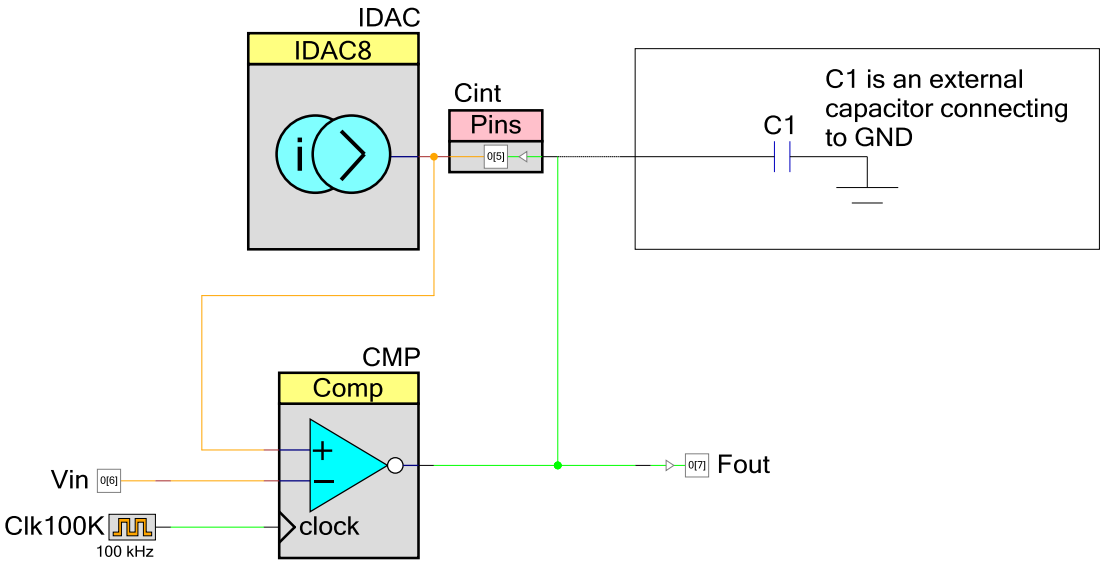
Overview

This code example explains how to create a voltage controlled oscillator with few PSoC 3 / PSoC 5 resources and an external capacitor.

Top Design

Figure 1 shows the components and their routing:

Figure 1. Component Routing



Operation

Following operations are performed in *main.c*

- Start IDAC
- Set IDAC current to 100uA
- Start the comparator

After these resources are started, no more firmware intervention is required.

Pin "Cint" P0[5] is configured as both Digital and Analog pin with a drive mode Open Drain drives low. When output of Comparator is High, IDAC output is connected to the pin. When comparator output is Low, the pin shorts to Ground.

IDAC – configured as a current source – charges the external capacitor connected to "Cint". When the capacitor voltage crosses input voltage Vin, comparator output becomes low (comparator is set for inverted logic) and

discharges the capacitor. As capacitor voltage becomes zero, the comparator output becomes high and IDAC starts charging the capacitor. The cycle continues and we get an oscillator whose frequency is inversely proportional to Vin. The circuit has excellent “Period vs. Vin” linearity. The period of the output waveform is directly proportional to the input voltage. The frequency output of the circuit can be found from the formula:

$$F = \frac{1}{\left(\frac{C * V}{I}\right) + t_{disch}}$$

Where:
F = Output Frequency
C = Capacitor
V = Input voltage
I = IDAC current
t_{disch} = Period of the Comparator’s Synch clock

The period of the synchronizing clock to the comparator should be long enough to discharge the capacitor. Too high a clock frequency, the capacitor may not discharge completely. Too low a clock frequency, the term t_{disch} dominates the denominator of the equation and reduces the linearity.

The value of the clock also depends on the value of the capacitor. Higher value of capacitor requires a longer discharge time.

Hardware Connections

Make the following connections on the CY8CKIT-001 PSoC Development Kit:

Connect a 0.1 uF capacitor between P0[5] (on header P19) and GND

Connect VR on header P14 to P0[6] on header P19

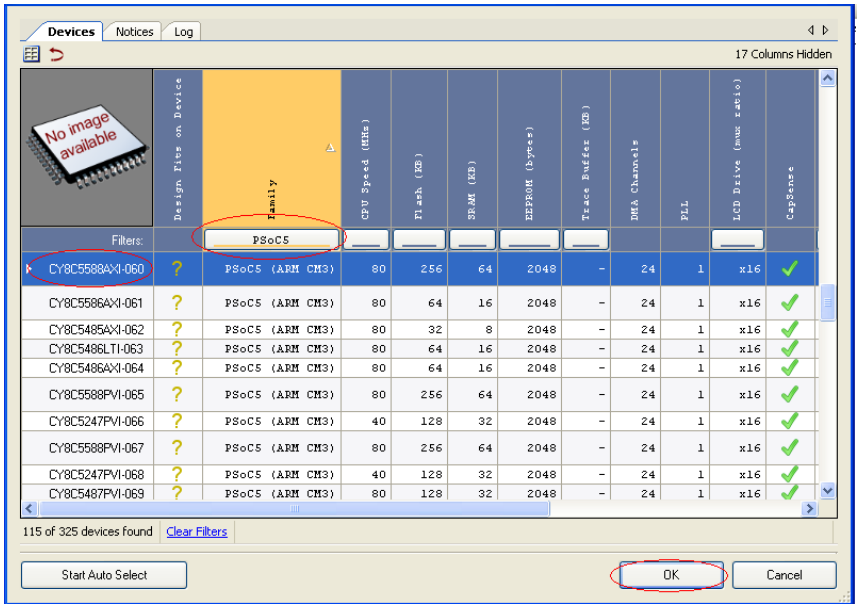
The frequency output is available on P0[7]

Output

Build the project and program the PSoC 3 device.

Note. The default device selection in the project is PSoC 3 (CY8C3866AXI-040). To use this project with PSoC 5 device, do the following:

Go to **Project → Device Selector →** Select **PSoC 5** device (CY8C5588AXI-060), build the project again and program the PSoC 5 device as follows:


Devices
Notices
Log
17 Columns Hidden
No image available
Design Files on Device
Family
CPU Speed (MHz)
Flash (KB)
SRAM (KB)
EEPROM (bytes)
Trace Buffer (KB)
DMA Channels
PLL
LCD Drive (mux ratio)
CapSense
Filters:
PSoC5
CY8C5588AXI-060 PSoC5 (ARM CM3) 80 256 64 2048 - 24 1 x16
CY8C5586AXI-061 PSoC5 (ARM CM3) 80 64 16 2048 - 24 1 x16
CY8C5485AXI-062 PSoC5 (ARM CM3) 80 32 8 2048 - 24 1 x16
CY8C5486LTI-063 PSoC5 (ARM CM3) 80 64 16 2048 - 24 1 x16
CY8C5486AXI-064 PSoC5 (ARM CM3) 80 64 16 2048 - 24 1 x16
CY8C5588PVI-065 PSoC5 (ARM CM3) 80 256 64 2048 - 24 1 x16
CY8C5247PVI-066 PSoC5 (ARM CM3) 40 128 32 2048 - 24 1 x16
CY8C5588PVI-067 PSoC5 (ARM CM3) 80 256 64 2048 - 24 1 x16
CY8C5247PVI-068 PSoC5 (ARM CM3) 40 128 32 2048 - 24 1 x16
CY8C5487PVI-069 PSoC5 (ARM CM3) 80 128 32 2048 - 24 1 x16
115 of 325 devices found
Clear Filters
Start Auto Select
OK
Cancel

Reset the device by pressing SW4 (Reset switch). Change Vin by adjusting VR and observe the Frequency output change on P0[7]. Below snapshots shows the output waveform at different pins.

Ch1 (Yellow) – FOUT (P0[7])

Ch2 (Blue) – Voltage across Capacitor (P0[5])

Ch3 (Pink) – VR (P0[6])

The screenshot on the left is with Vin = 1 V and the screenshot on the right is with Vin = 3 V