Designing for QDRII/DDRII and QDRII+/DDRII+

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Introduction

Memory devices are evolving to match the needs of applications which are in continuous demand like higher performance communications, networking, and digital signal processing (DSP) systems. Specialized memory products that optimize memory bandwidth for a specific system architecture are successful in increasing the overall performance in a variety of data processing systems. Operating speeds have increased beyond 400 MHz. The next generation of the QDR family of SRAMs released by the QDR consortium meets these requirements. The QDRII+ and DDRII+ products offers improved speeds up to 50 percent faster than the existing QDRII and DDRII products. QDRII+ and DDRII+ products deliver a higher bandwidth than QDRII and DDRII respectively – up to 72 Gbps, while using the same footprints and a 165 pin FBGA (Fine-pitch Ball Gate Array) package. The QDRII+/DDRII+ architecture leverages existing infrastructures to create higher performing products and allow a direct transition to higher frequencies.

The QDR and DDR families of SRAM provides designers with a complete memory solution for almost any network application. The QDRII/QDRII+ devices has two ports operating independently at twice the selected clock rate, allowing a transfer of four data words across the two ports in a single clock cycle. The DDRII/DDRII+ devices allows double data rate transfers over a common IO data bus.

This application note contains information on the differences between the QDRII/DDRII and QDRII+/DDRII+ devices and contains guidelines on how to design for both. For specific design guidelines on the QDRII/DDRII family of SRAMs, refer to the "*QDRII Design Guide Application Note*".

This document is based upon that the reader is familiar with the QDRII/DDRII device and its design requirements.

- Description of the QDRII+/DDRII+
- Differences between QDRII/DDRII and QDRII+/DDRII+ functionality and timing
- Design changes required to accommodate both QDRII/DDRII and QDRII+/DDRII+

Description of QDRII+/DDRII+ SRAM

Cypress, along with the other QDR consortium members, defined the QDRII+/DDRII+ SRAM architecture for high performance communications systems supporting up to 500 MHz frequencies. The QDRII+/DDRII+ SRAM devices are an extension of the existing QDRII/DDRII family of SRAMs in terms of frequency and performance.

The QDRII+/DDRII+ SRAM devices are similar in functionality to a QDRII/DDRII+ SRAM. The timing of the QDRII+/DDRII+ devices is slightly different from the QDRII/DDRII devices. However with similar functionality and only few changes to the host controller and the board, both these parts can be used interchangeably depending on the application. Designing to both QDRII/DDRII and QDRII+/DDRII+ paves the path for higher performance in the existing QDRII/DDRII designs.

Differences between QDRII/DDRII and QDRII+/DDRII+ Functionality and Timing

Functionally, the QDRII/DDRII and the QDRII+/DDRII+ devices are same. However, they do have certain differences in AC and DC parameters due to the higher speeds of operation in QDRII+/DDRII+

The major changes are:

- Higher Read Latency: Higher read latency enabled achieving higher frequency of operations. The QDRII/DDRII has a latency of 1.5 cycles and the QDRII+/DDRII+ supports both 2.0- and 2.5- cycle latencies (the latency is not user selectable within a device. Devices with different latencies have different part numbers.)
- Output clocks C and C# are removed: At high speeds (above 250 MHz), CQ clocks are recommended to latch data. In such cases, it is not required for the customer to implement the C clocks.
- QVLD pin: For easier board design, a QVLD (Output Valid Indicator) pin is added. The QVLD is edge aligned to the echo clocks and is issued half a cycle prior to the valid data.
- Linear Burst Addressing is Removed: In DDRII, there is a feature "Linear Burst addressing" which is used to select between the banks for complete flexibility. In DDRII+, this feature is removed as it is not possible to meet the higher speeds with this feature enabled.
- Pinout changes: In the QDRII device, the pins P6 and R6 are used as C and C# clocks. In QDRII+, the P6 is used as the QVLD pin and R6 is a NC (No connect). In DDRII+, since the linear burst addressing is not supported, the pins A0 and A1 are NCs.

- **Miscellaneous:**
  - The DLL lock time is changed from 1024 to 2048 cycles
  - The tKHK#H (K clock rising edge to K# clock rising edge) parameter is modified to be 42.5% from 45% of the input clock cycle.

A summary of all the differences is listed in Table 1. For more information on the AC timing and DC parameters, refer to the data sheets of the respective devices.

Table 1. Differences between QDRII/DDRII and QDRII+/DDRII+

	QDR II / DDRII	QDRII+ / DDRII+	Remark
Frequency (DLL ON)	119 MHz~300 MHz	300 MHz~400 MHz	
Organization	x8, x9, x18, x36	x18, x36	
VDD	1.8V +/–0.1V	1.8V +/–0.1V	
VDDQ	1.8V+/–0.1V or 1.5V+/–0.1V	1.8V+/–0.1V or 1.5V+/–0.1V	
Read Latency	1.5 clocks	2.0 & 2.5 clocks	QDRII+/DDRII+ read latency is not user selectable. Offered as two different devices.
Input Clocks	Single Ended (K,K#)	Single Ended (K,K#)	
Output Clocks (C,C#)	Yes	No	
A0 (DDR B2)	Yes	No	
A0, A1 (DDR B4)	Yes	No	
Echo Clock Number	1 Pair	1 Pair	Echo Clocks are Single Ended.
PKG	165 ball FBGA	165 ball FBGA	
Individual Byte Write (BWa#,BWb#)	Yes	Yes	

Design Changes Required to Accommodate both QDRII/DDRII and QDRII+/DDRII+

QDRII+/DDRII+ provides a higher speed path for most applications. It is advantageous to customers to implement certain design changes in their existing designs to enable designing to both QDRII/DDRII and QDRII+/DDRII+ devices. Most of the changes mentioned in the earlier section can be met without a lot of changes to the board.

The changes can be categorized as:

1. Pinout Changes
2. Host Controller Changes
3. Board Changes

Pinout Changes

- QDRII: The pins which were C and C# clocks in the QDRII are replaced by a NC and the QVLD pin in the QDRII+. This requires the designs not use the output clocks C and C#. Also, the pin P6 should be pulled high with a 1 KΩ resistor. This will help in disconnecting the resistor to float the pin when QDRII+ is designed.
- DDRII: As the linear burst addressing is not present in DDRII+, the pins A0 and A1 are no connects. This is a minor change compared to the rest of the changes because the pins are internally bonded so their connection state does not matter. They can be connected to any value or left floating.

Host Controller Changes

- Change of latency from 1.5 cycles to 2.0 and 2.5 cycles: In the QDRII+, the read latency is increased to 2 and 2.5 cycles from the QDRII where the read latency is only 1.5 cycles. The host controller should be able to support either 2 or 2.5 cycles of latency (it does not have to support both latencies because each part only supports one latency). The choice between the 2.0 and 2.5 cycles of read latency should be made early in the design definition phase, based on the bandwidth and the host controller capabilities.
- Echo clocks to latch read data: CQ if in the existing design, the design uses the K or the C clocks to latch the read data. This should be modified to use the CQ clocks to latch the data.

Board Changes

- Higher performance: The board should be designed to support speeds up to 400 MHz.
- Output valid indicator: The board should be modified to include the QVLD signal and to take advantage of it when QDRII+ is designed.

Conclusion

QDRII+/DDRII+ devices provide the ability to achieve high performance and bandwidth with few changes to existing boards as well as the ability to create new designs. By designing boards and host controllers to meet both QDRII/DDRII and QDRII+/DDRII+ requirements, systems can support high performance of up to 400 MHz or 72 Gbps bandwidth in the next generations without any changes to the existing boards or host controllers.

In March of 2007, Cypress recataloged all of its Application Notes using a new documentation number and revision code. This new documentation number and revision code (001-xxxxx, beginning with rev. **), located in the footer of the document, will be used in all subsequent revisions

QDR RAMs and Quad Data Rate RAMs comprise a new family of products developed by Cypress, IDT, NEC, Renesas, and Samsung.All other trademarks or registered trademarks referenced herein are the property of their respective owners.

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