High-speed USB PCB Layout Recommendations

AN1168

Associated Project: No
Associated Application Notes: None

Abstract

This application note details guidelines for designing, controlled-impedance; high-speed USB printed circuit boards to comply with the USB specification. This note is applicable to all Cypress high-speed USB solutions. Some Cypress high-speed USB chips have separate application notes that address chip-specific PCB design guidelines.

Introduction

High-speed USB operates at 480 Mbps with 400-mV signaling. For backwards compatibility, devices that are high-speed capable must also be able to communicate with full-speed USB products at 12 Mbps with 3.3 V signaling. High-speed USB hubs are also required to talk to low-speed products at 1.5 Mbps. Designing printed circuit boards (PCBs) that meet these requirements can be challenging.

High-speed USB is defined in the Universal Serial Bus Specification Revision 2.0, located at http://www.usb.org. The organization that oversees the specification is the USB Implementers Forum. The USB-IF requires that all devices receive testing to show compliance to the specification and to ensure interoperability with other devices. Cypress recommends that designers pre-test their products for USB compliance before attending a USB Compliance Workshop.

This application note details guidelines for designing, controlled-impedance, high-speed USB printed circuit boards to comply with the USB specification. This note is applicable to all Cypress high-speed USB solutions. Some Cypress high-speed USB chips have separate application notes that address chip-specific PCB design guidelines.

High-speed USB PCBs are typically 4 or more layers boards. Cypress does not recommend using a 2-layer board for high-speed USB PCB design.

PCB design influences USB signal quality test results more than any other factor. This application note addresses five key areas of high-speed USB PCB design and layout:

- Controlled Differential Impedance
- USB Signals
- Power and Ground
- Crystal or Oscillator
- Troubleshooting

Controlled Differential Impedance

Controlled differential impedance of the D+ and D– traces is important in USB PCB design. The impedance of the D+ and D– traces affect signal eye pattern, end-of-packet (EOP) width, jitter, and crossover voltage measurements. It is important to understand the underlying theory of differential impedance in order to achieve a 90 Ω ± 10% impedance.

Theory

Microstrips are the copper traces on the outer layers of a PCB. A microstrip has an impedance, Z_o, that is determined by its width (W), height (T), distance to the nearest copper plane (H), and the relative permittivity (ε_r) of the material (commonly FR-4) between the microstrip and the nearest plane.

When two microstrips run parallel to each other cross-coupling occurs. The space between the microstrips (S) as related to their height above a plane (H) affects the amount of cross-coupling that occurs. The amount of cross-coupling increases as the space between the microstrips is reduced. As cross-coupling increases the microstrips' impedances decrease. Differential impedance, Z_{diff}, is measured by measuring the impedance of both microstrips and summing them.

Figure 1. Microstrip Model of Differential Impedance

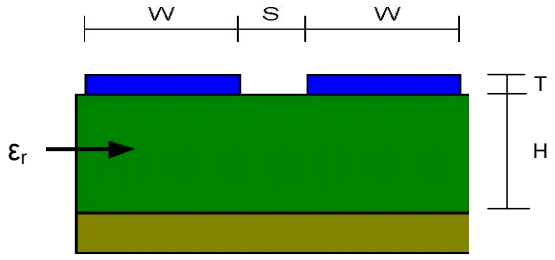


Figure 1 shows a cross-sectional representation of a PCB showing (from top to bottom) the differential traces, the substrate, and the GND plane. Figure 2 provides the formulas necessary for estimating differential impedance using a 2D parallel microstrip model. Table 1 provides the definition of the variables. These formulas are valid for $0.1 < W/H < 2.0$ and $0.2 < S/H < 3.0$. Commercial utilities

can obtain more accurate results using empirical or 3D modeling algorithms.

Figure 2. Differential Impedance Formula

$$Z_{diff} = 2Z_0 (1 - 0.48e^{-0.96\ S/H})$$

$$Z_0 = (87/(\varepsilon_r + 1.41)^{0.5})\ \ln(5.98H/0.8W + T)$$

Table 1. Definition of Differential Impedance Variables

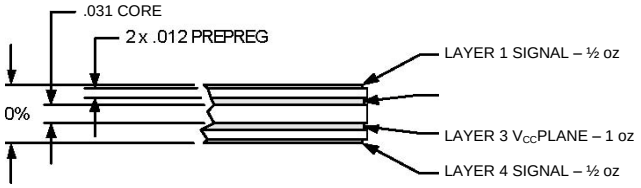
Variable	Description
Zdiff	Differential impedance of two parallel micro-strips over a plane
Z0	Impedance of one microstrip over a plane
W	Width of the traces
H	Distance from the GND plane to the traces
T	Trace thickness ( )1/2 oz copper ≅ 0.65 mils
S	Space between differential traces (air gap)
εr	Relative permittivity of substrate ( )FR-4 ≅ 4.5

Typical 62-mil, 4-layer PCB Example

The recommended stackup for a standard 62-mil (1.6-mm) thick PCB is shown in Figure 3. When this stackup is used with two parallel traces each with a width, W, of 16 mils and a spacing, S, of 7 mils the calculated differential impedance, Z_{diff}, is 87 Ω.

With the same stackup it is possible to achieve a 90 Ω ± 10% differential impedance on D+ and D– using other combinations of variables.

Figure 3. Typical Stackup for a 62-mil, 4-layer PCB



NOTE: .016 TRACES ARE 90-OHM DIFFERENTIAL IMPEDANCE

Recommendations

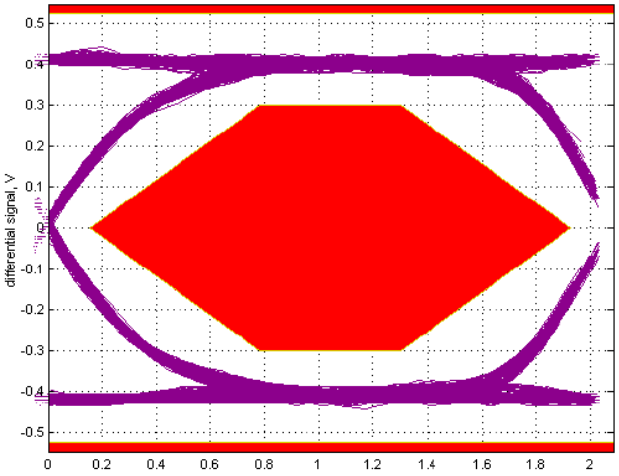
Use the following recommendations to achieve the proper differential impedance:

1. Consult with the PCB manufacturer to obtain the necessary design parameters and stackup to obtain a 90 Ω ± 10% differential impedance on D+ and D–.
2. Set the correct trace widths and trace spacing for the D+ and D– traces in the layout tool.
3. Draw the proper stackup on the PCB Fabrication Drawing and require the PCB manufacturer to follow the drawing. See Figure 3.
4. Annotate the PCB Fabrication Drawing to indicate which trace widths are differential impedance. Also indicate what impedance and tolerance is required.
5. Request differential impedance test results from the PCB manufacturer.

EYE Diagram

One key measurement of USB data signal quality is the eye pattern. The eye pattern is a representation of USB signaling that provides minimum and maximum voltage levels as well as signal jitter. Section 7.1 in the USB 2.0 Specification provides detailed explanation and requirements for a compliant eye pattern. Figure 4 is an eye diagram of high-speed signaling as measured on the EZ-USB FX2LP component.

Figure 4. Eye Diagram of High-speed Signaling



In the diagram, notice how no signal traces overlap the central, six-sided, shaded area. Also, no trace overlaps the extremes of permissible voltage as shown in the shaded lines at the very top and very bottom of the figure. Overlap of signal trace over the shaded areas would be a violation of the USB 2.0 specification. Overlap can be caused by excessive data jitter, mismatched impedance, and improper EMI filtering.

USB Signals

There are five USB signals: VBUS, D+, D–, GND, and SHIELD. Their functions are shown in Table 2.

Table 2. USB Signals

Signal	Description
VBUS	Device power, +5 V, 500 mA (max)
D+ and D–	Data signals, mostly differential
GND	Ground return for VBUS
SHIELD	Cable shielding and receptacle housing

D+ and D–

Properly routing D+ and D– leads to high-quality signal eye pattern, EOP width, jitter, crossover voltage, and receiver sensitivity test results. The following recommendations improve signal quality:

1. Place the Cypress high-speed USB chip on the signal layer adjacent to the GND plane.

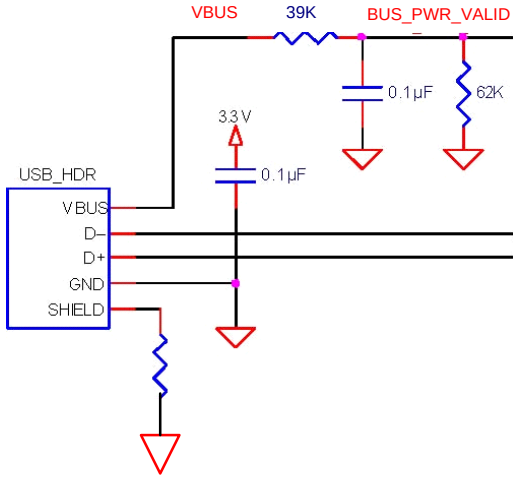
2. Route D+ and D– on the signal layer adjacent to the GND plane.
3. Route D+ and D– before other signals.
4. Keep the GND plane solid under D+ and D–. Splitting the GND plane underneath these signals introduces impedance mismatch and increases electrical emissions.
5. Avoid routing D+ and D– through vias; vias introduce impedance mismatch. Where vias are necessary (e.g., using mini-B connector) keep them small (25-mil pad, 10-mil hole) and keep the D+ and D– traces on the same layers.
6. Keep the length of D+ and D– less than 3 inches (75 mm). A 1-inch length (25–30 mm) or less is preferred.
7. Match the lengths of D+ and D– to be within 50 mils (1.25 mm) of each other to avoid skewing the signals and affecting the crossover voltage.
8. Keep the D+ and D– trace spacing, S, constant along their route. Varying trace separation creates impedance mismatch.
9. Keep a 250-mil (6.5-mm) distance between D+ and D– and other non-static traces wherever possible.
10. Use two 45° bends or round corners instead of 90° bends.
11. Keep five trace widths minimum between D+ and D– and adjacent copper pour. Copper pour when placed too close to these signals affects their impedance.
12. If the Cypress High-speed USB chip requires series termination and pull-up resistors on D+ and D– place their pads on the traces. Avoid stubs. Locate these resistors as close as possible to the chip. See Figure 6 for reference.
13. Avoid common-mode chokes on D+ and D– unless required to reduce EMI. Common mode chokes typically provide little benefit for high-speed signals and can adversely affect full-speed signal waveforms.

VBUS, GND, and SHIELD

These recommendations for the VBUS, GND, and SHIELD signals improve inrush current measurements and reduce susceptibility to EMI, RFI, and ESD.

1. Route VBUS on the signal layer adjacent to the V_{CC} plane. This prevents it from interfering with the D+ and D– signals.
2. Filter VBUS to make it less susceptible to ESD events. This is especially important if the Cypress high-speed USB chip uses VBUS to determine whether it is connected or disconnected from the bus. A simple RC filter works well. See Figure 5 for details. The filter should be placed closer to the USB connector than the USB chip.
3. Use 10 µF or less of capacitance on VBUS to prevent violating the USB inrush current requirements.
4. Connect the SHIELD connection to GND through a resistor. This helps isolate it and reduces EMI and RFI emissions. Keep this resistor close to the USB connector. Some experimentation may be necessary to obtain the correct value.
5. Provide a plane for the USB shield on the signal layer adjacent to the V_{CC} plane that is no larger than the USB header.

Figure 5. Schematic Showing the VBUS Filter, USB SHIELD-to-GND Resistor and Decoupling Capacitor

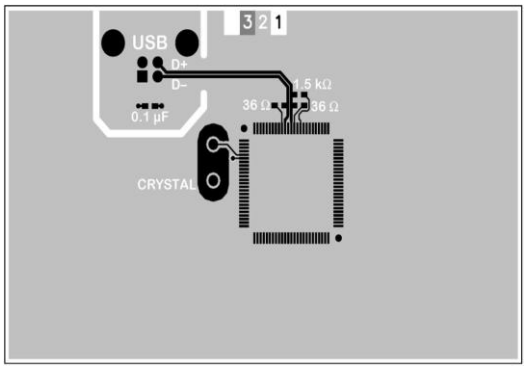


USB Peninsula

If the location of a USB connector is near the edge of the PCB, consider placing it on a ‘USB Peninsula’ as described below. EMI and RFI are decreased by reducing noise on the V_{CC} and GND planes, as they are partially isolated from the rest of the board.

1. Make a cut in the V_{CC} and GND planes around the USB connector leaving a 200-mil (5-mm) opening for D+ and D– to preserve their differential impedance.
2. Use a 0.1-µF capacitor to decouple the V_{CC} and GND planes on the USB peninsula.
3. Place the SHIELD-to-GND resistor on the peninsula. If necessary, a second set of pads that connects SHIELD to the GND plane off the peninsula is useful.
4. Place a common-mode choke (if used, though not recommended) at the opening for D+ and D–.

Figure 6. USB Chip Layout Showing D+/D– Traces, Series Termination Resistors, USB Peninsula, and Crystal



Power and Ground

It is important to provide adequate power and ground for high-speed USB designs. The proper design is as important as layout technique.

V_{CC} and GND Planes

V_{CC} and GND planes are required for high-speed USB PCB design. They reduce jitter on USB signals and help minimize susceptibility to EMI and RFI.

1. Use dedicated planes for V_{CC} and GND.
2. Use cutouts on the V_{CC} plane if more than one voltage is required on the board (e.g., 2.5 V, 3.3 V, 5.0 V).
3. Do not split the GND plane. Do not cut it except as described in 'USB Peninsula.' This reduces electrical noise and decreases jitter on the USB signals.

Power Traces

For situations where it is not necessary to dedicate a split plane to a voltage level (e.g., 5 V or 12 V), but the voltage is required on the board, route a trace instead. The following guidelines are recommended for power traces:

1. Keep the power traces away from high-speed data lines and active components.
2. Keep trace widths at least 40 mils to reduce inductance.
3. Keep power traces short. Keep routing minimal.
4. Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
5. Provide adequate capacitance (see below).
6. Use a chip filter if necessary to reduce noise.

Voltage Regulation

The following guidelines are recommended for voltage regulators to reduce electrical emissions and prevent regulation problems during USB suspend.

1. Select voltage regulators whose quiescent current is appropriate for the board's minimum current during USB suspend.
2. Select voltage regulators whose minimum load current is less than the board's load current during USB suspend. If the current draw on the regulator is less than the regulator's minimum load current then the output voltage may change.
3. Place voltage regulator(s) so they straddle split V_{CC} planes; this reduces emissions.

Decoupling and Bulk Capacitance

1. Provide 0.1-µF ceramic capacitors to decouple device power input pins. Place one cap per pin. Keep the distance from the pad to the power input pin less than 2.0 mm where possible.
2. Place bulk capacitors near the power input and output headers and the voltage regulator(s).
3. Provide 10–20 µF capacitance for the Cypress USB chips. Ceramic or tantalum capacitors are recommended. Electrolytic capacitors are not suitable for bulk capacitance.
4. Filter power inputs and outputs near the power headers to reduce electrical noise.
5. Follow chip-specific guidelines to properly isolate AV_{CC} from V_{CC} and AGND from GND.
6. Follow chip-specific guidelines to provide enough bulk and decoupling capacitance for AV_{CC}. Use ceramic or tantalum capacitors. Electrolytic capacitors are not suitable for bulk capacitance.

Crystal or Oscillator

A crystal or oscillator provides the reference clock for the Cypress high-speed USB chip. It is important to provide a clean signal to the USB chip and to not interfere with other high-speed signals, like D+ and D–.

1. Use a crystal or oscillator whose accuracy is 100 ppm or less.
2. Use a crystal whose first harmonic is either 24 or 30 MHz (depending on the Cypress High-speed USB chip). This requires less crystal start-up circuitry and is less error prone.
3. Place the crystal or oscillator near the clock input and output pins of the Cypress High-speed USB chip.
4. Keep the traces from the crystal or oscillator to the USB chip short.
5. Keep the crystal or oscillator traces away from D+ and D–.
6. Use ceramic capacitors that match the load capacitance of the crystal.

Troubleshooting

The USB electrical compliance tests often show mistakes in PCB layouts. The type of failure can point to the cause. Table 3 shows some common problems and their possible causes for boards that fail high-speed or full-speed signal integrity or high-speed receiver sensitivity tests.

Conclusion

High Speed USB Printed circuit boards must be designed to meet USB electrical requirements. This is best achieved by using controlled impedance PCBs, properly laying out D+ and D–, and adequately decoupling the V_{CC} and GND planes to keep them electrically quiet.

Cypress Semiconductor provides a variety of high-speed USB development and reference design kits. These are helpful to see design examples and contain chip-specific design guidelines.

Table 3. Troubleshooting High-speed USB PCBs

Common Problem	Possible Causes
The high-speed or full-speed signal integrity tests show excessive jitter.	There is an impedance mismatch on D+ and D–.
	A noisy trace is located too close to D+ and D–.
	A common-mode choke is interfering.
	An active component (e.g., voltage regulator, SRAM, etc.) is not properly decoupled.
	AV_{CC} and AGND are not properly isolated or may not have enough bulk capacitance with a low ESR.
The EOP is not detected or out of spec during high-speed or full-speed signal integrity testing.	A common-mode choke is interfering with the EOP.
The crossover voltage is out of the specified range.	The trace lengths of D+ and D– are not matched.
	There is an impedance mismatch on D+ and D–.
The voltage level at the beginning of the high-speed chirp is too high when coming out of suspend.	The voltage regulator is unable to maintain 3.3 V at 100 µA.
Receiver sensitivity is below the acceptable limit.	There is a split in the GND plane underneath D+ and D–.
	A common-mode choke is interfering.
	AV_{CC} and AGND are not properly isolated or may not have enough bulk capacitance with a low ESR.
Inrush current is above the acceptable limit.	Reduce bulk capacitance on VBUS. If designing a bus-powered solution employ a soft-start circuit so all of the capacitance is not filled at once.

Document History

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Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com/