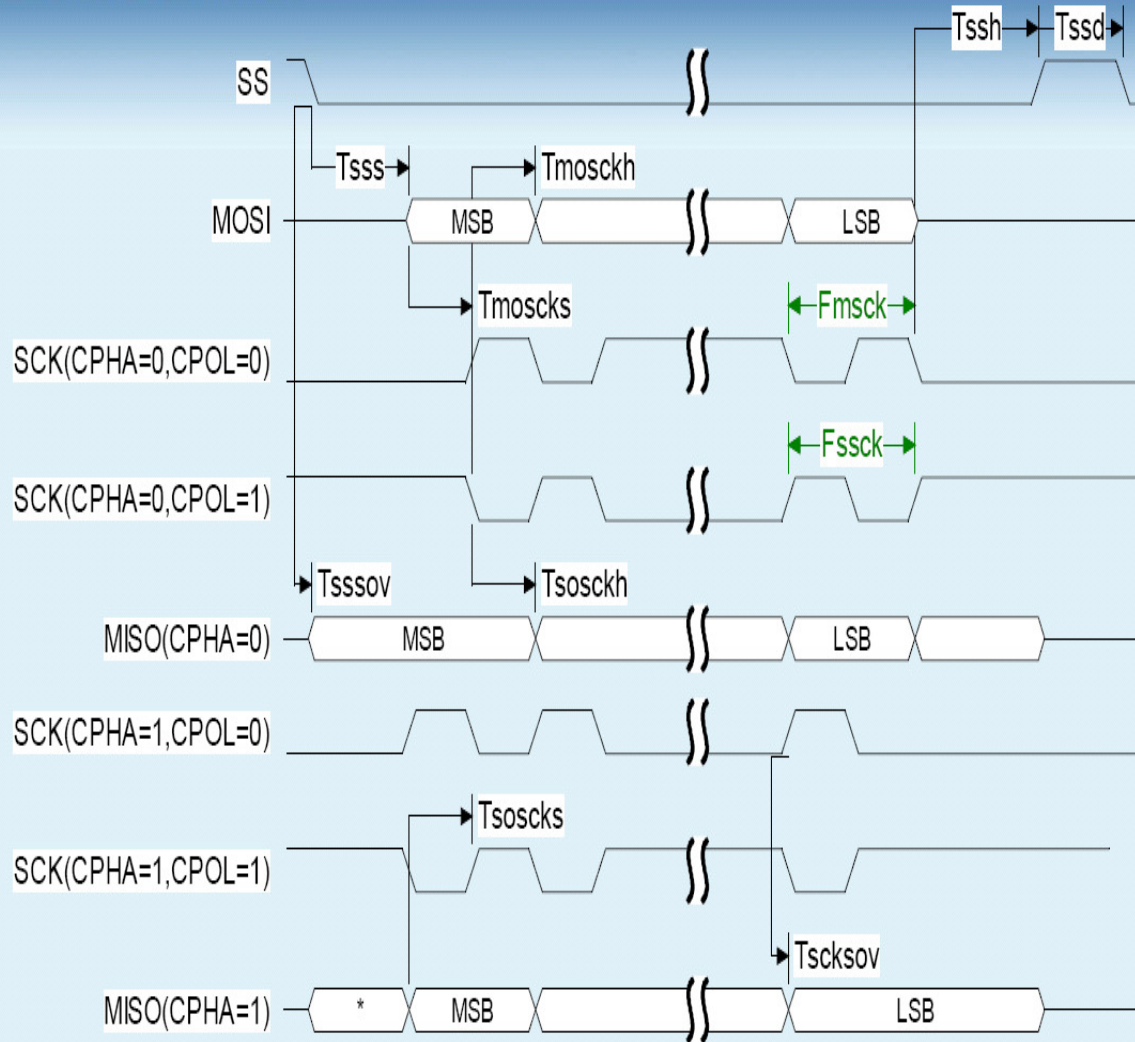




CYPRESS

Connecting From Last Mile to First Mile™

# OTG-Host Block Detail:SPI Timing

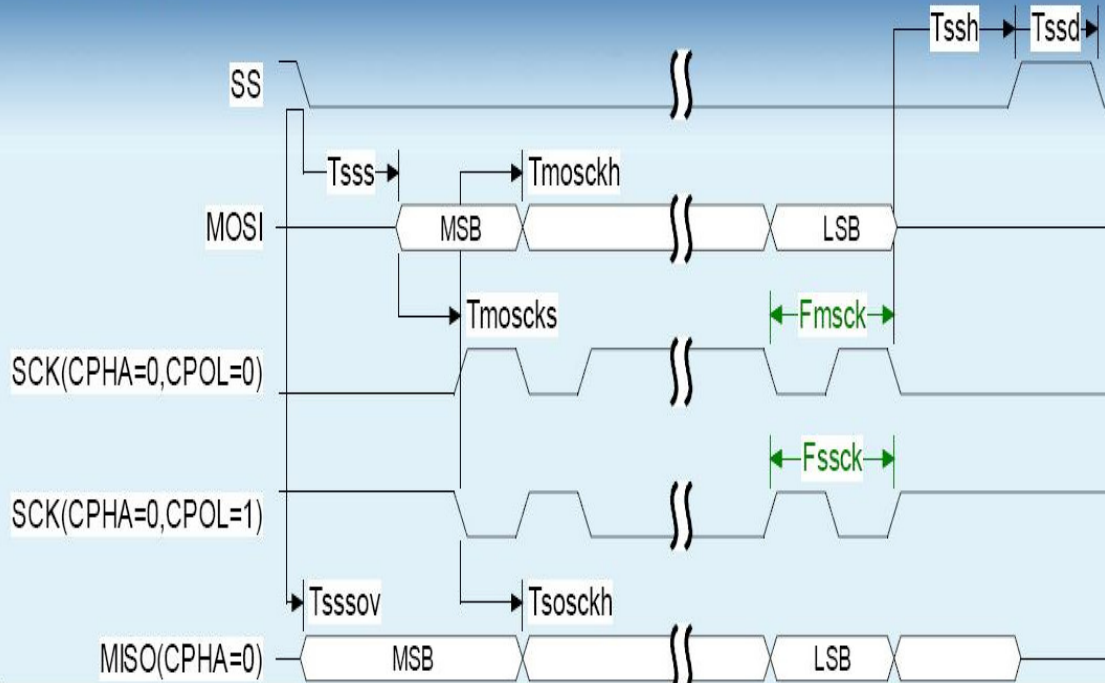




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# OTG-Host Block Detail:SPI Timing

Connecting From Last Mile to First Mile™



Parameter	Description	Min.	Max.	Unit	Conditions
Fmsck	Master SCK Clock Rate	0.25	12.0*	MHz	SPIio Block System Clock @ 48MHz
Fssck	Slave SCK Clock Rate		2.0*	MHz	with clock margin of 10%
Tmoscks	Master Out to SCK Setup time	37.5		ns	Setup to latching SCK clock edge
Tmosckh	Master Out to SCK hold time	37.5		ns	Latching SCK edge to Data invalid
Tsoscks	Slave Out to SCK Setup time	37.5		ns	Setup to latching SCK clock edge
Tsosckh	Slave Out to SCK hold time	37.5		ns	Latching SCK edge to Data invalid
Tsssov	Slave Select to Slave Out Valid		105	ns	SS assertion when CPHA = 0
Tscksov	SCK to Slave Out Valid time		105		
5*Tcyc	ns	Driving SCK edge to Data valid			
Tsss	Slave Select Setup time	125		ns	Slave Configuration
Tssh	Slave Select Hold time	125		ns	Slave Configuration
Tssd	Slave Select Disable time	125		ns	Slave Configuration