Hardware Multiplexing of SAR ADC – PSoC® 5

EP64560
Project Name: HardwareMultiplexing_SAR
Programming Language: C
Associated Part Families: CY8C55xx
Software: PSoC® Creator™
Related Hardware: CY8CKIT-001
Prerequisites: EP61959: 8-Bit ADC Data Buffering Using DMA - PSoC® 3 / PSoC 5, EP62512: Using SAR ADC in PSoC® 5
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Project Objective

The project demonstrates the multiplexing of SAR ADC using hardware multiplexer component.

Overview

When there are several signals to be measured using a single ADC, the ADC needs to be time multiplexed to convert the signals one after the other. In PSoC® 5, SAR ADC can be multiplexed completely in hardware without involvement of CPU, using the hardware multiplexer component (AMuxHw).

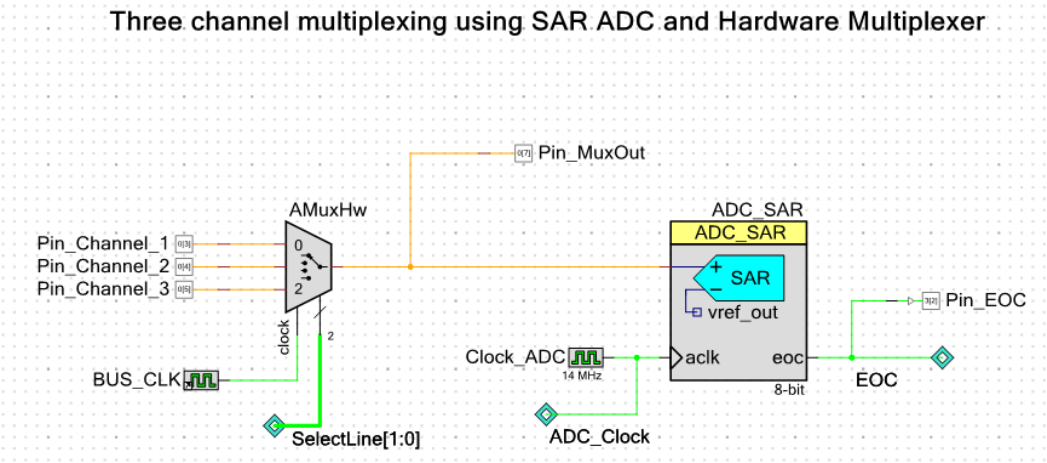
In this example project, three-channel multiplexing is shown. The SAR ADC converts at one Msps speed at 8-bit resolution. Each channel is converted at the rate around 333 Ksps. A DMA is configured to transfer the channel results to voltage DACs. Three different waveforms are given as inputs to the multiplexer and the same waveforms are reproduced at the DAC outputs to verify the working of multiplexing.

Component List

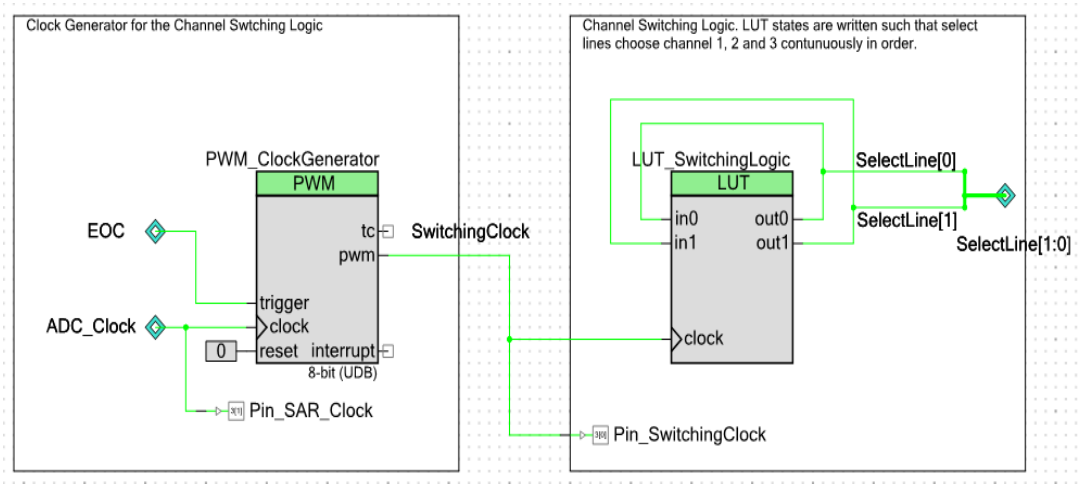
Instance Name	Component Name	Version	Component Category	Comments
ADC_SAR	SAR ADC	1.5	Analog → ADC	The ADC is configured in continuous mode and 8 bit resolution
AMuxHw	Analog Hardware Mux (GPIO)	1.5	Analog → Analog MUX	It is configured for 3 channels
Clock_ADC	Clock	1.5	System	It is set to 14 MHz so that SAR ADC operates at 1 Msps.
Clock_Mux	Clock	1.5	System	It is synchronization clock to AMuxHw. It is set to BUS_CLK
PWM_ClockGenerator	PWM	1.5	Digital → Functions	It is used to generate a clock for the LUT switching logic. A pulse is generated 5 clock cycles after EOC of ADC
LUT_SwitchingLogic	Lookup Table	1.5	Digital →Logic	The LUT changes the select lines to select the next channel. It is given a clock from LUT
DMA	DMA	1.5	System	It is configured to have three TDs. It transfers the ADC result to DACs.
VDAC8_1, VDAC8_2, VDAC8_3	VDAC	1.5	Analog → DAC	It is set in the 4 V range.
Opamp_Buffer_1, Opamp_Buffer_2, Opamp_Buffer_3,	Opamp	1.5	Analog → Amplifiers	The DAC has high output impedance therefore the DAC output is buffered before routed to pin.
Pin_Channel_1, Pin_Channel_2, Pin_Channel_3, Pin_MuxOut, Pin_DAC_1, Pin_DAC_2, Pin_DAC_3	Analog Pin	1.5	Ports and Pins	-
Pin_EOC, Pin_SwitchingClock, Pin_SAR_Clock	Digital Output Pin	1.5	Ports and Pins	These signals are put on the pins for monitoring.

Top Design

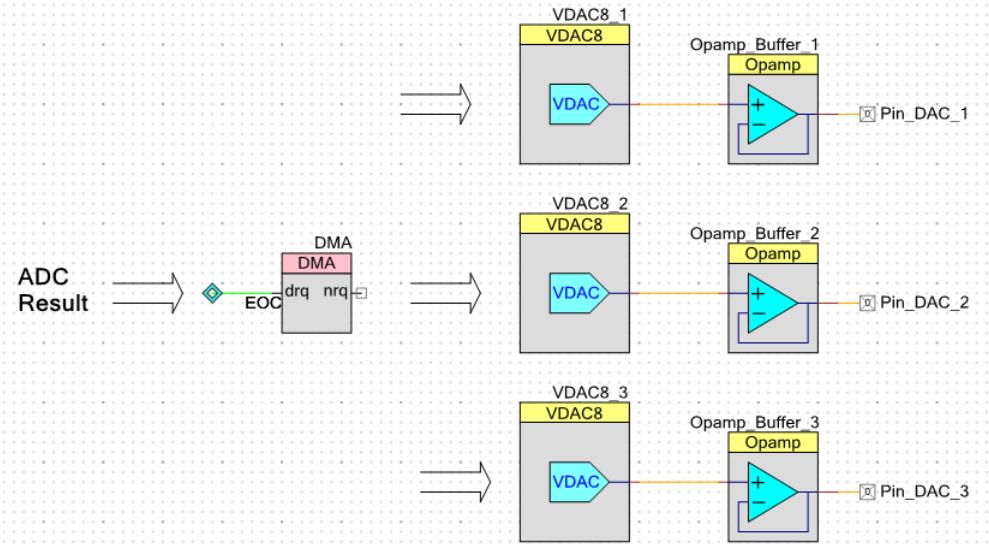
Page 1: ADC_Muliplexing



Page 2: Switching Logic



Page 3: DMA and DAC

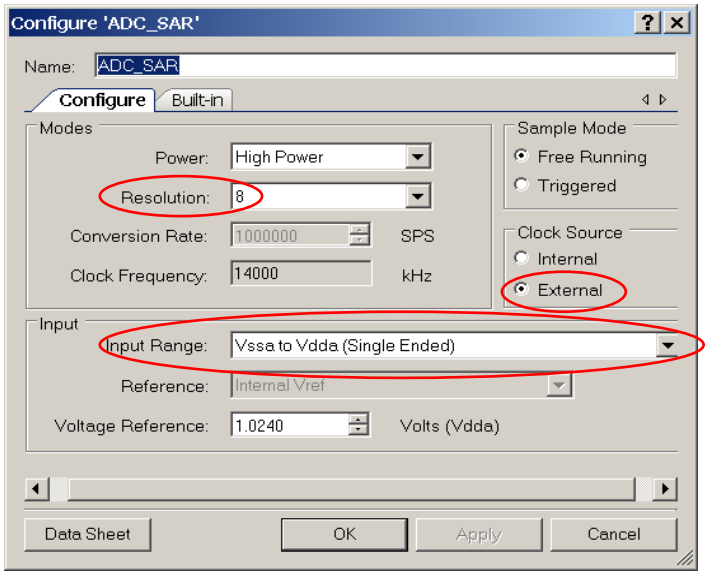


The following figure shows the pin placement as it appears in the *.cydwr* file.

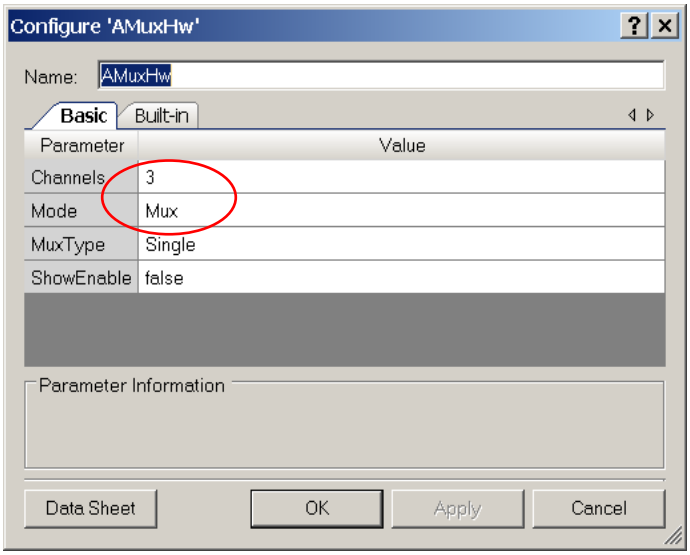
Alias	Name	Pin	Lock
	Pin_MuxOut	P0[7]	☑
	Pin_EOC	P3[2]	☑
	Pin_SwitchingClock	P3[0]	☑
	Pin_SAR_Clock	P3[1]	☑
	Pin_Channel_1	P0[3]	☑
	Pin_Channel_3	P0[5]	☑
	Pin_Channel_2	P0[4]	☑
	Pin_DAC_2	P0[1]	☑
	Pin_DAC_1	P0[0]	☑
	Pin_DAC_3	P3[6]	☑

Component Configuration

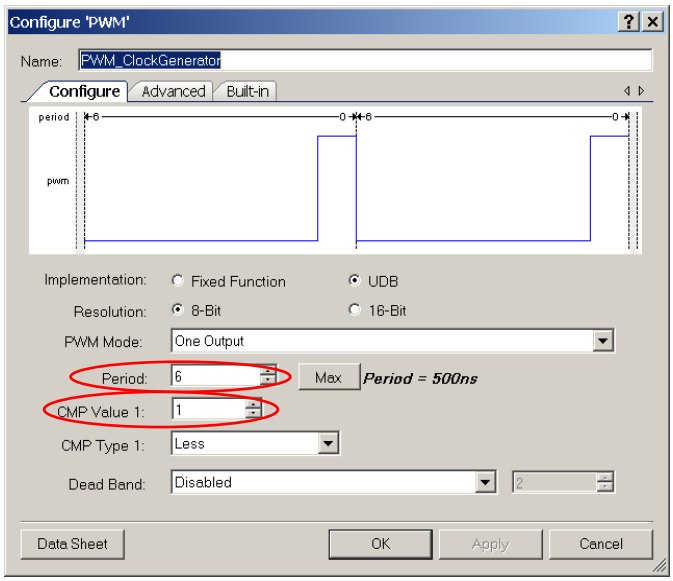
ADC_SAR



AMuxHw

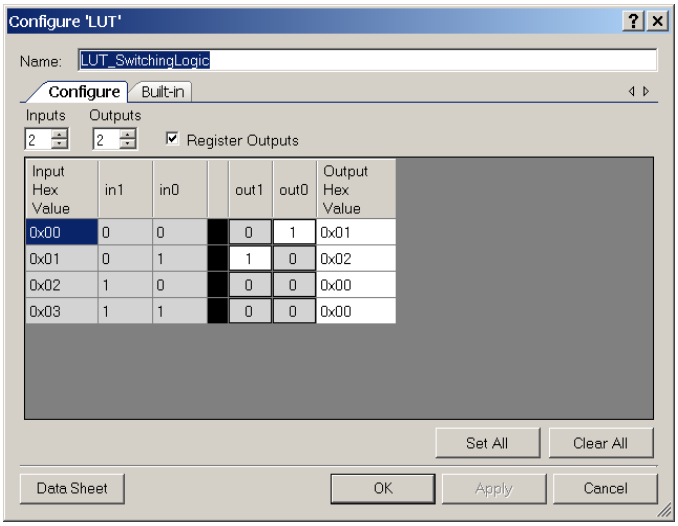


PWM_ClockGenerator



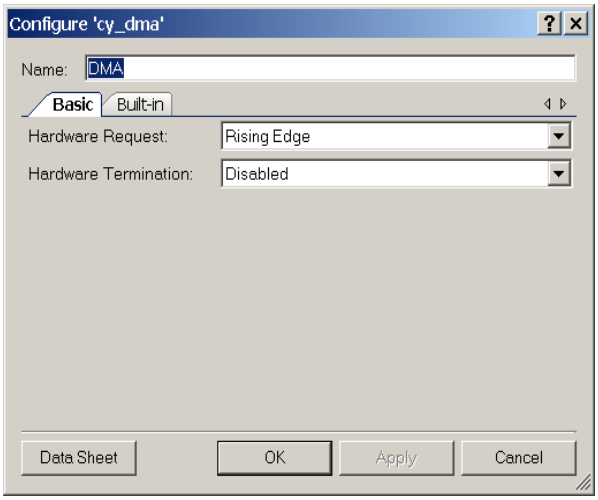
The PWM is configured to generate a pulse one clock cycle wide. This pulse occurs five clock cycles after it is triggered by the ADC EOC.

LUT_SwitchingLogic



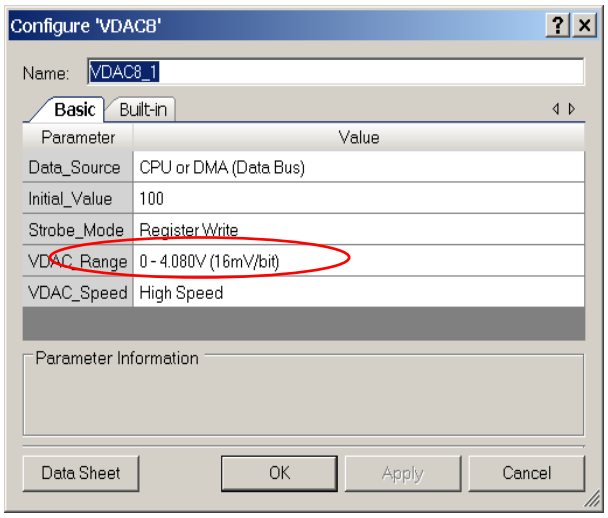
LUT outputs out1 and out0 are connected to select lines of AMuxHw. There are three valid states in the LUT; each state provides output to select a unique channel. The transition to the next state occurs on every rising edge of the clock input.

DMA



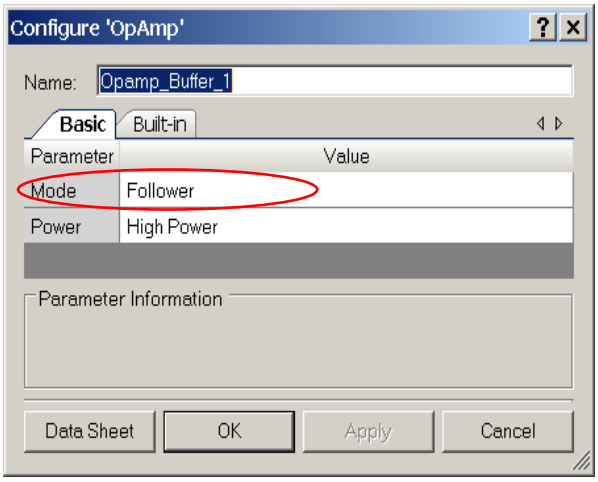
DMA is configured in the function DMA_Initialize() in *main.c* file using DMA APIs.

VDAC8_1



The same configuration is done for the VDAC8_2 and VDAC8_3.

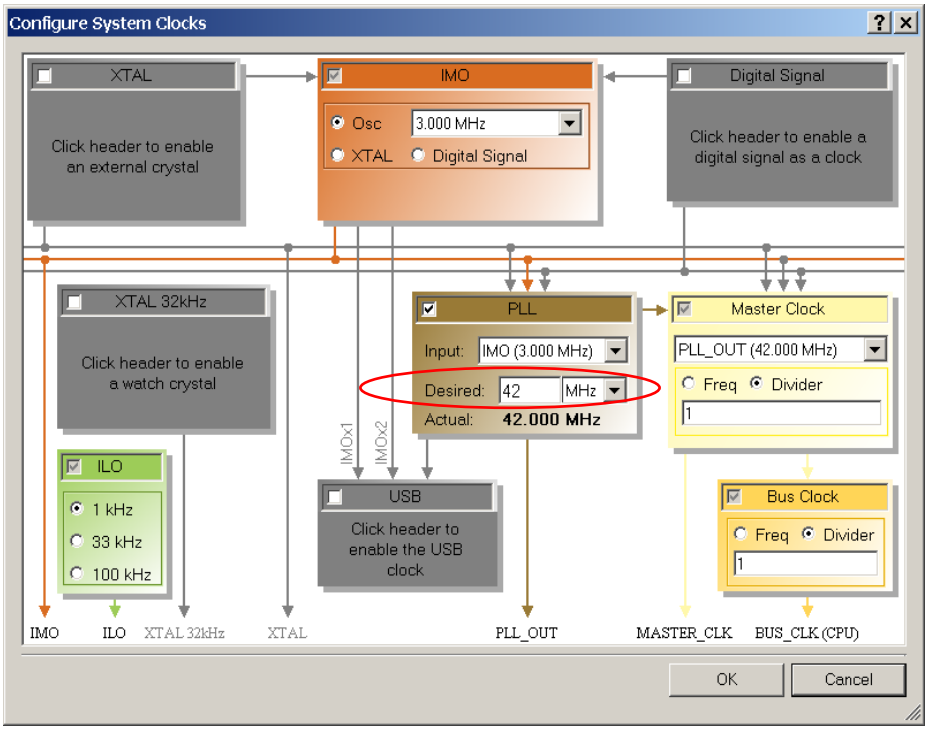
Opamp_Buffer_1



The same configuration is done for the Opamp_Buffer_2 and Opamp_Buffer_3.

Design Wide Resources

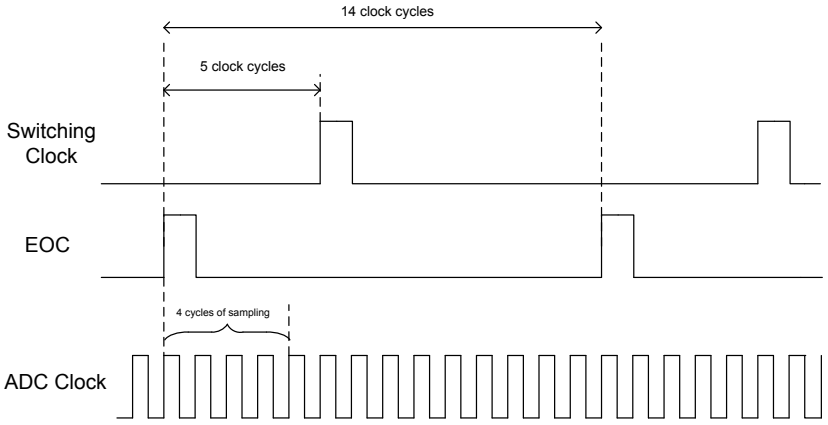
Configure the clocks as shown in the following figure. The Master clock is set to 42 MHz so that with integer divider the SAR ADC gets 14 MHz clock. Open the Clocks tab in the cydwr and click on the BUS_CLK to get the system clocks configuration window as shown in the following figure.



Remaining settings in the design wide resources are left as default.

Operation

The SAR ADC is configured for 8-bit resolution and in continuous mode operation. A 14-MHz clock is given to clock input of the SAR ADC. It takes 14 clock cycles for each conversion resulting in conversion rate of one Msps. It samples the input for four clock cycles. The number of cycles for sampling is configurable in register ADC_SAR_SAR_CSR2_REG. The default number of cycles for sampling is four. After sampling, it converts the signal from analog to digital for next 10 clock cycles. During these ten clock cycles, the input is not being used by the ADC and channel is switched during this time. Following is the timing diagram.



ADC generates the EOC signal after every end of conversion and it starts sampling the input for next conversion. The channel is switched five clock cycles after EOC. A switching clock is generated using PWM, it is a pulse with width of one ADC clock cycle. It occurs six cycles after the EOC as shown earlier. This clock is given as a trigger to channel switching logic that changes the select lines of the mux to select the next channel.

The channel switching logic is built with LUT. The outputs of the LUT are connected to select lines. The LUT states are written such that the channel 1, channel 2 and channel 3 are selected one after the other in round robin manner. Whenever there is a rising edge on the LUT clock, it changes the select lines to select the next channel. The AMuxHw senses the select lines on every rising edge of its clock. A BUS_CLK (42 MHz) is connected to AMuxHw for synchronization and implementing 'Break before Make' feature. It detects any change on the select lines on rising edge of the clock, if there is a change, it disconnects all the channels (Break). On the next rising edge of the clock, it connects the new channel selected by the select lines (Make). Therefore, there can be maximum delay of two clock cycles of 42 MHz after the select lines select the new channel and the channel is actually switched.

DMA is configured to transfer the ADC results to VDAC. Three Transaction Descriptor (TDs) are used to transfer three channel results to three VDACs. The ADC range is set to Vssa to Vdda but the VDAC has range Vssa to 4.08 V. Therefore, though the ADC and DAC both have 8-bit resolution, the VDAC output will be scaled voltage of the actual ADC input. The waveforms are shown in the Output section.

Hardware Connections

The project is tested with PSoC Development Kit CY8CKIT-001 (DVK). The kit is used with jumpers in the default state. Refer to the PSoC Development Kit Board Guide, provided with the kit.

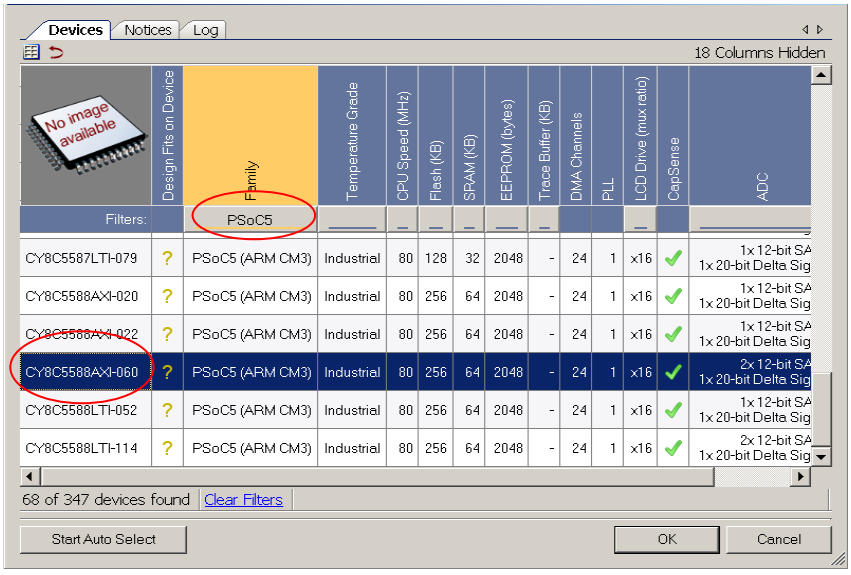
- Two-channel function generator is used, two channels are set to give different waveforms like sine, square or triangular. The voltage range of the signals should be within the Vssa and Vdda, otherwise it may damage the device. The first channel is connected to P0[3] with respect to ground. The second channel is connected to P0[4]. These signals are channel 1 and channel 2 of mux.
- The potentiometer on the DVK is powered by placing the jumper on the J11.
- The VR (potentiometer output) is connected to P0[5] on P14 of DVK. This is third channel of the mux.
- Connect Pin P0[0], P0[1] and P3[6] to oscilloscope to observe the outputs. Use two-channel function generator and set both channels to give triangular wave of frequency 100 Hz, 1 V p-p and with phase difference $0^{0.}$ Set the offsets of both the channels to a voltage equal to Vdda/2.

Output

- Build the project and program the PSoC 5 device.

  Note The default device selection is PSoC 3 (CY8C3866AXI-040), for using this project with PSoC 5 device follow the given steps.

- Go to **Project** → **Device Selector** → Select **PSoC 5** device (CY8C5588AXI-060), build the project again and program the PSoC 5 device as shown in the following figure.



- The pin P0[0], P0[1] and P3[6] are observed on the oscilloscope. Vary the frequency, amplitude and shape of the waveform and observe the same on the output. Note that the input signal range should be within the Vssa to Vddd.

  Below are the example waveforms.

  - **Inputs:**

    Channel 1 of mux (P0[3]): Sine waveform from function generator channel 1.

    Freq= 10 kHz, 2 Vp-p, Offset = Vdda/2 (Vdda=5 V)

    Channel 2 of mux (P0[4]): Triangular waveform from function generator channel 2.

    Freq= 10 kHz, 2 Vp-p, Offset = Vdda/2 (Vdda= 5V)

    Channel 3 of mux (P0[5]): DC voltage from potentiometer on the DVK.

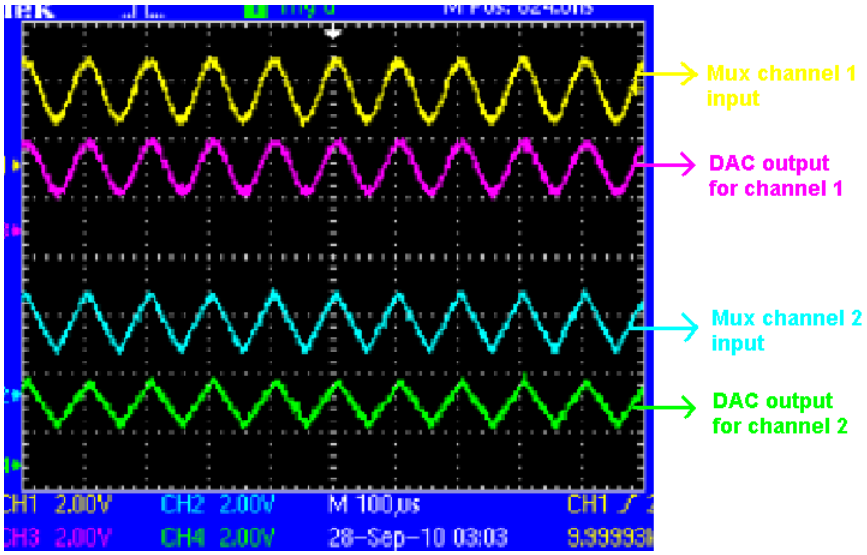
  - **DAC Outputs:**

    Channel 1:Pin P0[0]

    Channel 2:Pin P0[1]

    Channel 3:Pin P3[6]

    Note Only four signals are shown on oscilloscope, two inputs from function generator and two DAC outputs. The DAC output will be scaled down version of the input because ADC range is 0 to Vdda and the DAC range is 0 to 4.08 V. Vdda is set at 5 V.



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