Assuring The Data Integrity of Serial EEPROMs - AN5078

Introduction

As the various power rails within a system rise or fall, the serial EEPROM used with the EZ-USB® family of devices may be susceptible to data corruption at lower power levels under which the LP line of part can continue to operate. Operating in this unstable state may result in the EEPROM interpreting I^2C communication as a write command, causing data to be unintentionally overwritten.

The purpose of this application note is to present recommended design guidelines for assuring the data integrity of serial EEPROM devices when used in EZ-USB designs[1].

Overview

The LP devices have a low-power core that allows them to comply with the bus-powered requirements of the USB 2.0 specification. Because the low-power core may continue to operate under conditions in which EEPROM devices may be unstable, care needs to be taken to ensure that corruption of the data does not occur during power-up or -down. There are several methods for protecting against this type of spurious activity, but the four main design recommendations discussed in this document are:

- Controlling Power Supply Ramp-down
- Using GPIO Pins to Drive Control Signals
- Employing A Voltage Monitoring Device
- Permanent Write-Protection of EEPROMs

While this application note will only focus on protecting serial EEPROM devices used with the LP parts, the same principles can be applied to other peripheral devices that may also be susceptible to the same conditions.

Controlling Power Supply Ramp-down

Using large capacitors in power supply designs is often necessary to ensure stable operation. However, a side-effect of having such large capacitance is that the power rails often ramp down slowly after the supply has been turned off, especially if the power-off load is not large. The addition of motors or other moving parts in a design, such as a hard drive's main spindle motor, can also contribute to the overall speed of the power rail's ramp-down as they continue to spin after power is removed.

While solutions to this issue can involve complex circuitry that minimizes power loss during normal operation, the simplest method of quickly bringing down the power rail is to add a bleed-down resistor between V_{CC} and GND. The resistor should be large enough that it does not cause unnecessary power consumption, while still discharging the bulk capacitors as quickly as possible. Specific resistor values will depend on the overall design of the system, but in general the voltage drop-off time should not exceed 20 ms.

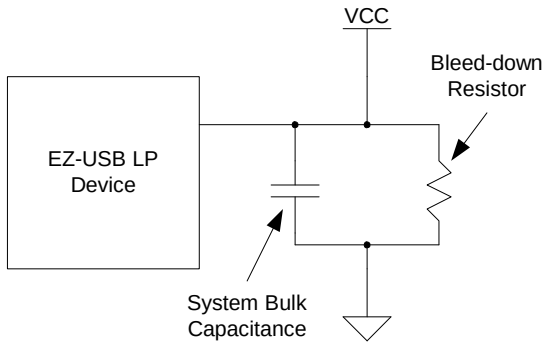

Figure 1. Bleed-down Resistor Used to Ensure that VCC Drops Off Quickly when Power is Removed

Special care should be taken with USB-powered designs to ensure that the power consumption limitations in the USB specification are not violated. By designing a power supply that drops off sharply and does not ring, the majority of EEPROM corruption issues can be avoided.

Using GPIO Pins to Drive Control Signals

Many EEPROMs have a write-protect (WP) or chip-enable signal that will prevent data from actually being written, despite what commands are sent to them. The recommended serial EEPROM that is used in most LP designs can be protected from unintended writes by tying the WP pin to a GPIO pin, or other signal that is not normally set LOW, and having that signal remain HIGH unless a valid I^2C write operation is being performed.

The ATA reset pin in a mass storage design is a good example of the type of signal that can be used to protect EEPROM contents from being corrupted, since it is typically pulled HIGH during normal operation. By tying it to the WP pin on the EEPROM and using firmware or software that asserts it LOW during an I^2C write, access to the data can still be made available while protecting the contents from unintentional writes during unstable power conditions.

Note

1. This document only addresses EEPROMs used with the LP devices. Methods for protecting any other peripheral devices are beyond the scope of this document.

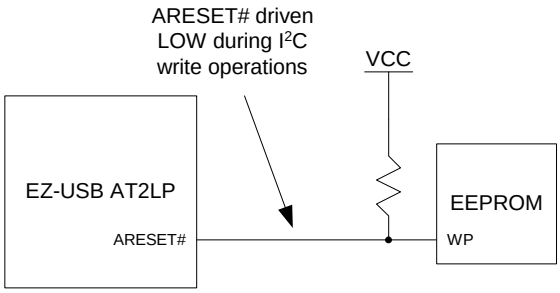

Figure 2. The WP Pin on the Serial EEPROM Being Controlled by the ARESET# Signal from AT2LP

Cypress has already developed a version of the AT2LP Blaster and Primer software that will assert ARESET# during an I^2C write. It is available on a per-request basis and can be obtained by contacting Cypress Support. FX2LP firmware, like vend_ax, has also been modified to behave in a similar manner during regular I^2C writes, and should not require special software builds. The source for vend_ax is available in the FX2LP development kit files, and an example of the modified code is available upon request.

Employing a Voltage Monitoring Device

Perhaps the safest method for ensuring EEPROM data integrity is to ensure that there is no I^2C activity at all during brownout conditions. The best way to do that is to employ a voltage monitoring device that will hold the LP part in reset whenever power levels drop. Past reference designs for Cypress's EZ-USB parts have used a simple R/C circuit to hold the chip in reset at power-up until the power supply has had enough time to stabilize. Such an R/C circuit is appropriate enough for that task, but it does nothing to protect against brownout conditions when the various power rails in a design are not stable.

If a voltage monitor is used, Cypress recommends that it be applied to the highest voltage rail in the design to ensure that the LP part is reset before any other device in the system reaches an unstable state. If this is not possible, then the monitor should be applied so that it does not allow the LP part to operate when the 3.3V power supply is below the minimum value specified in its data sheet.

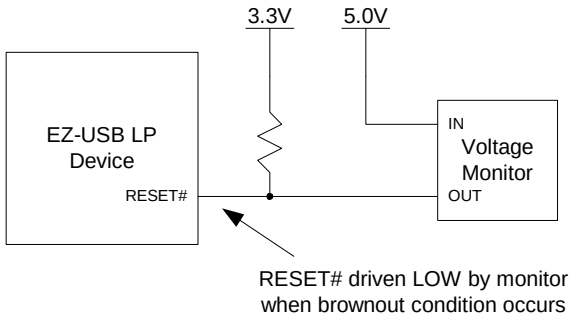

Figure 3. Voltage Monitoring IC Used to Control the LP Device's RESET# Signal

For USB-powered designs, it should be noted that the USB specification allows VBUS to drop as low as 4.7V before it is considered to be at an invalid level. Care should be taken to ensure that a voltage monitor used in a bus-powered design does not needlessly reset the LP device.

Voltage monitoring ICs that can be used to reset the EZ-USB during unstable power conditions are widely available, sporting various package sizes and types to fit design requirements.

Permanent Write-Protection of EEPROMs

An alternative to the previously mentioned recommendations is to permanently tie the WP pin of the EEPROM to its protected state, ensuring that no writes are ever made to the internal memory. This method is typically not the ideal way to protect the data, since most designs take advantage of the LP device's ability to program the EEPROM over USB. However, for manufacturers who rely on factory-programmed EEPROMs, external programmers, or in-circuit programming through means other than USB, this option is certainly valid.

Conclusion

A few simple precautions can ensure that your design is protected against EEPROM corruption during unstable power conditions. The recommendations mentioned in this document are just a few of the many possible methods that could be used to ensure that your design remains reliable under any condition. Proper testing of prototype devices is an essential step in the development of any quality device and will reveal any design weaknesses before mass production begins.

As with all previous USB products from Cypress, the LP line of EZ-USB devices is made available with world-class development tools and software support. Visit www.cypress.com for more details, application notes, and data sheet information.

Additional Resources

Cypress Semiconductor

Please visit Cypress's website at *http//:www.cypress.com* for more information, including:

- EZ-USB LP Data Sheets
- Additional Application Notes
- Cypress Support Contact Information

USB Specification version 2.0

(http://www.usb.org/developers/docs/)

Cypress Semiconductor
198 Champion Court
San Jose, CA 95134-1709
Phone: 408-943-2600
Fax: 408-943-4730
http://www.cypress.com