EZ-PD PMG1 Hardware Design Guidelines and Checklist

Associated part family

- CYPM1011
- CYPM1111
- CYPM1211

About this document

Scope and purpose

This application note provides the hardware design and PCB layout guidelines for EZ-PD™ Power Delivery Microcontroller Gen1 (PMG1) family of high-voltage USB-C power delivery (PD) microcontrollers. This application note provides detailed hardware design aspects of PMG1 MCU-based system design. The document uses PMG1 family prototyping kit as the design reference. This application note includes a schematics and layout review checklist, which consolidates the important points to be considered while designing with PMG1.

Intended audience

This application note is intended to familiarize engineers with the hardware design guidelines for PMG1 MCU-based designs.

Table of contents

1 Introduction

EZ-PD PMG1 is a family of high-voltage USB PD MCUs with Arm® Cortex®-M0/Cortex-M0+ CPU. The PMG1 family of controllers includes different MCUs with integrated USB PD controller, analog, and digital peripherals. You can choose the controller based on the design requirement. PMG1 is targeted at embedded systems that provide or consume power to or from a high-voltage USB-C PD port and leverage the MCU to provide additional control capability.

2 Device selection

This section describes the basic features of the PMG1 family. **Table 1** compares the basic features of various MCUs in the PMG1 family.

Table 1 Comparison of features of different MCUs of PMG1 family

Sub-system or Range	Item	PMG1-S0	PMG1-S1	PMG1-S2
CPU and Memory Sub-system	Core	Arm Cortex-M0	Arm Cortex-M0	Arm Cortex-M0
	Max Freq (MHz)	48	48	48
	Flash (KB)	64	128	128
	SRAM (KB)	8	12	8
Power Delivery	Power Delivery Ports	1	1	1
	Role	Sink	DRP	DRP
	MOSFET Gate Drivers	1x PFET	2x PFET	2x PFET/NFET
	Fault Protections	VBUS OVP[1] and UVP[2]	VBUS OVP, UVP, and OCP[3]	VBUS OVP, UVP and OCP
USB	Integrated Full Speed USB 2.0 Device with Billboard Class support	No	No	Yes
Voltage Range	Supply (V)	VDDD (2.7 - 5.5) VBUS (4 - 21.5)	VSYS (2.75 - 5.5) VBUS (4 - 21.5)	VSYS (2.7 - 5.5) VBUS (4 - 21.5)
	IO (V)	1.71 - 5.5	1.71 - 5.5	1.71 - 5.5
Digital	Serial Communication Block (configurable as I2C/UART/SPI)	2	4	4
	TCPWM Block	4	2	4
	Hardware Authentication Block (Crypto)	No	No	Yes
Analog	ADC	2x 8-bit SAR	1x 8-bit SAR	2x 8-bit SAR
	On-chip Temperature Sensor	Yes	Yes	Yes
GPIO	Max # of I/O	12(10+2 OVT[4])	17(15+2 OVT)	20(18+2 OVT)
Charging Standards	Charging Source	-	BC 1.2, AC	BC 1.2, AC
	Charging Sink	BC 1.2, Apple Charging (AC)	BC 1.2, AC	BC 1.2, AC

[1] OVP stands for Over Voltage Protection

[2] UVP stands for Under Voltage Protection

[3] OCP stands for Over Current Protection

[4] OVT stands for Over-Voltage Tolerant

Sub-system or Range	Item	PMG1-S0	PMG1-S1	PMG1-S2
ESD Protection	See **ESD and EMI/EMC protection** for details on in-built ESD thresholds			
Packages	Package Options	24 QFN (4x4mm, 0.5mm pitch)	40 QFN (6×6mm, 0.5mm pitch)	40 QFN (6×6mm, 0.5mm pitch)

2.1 Ordering information

Table 2 Ordering information

MCU	MPN	Type-C port	Termination resistor	Package type	Si ID
PMG1-S0	CYPM1011-24LQXI CYPM1011-24LQXIT	1	R_D, R_{D-DB}	24-Pin QFN	0x2020
PMG1-S1	CYPM1111-40LQXI CYPM1111-40LQXIT	1	R_P, R_D, R_{D-DB}	40-Pin QFN	0x2A20
PMG1-S2	CYPM1211-40LQXI CYPM1211-40LQXIT	1	R_P, R_D, R_{D-DB}	40-Pin QFN	0x1D20

3 System architecture

3.1 USB PD Sink only applications

The USB PD sink systems or applications are powered directly through the USB PD port on the design and requires no separate power input. In the USB PD Sink role, the PMG1 MCUs are capable of handling a PD contract of up to 20 V, 5 A (10 0W).

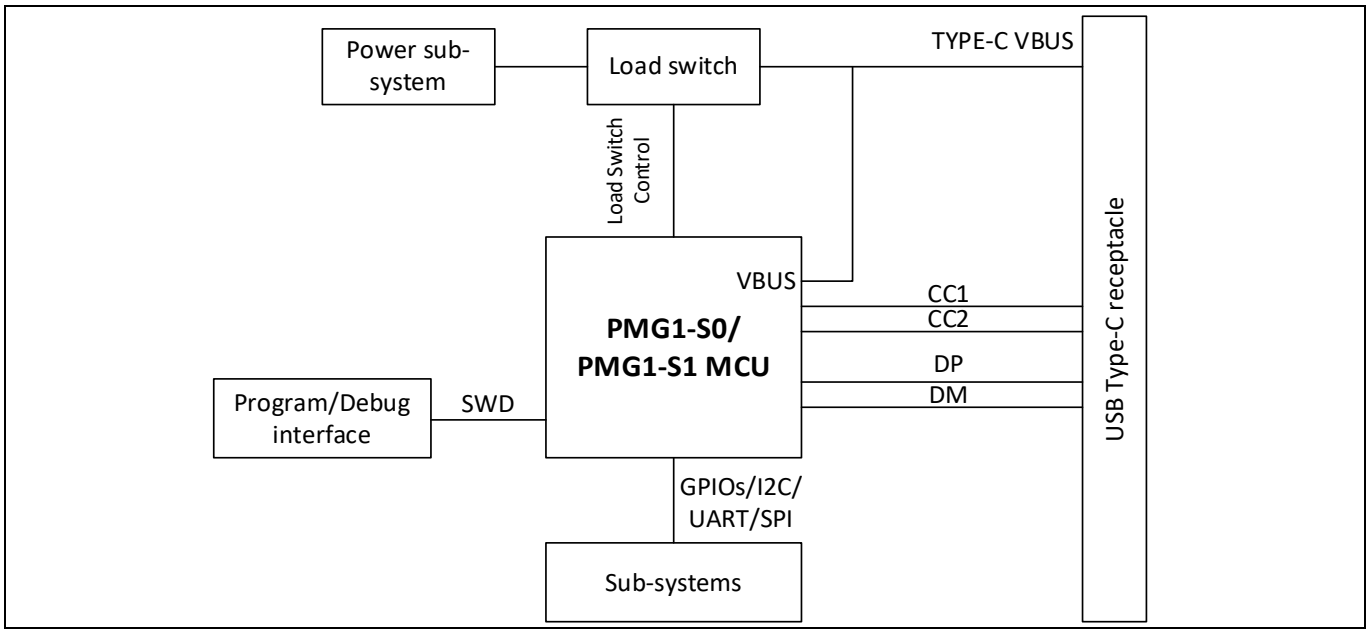

Figure 1 USB PD Sink only application using PMG1-S0/PMG1-S1

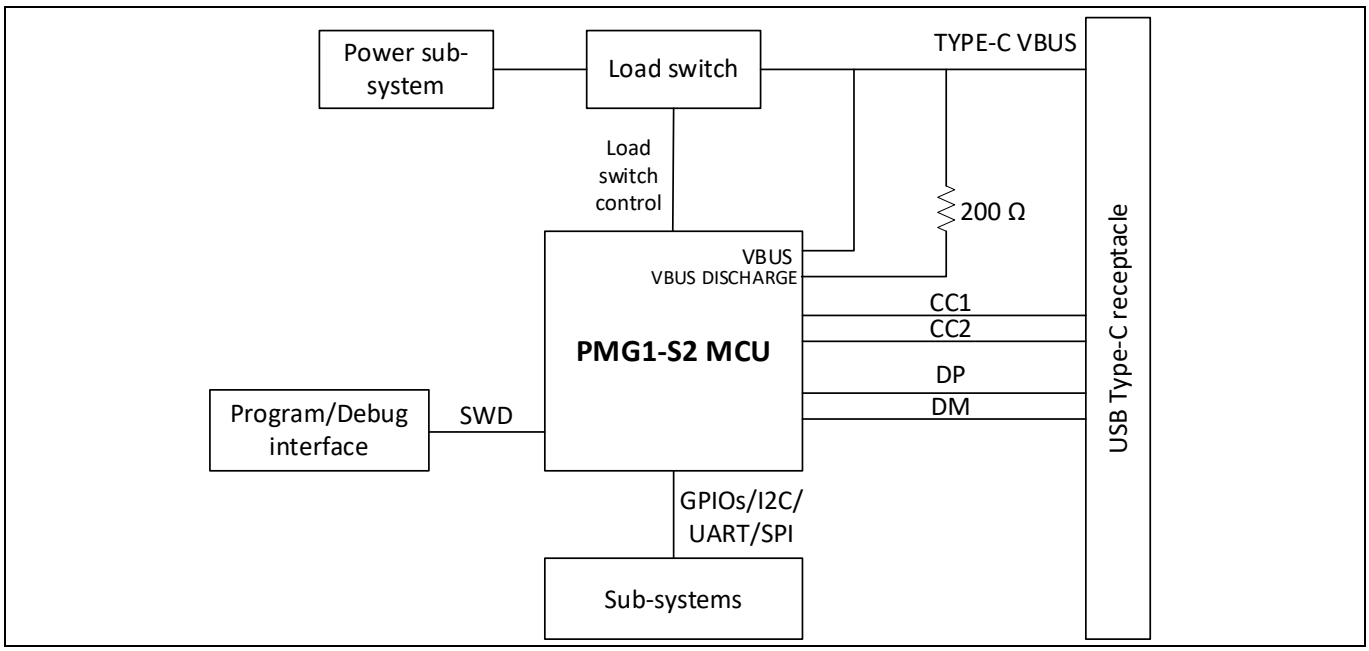

Figure 2 USB PD Sink only application using PMG1-S2

4 Schematic design requirements

This section explains the schematic design requirements and considerations for a PMG1 MCU-based system. CY711X PMG1-SX Prototyping Kits are used as the reference for design. See the following kit pages for details:

- **CY7110 EZ-PD PMG1-S0 Prototyping Kit**
- **CY7111 EZ-PD PMG1-S1 Prototyping Kit**
- **CY7112 EZ-PD PMG1-S2 Prototyping Kit**

4.1 Power system

The PMG1 MCUs support powering of chip directly from the Type-C PD port through the VBUS pin on the MCU. The USB PD sink, dead battery, and other bus powered applications use the VBUS pin as the power input for the MCU. When powered through VBUS, the internal regulator generates VDDD of 3.3 V for chip operation and further regulated VCCD (1.8 V) for core operation. PMG1 MCUs, except PMG1-S0, have a dedicated power input pin for any USB PD DRP/Source only application and all general MCU applications.

In PMG1-S0, VDDD voltage can be supplied directly to power the MCU. PMG1-S1 and PMG1-S2 MCUs have dedicated power input pin VSYS, and does not support VDDD as the power input pin. VSYS power pin is connected to VDDD internally through a switch. The core regulator regulates VDDD voltage to 1.8 V for core operation and the output of the 1.8-V regulator denoted as VCCD.

A separate power domain, VDDIO, is provided for the powering GPIOs in PMG1-S1 and PMG1-S2 MCUs. The VDDD and VDDIO pins can be shorted, if required. These devices support VCONN functionality and additional input supply option is available in the silicon for powering VCONN FETs.

Table 3 summarizes the power inputs in the PMG1 MCUs.

Table 3 PMG1 MCU power pins and operating voltages

MCU	Power pin	Power pin description	Valid input voltage level
PMG1-S0	VBUS	Bus Power	4.0 V – 21.5 V
	VDDD	MCU Power Input, internal LDO output	2.7 V – 5.5 V
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	
PMG1-S1	VBUS	Bus Power	4.0 V - 21.5 V
	VSYS	Device Power input	2.75 V – 5.5 V
	VDDIO	Supply for I/Os	1.8 V – VDDD
	VCONN_ Source	Supply to VCONN FETs	
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	
PMG1-S2	VBUS	Bus Power	4.0 V - 21.5 V
	VSYS	Device Power input	2.75 V – 5.5 V
	VDDIO	Supply for I/Os	1.8 V – VDDD
	VCONN_ Source	Supply to VCONN FETs	

MCU	Power pin	Power pin description	Valid input voltage level
	VCCD	The core voltage of the device is brought out to the pin. This pin cannot be used as a voltage source and is intended to connect only a decoupling capacitor.	

Following are the power system design considerations for USB PD Sink application using PMG1 MCUs:

- The VBUS pin of the MCU should be the power input pin. The power pin of the Type-C connector should connect to the VBUS pin as shown in **Figure 3** and **Figure 4**.
- Do not connect the other input pin (VDDD in PMG1-S0 and VSYS in PMG1-S1/S2) to any power rail. Connect decoupling capacitors to those pins (see **Table 3** for the decoupling capacitor value).
- Short VDDD and VDDIO pins in PMG1-S1 and PMG1-S2.
- Do not connect any signal or power rail to VCCD, and add only decoupling capacitor.

4.1.1 Decoupling and bypass capacitors

Add decoupling and bypass capacitors to all power input pins and internal regulator output pins to filter out AC noise/voltage spikes and decouple the device power domains. **Table 4** lists the recommended values of decoupling and bypass capacitors for each power domain signal in the PMG1 family MCUs.

For VDDD, VBUS, and VSYS, it is recommended to use multiple capacitor decoupling circuit to improve filtering and reduce the effect of ESR of the capacitor. Along with recommended values, you can place one or two low-ESR 100nF capacitors as the decoupling capacitor.

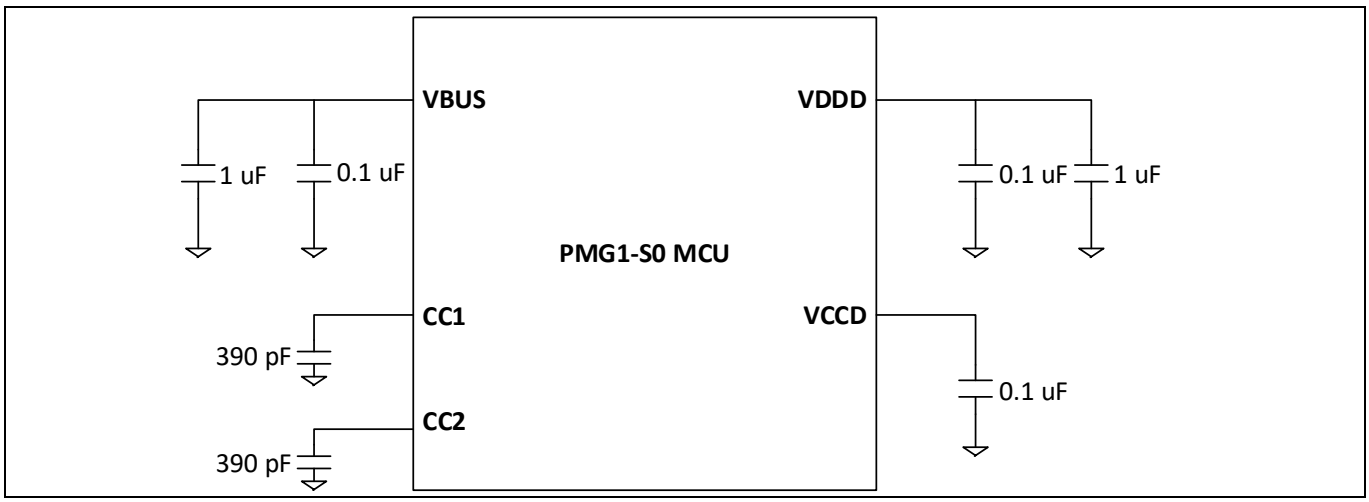

Figure 3 PMG1-S0 decoupling capacitor

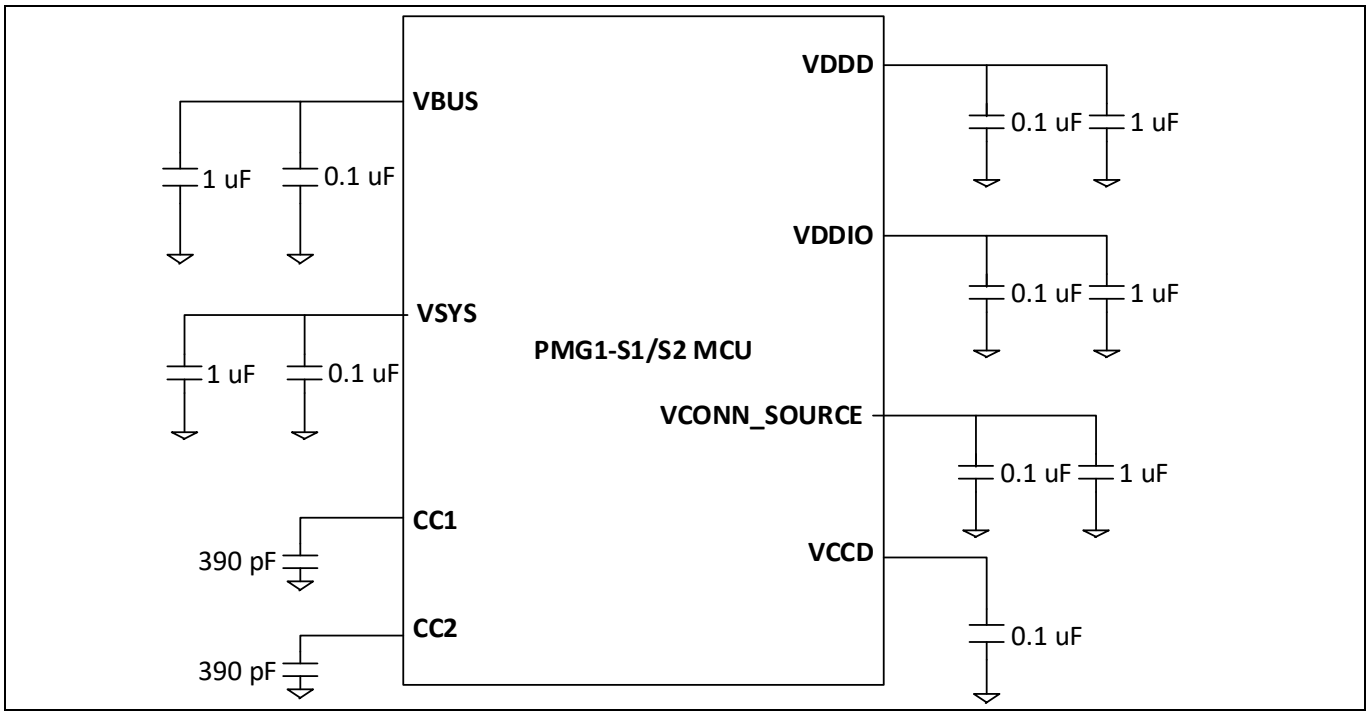

Figure 4 PMG1-S1, PMG-S2 MCUs decoupling capacitors

Table 4 Power supply pins and decoupling capacitors

MCU	Power Supply Pin	Decoupling capacitor
PMG1-S0	VBUS	1 µF
	VDDD	1 µF
	VCCD	1 µF
PMG1-S1	VBUS	1 µF
	VSYS	1 µF
	VDDIO	0.1 µF
	VCONN_ Source	1 µF
	VCCD	1 µF
PMG1-S2	VBUS	1 µF
	VSYS	1 µF
	VDDIO	0.1 µF
	VCONN_ Source	1 µF
	VCCD	1 µF

4.2 External voltage regulators

External voltage regulators are required in the application when an external module has higher current requirement than the PMG1 MCU GPIOs can supply. The GPIOs can source or sink a maximum current of 25 mA (per GPIO).

Linear Dropout (LDO) regulators are required in the PMG1 MCU designs to power various sub-systems, such as LEDs, sensor modules, extension, adapter board, and so on, in the solution or design. Select the LDO by considering the required output voltage, maximum load current, and power ratings.

Table 5 lists the recommended LDOs.

Table 5 Recommended LDO regulators

MPN	Manufacturer	Input Voltage Max	Output Voltage	Output Current	Application
IFX25001	Infineon	45 V	2.5 V, 3.3 V, 5.0 V, 8.5 V, or 10.0 V	400 mA	Standard
TLE42744	Infineon	40 V	5 V and 3.3 V ±2%	400 mA	Automotive
IFX27001	Infineon	40 V	1.5 V, 1.8 V, 2.6 V, 3.3 V, 5.0 V, or Adjustable output voltage	1 A	Standard

4.3 Reset circuit and clock

The PMG1 MCUs, except PMG1-S0, have an external reset control pin, XRES, to manually reset the MCU. The MCUs have active LOW reset, and should be held low for a minimum of 5 us to reset the chip. All PMG1 MCUs support Power-on-Reset (POR) mechanism.

- In PMG1-S1, reset pin should be pulled-up to VDDIO/VDDD using a 4.7k resistor. This will make sure that the XRES pin is not left floating in the design and the device can function properly.

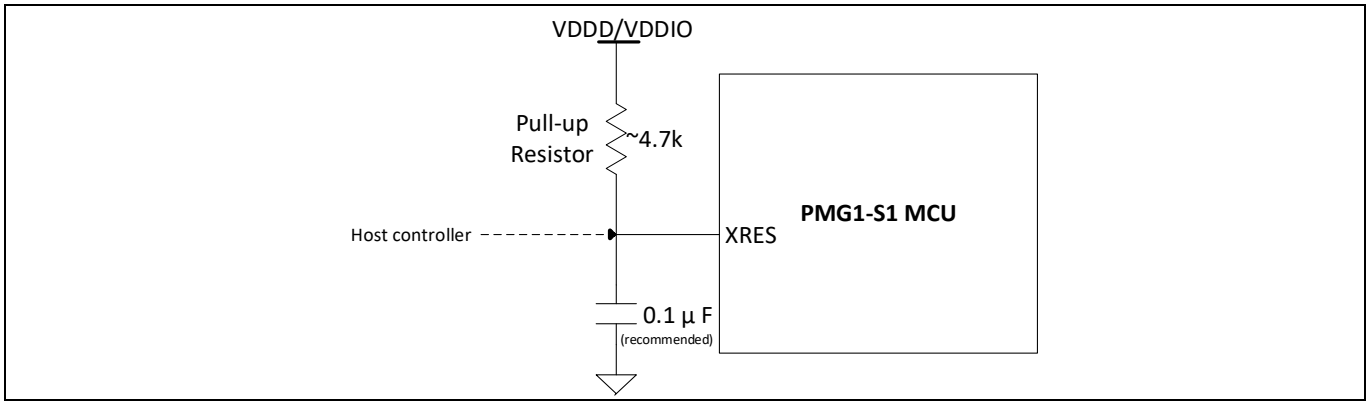

Figure 5 PMG1-S1 XRES pin connection

- PMG1-S2 has an internal pull-up on the XRES pin, and an external pull-up resistor need not be connected.

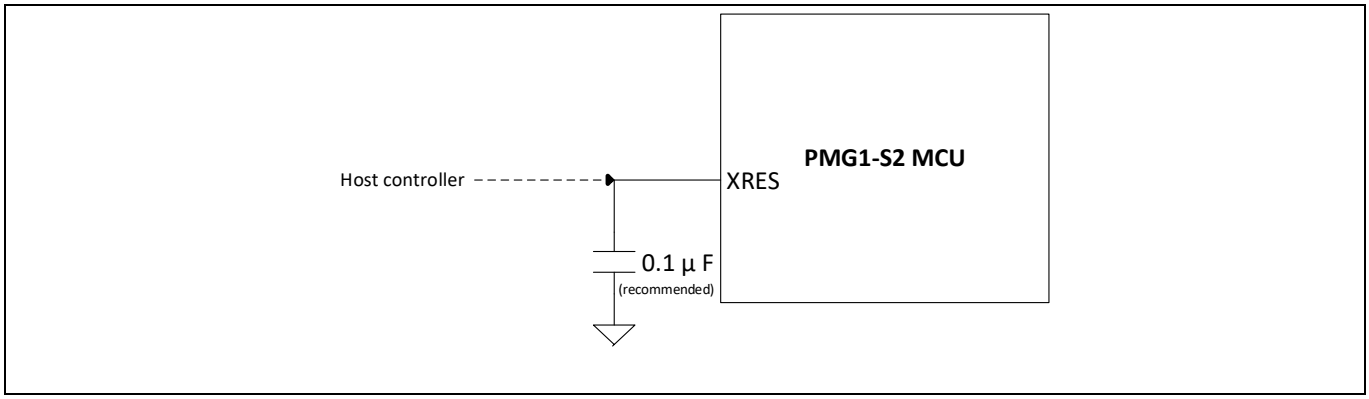

Figure 6 PMG1-S2 XRES pin connection

- It is recommended to connect a capacitor (typically 0.1 µF) to the XRES pin to filter out glitches and to give the reset signal better noise immunity.
- Optionally, if PMG1 is controlled by an external controller, the XRES pin can be directly driven by the host.

PMG1 MCUs have an integrated clock circuitry; external components such as a crystal or oscillator are not required.

4.4 GPIO

PMG1 MCUs provide flexible GPIOs with alterative connection to digital and analog peripherals. Different peripherals have different dedicated or fixed pins for their terminals. The USB PD pins are fixed signals connected to USB PD subsystem.

4.4.1 I/O pin selection

Table 6 lists the MCU pins assigned for digital block, analog block, and USB sub-system.

Table 6 PMG1 MCU pin assignment

Block	Pin Name	Pin #			Remarks
		PMG1-S0	PMG1-S1	PMG1-S2	
System function pins					
Reset	XRES	N/A	10	26	Reset input
USB and USB PD					
USB PD Sub system	CC1	15	9	5	Configuration Channel
	CC2	14	7	3	
	CSN	N/A	40	39	Current Sense
	CSP	N/A	1	40	
	DP	17	N/A	21	USB D+/D- signals
	DM	16	N/A	22	
	DP_SYS	N/A	23	N/A	
	DM_SYS	N/A	24	N/A	
	DP_TOP	N/A	28	N/A	
	DM_TOP	N/A	27	N/A	

Block	Pin Name	Pin #			Remarks
		PMG1-S0	PMG1-S1	PMG1-S2	
	DP_BOT	N/A	26	N/A	
	DM_BOT	N/A	25	N/A	
	FET control pins				Load switch control pins
Digital Pins					
Serial Communication Block (SCB)	SCB Pins	See **Table 9**			PMG1-S0 has two SCBs and PMG1-S1 and PMG1-S2 have four SCBs. The SCBs can be configured as SPI, I2C, or UART
TCPWM	TCPWM pins	See **Table 10**			PMG1-S0 and PMG1-S2 have four TCPWM and PMG1-S1 has two TCPWM. All these signals are routed to dedicated GPIO pins.
Analog Pins					
SAR ADC	ADC	See the datasheet **[4]**			PMG1-S0 and PMG1-S2 have 2x 8-bit ADC and PMG1-S1 has one 8-bit ADC.

4.4.2 Over-voltage tolerant GPIO

All PMG1-MCUs have two over-voltage tolerant (OVT) pins; I2C signal pins (I2C SDA and I2C SCL) from SCB0 are the OVT pins. These GPIOs are capable of handling an absolute maximum voltage of 6 V. The pins are similar to regular GPIOs with additional features such as over-voltage tolerance, and better pull-down drive strength. When SCB0 is configured as an I2C component, it meets the following I2C specifications:

- Fast Mode hot-swap
- Fast Mode Plus IOL Specification
- Fast Mode and Fast Mode Plus Hysteresis and minimum fall time specifications

Table 7 lists the OVT-GPIOs for each MCU in the PMG1 family.

Table 7 OVT-GPIOs

	PMG1-S0	PMG1-S1	PMG1-S2
OVT-GPIO (GPIO [MCU pin#])	P0.0 [7]	P5.0 [16]	P0.0 [27]
	P0.1 [8]	P5.1 [17]	P0.1 [28]

4.5 Programming and debugging interfaces

PMG1 MCU supports Serial Wire Debug (SWD) protocol for programming and debugging. The SWD data and SWD clock signals are available on specific GPIOs of the MCU. **Table 8** lists the SWD pin mapped GPIOs in all devices. PMG1-S1 and PMG1-S2 devices support reset mode for acquiring the device for programming or debugging. In reset mode, the programmer/debugger applies reset signal over the XRES pin on the MCU. The device should be powered externally while using this mode, or the programmer should be able to power the chip.

Table 8 SWD signal pin assignment

	GPIO Port [MCU Pin#]		
	PMG1-S0	PMG1-S1	PMG1-S2
SWD IO (SWD Data)	P0.0 [7]	P1.4 [6]	P2.0 [15]
SWD CLK (SWD Clock)	P0.1 [8]	P1.0 [2]	P2.1 [16]

PMG1-S0 device does not have reset signal, and the device is acquired in power cycle mode. In power cycle mode, the target MCU is acquired by toggling device power, and the device should not be externally powered in this mode.

The SWD signals can be routed to 5-pin or 10-pin standard SWD connector, so that it can be used as programming/debugging connector. **Figure 7** and **Figure 8** show the standard 5-pin and 10-pin SWD connector pin out, respectively. In PMG1-S0, the reset pin of the header should be left unconnected.

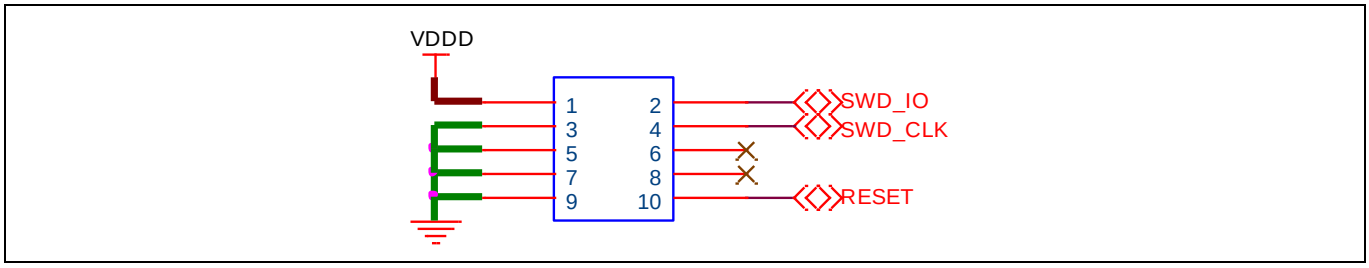

Figure 7 10-pin SWD header

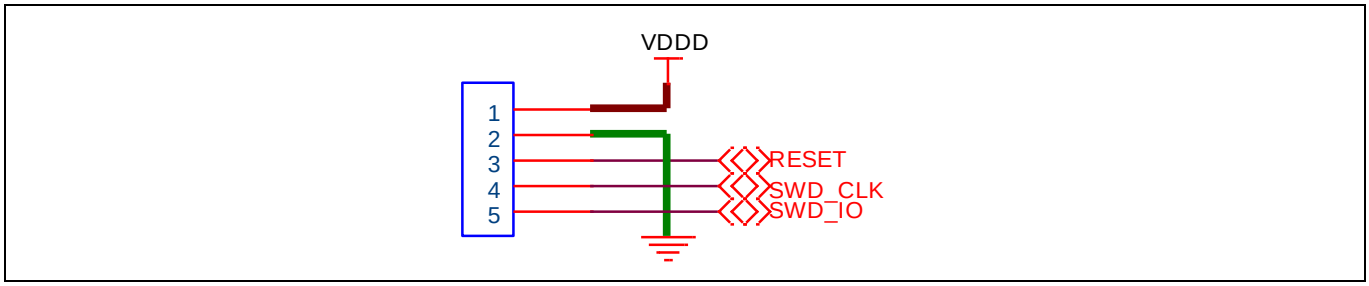

Figure 8 5-pin SWD header

4.6 Digital Blocks

4.6.1 Serial Communication Block (SCB)

SCBs are multifunctional hardware blocks that implement UART, I2C, and SPI communication components. You can use any available SCB and configure it as the desired communication block in ModusToolbox® IDE. The communication signals, in SCB, are routed to specific GPIOs. See **Table 9** for the details of assignment.

4.6.1.1 Serial Peripheral Interface (SPI)

PMG1 MCUs can operate in SPI master and slave modes. The SCB supports single master-multiple slave topology for SPI. SPI master mode can be used when PMG1 has to communicate with one or more SPI slave devices, and slave mode can be used when PMG1 has to communicate with an SPI master. The SCB offers different protocol types, data frame size, and configurable parameters as SPI peripheral.

4.6.1.2 I2C

The PMG1 supports master and slave modes of operation for I2C. The I2C peripheral offers configurability to multiple I2C parameters. The I2C signals does not have any internal pull-ups in the MCU. You have to pull-up the signals to VDDIO/VDDD using 2.2k resistor.

4.6.1.3 UART

UART communication is typically point-to-point communication protocol through TX and RX signals. TX or transmitter output transmits the data, and RX or receiver input receives data from the other module. RX of the PMG1 should be connected to TX of the other module and TX of the PMG1 should connect to RX of the module.

Table 9 lists the GPIO pin assignment for SCBs in PMG1 MCUs.

Table 9 PMG1 SCBs and pin assignment

Component	Signal	Port and pin assignment (Port [MCU pin])			
		SCB0	SCB1	SCB2	SCB3
PMG1-S0					
UART	UART_RX	P2.3 [13] or P2.1 [10]	P1.3 [6] or P3.1 [16]		
	UART_TX	P2.2 [12] or P2.0 [9]	P1.2 [5] or P3.0 [17]		
	UART_CTS	P0.0 [7]	P1.0 [1]		
	UART_RTS	P0.1 [8]	P1.1 [2]		
I2C	I2C_SDA	P0.0 [7]	P1.0 [1] or P2.2 [12]		
	I2C_SCL	P0.1 [8]	P1.1 [2] or P2.3 [13]		
SPI	SPI_MOSI	P1.2 [5]	P0.0 [7]		
	SPI_MISO	P1.1 [2]	P0.1 [8]		
	SPI_SEL	P1.0 [1]	P2.0 [9]		
	SPI_CLK	P1.3 [6]	P2.1 [10]		
PMG1-S1					

Component	Signal	Port and pin assignment (Port [MCU pin])			
		SCB0	SCB1	SCB2	SCB3
UART	UART_RX	P3.0 [18]	P1.0 [2]	P4.1 [30]	P0.1 [39]
	UART_TX	P5.1 [17]	P1.1 [3]	P4.0 [29]	P0.0 [38]
	UART_CTS	P2.2 [15]	P1.2 [4]	P3.1 [20]	P2.0 [13]
	UART_RTS	P5.0 [16]	P1.3 [5]	P3.2 [21]	P2.1 [14]
I2C	I2C_SDA	P5.0 [16]	P1.1 [3]	P3.1 [20]	P2.1 [14]
	I2C_SCL	P5.1 [17]	P1.2 [4]	P3.2 [21]	P2.0 [13]
SPI	SPI_MOSI	P5.0 [16]	P1.1 [3]	P3.2 [21]	P2.1 [14]
	SPI_MISO	P5.1 [17]	P1.2 [4]	P4.0 [29]	P0.0 [38]
	SPI_SEL	P2.2 [15]	P1.0 [2]	P3.1 [20]	P2.0 [13]
	SPI_CLK	P3.0 [18]	P1.3 [5]	P4.1 [30]	P0.1 [39]
PMG1-S2					
UART	UART_RX	P2.6 [25] or P1.2 [9]	P1.7 [14]	P1.1 [8]	P1.5 [13]
	UART_TX	P2.5 [24] or P1.3 [10]	P1.6 [11]	P1.0 [7]	P1.4 [12]
	UART_CTS	P0.0 [27]	P2.0 [15]	P3.4 [36]	P1.2 [9]
	UART_RTS	P0.1 [28]	P2.1 [16]	P3.5 [37]	P1.3 [10]
I2C	I2C_SDA	P0.0 [27]	P2.1 [16]	P3.4 [36]	P1.3 [10]
	I2C_SCL	P0.1 [28]	P2.0 [15]	P3.5 [37]	P1.2 [9]
SPI	SPI_MOSI	P2.5 [24]	P2.1 [16]	P3.4 [36]	P1.2 [9]
	SPI_MISO	P0.1 [28]	P1.6 [11]	P1.0 [7]	P1.4 [12]
	SPI_SEL	P0.0 [27]	P1.7 [14]	P1.1 [8]	P1.5 [13]
	SPI_CLK	P2.6 [25]	P2.0 [15]	P3.5 [37]	P1.3 [10]

4.6.2 Timer, Counter, and Pulse Width Modulator (TCPWM)

TCPWM is a multifunctional component that implements core microcontroller functionality. PMG1-S0 and PMG1-S2 MCUs have four TCPWM blocks and PMG1-S1 has two TCPWM blocks. TCWM block in PMG1 MCU implements the 16-bit timer, counter, pulse width modulator, and quadrature decoder functionality. The block can be used to measure the period and pulse width of an input signal (timer), find the number of times a particular event occurs (counter), generate PWM signals, or decode quadrature signals. **Table 10** lists the line output pin of TCPWM blocks in PMG1 MCUs. See the datasheet **[4]** for more details.

Table 10 List of TCPWM output pins

TCPWM signal	GPIO port [MCU Pin#]			Description
	PMG1-S0	PMG1-S1	PMG1-S2	
TCPWM_line_0	P0.0 [7]	P1.2 [4]	P3.2 [34]	Output of TCPWM-0
	P2.2 [12]		P0.0 [27]	
TCPWM_line_1	P0.1 [8]	P1.4 [6]	P3.3 [35]	Output of TCPWM-1
	P2.3 [13]		P0.1 [28]	

TCPWM signal	GPIO port [MCU Pin#]			Description
	PMG1-S0	PMG1-S1	PMG1-S2	
TCPWM_line_2	P2.0 [9]	N/A	P3.4 [36]	Output of TCPWM-2
	P1.0 [1]			
TCPWM_line_3	P2.1 [10]	N/a	P3.5 [37]	Output of TCPWM-3
	P1.1 [2]			

4.7 USB PD block

This section explains the recommended hardware design considerations for USB- data and USB PD designs.

4.7.1 VBUS discharge

Integrated VBUS discharge circuitry discharges VBUS during detach condition or negative voltage transition. PMG1-S0 and PMG1-S1 MCUs have integrated VBUS discharge circuit. The PMG1-S2 requires external resistor for discharging VBUS. The VBUS_C discharge switch allows discharging of VBUS through the external resistor. In PMG1-S2 based designs, VBUS_DISCHARGE pin of the MCU should be connected to the VBUS pin through an external resistor of 200 Ohm (100 Ohm).

4.7.2 CC and VCONN

PMG1 MCUs support USB PD contract of up to 20 V, 5 A (100 W) in sink, source, and DRP roles. CC1 and CC2 pins on the PMG1 device should be connected CC1 and CC2 pins on the Type-C PD connector. A 390-pF decoupling capacitor should be connected to CC lines (CC1, CC2) to maintain the signal quality at the signaling rate of 300 kHz. The CC pin decoupling capacitor should be placed as close as possible to the MCU pins.

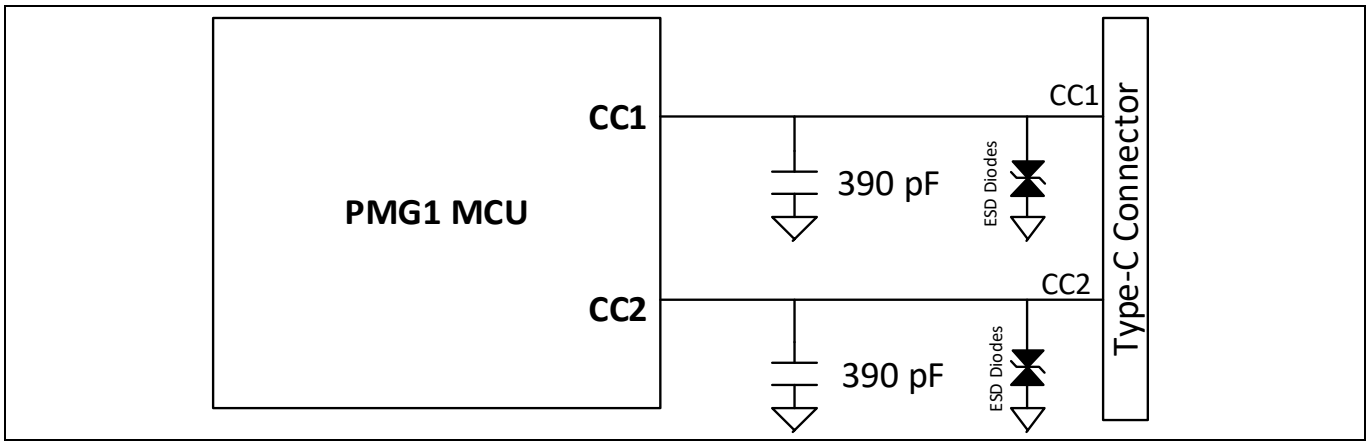

Figure 9 CC1, CC2 signals

If the application supports VCONN functionality in the USB PD port, VCONN_Source should be connected to the voltage source to power internal VCONN FETs. The power source should be capable of handling VCONN power requirement and decoupling capacitors should be placed on the MCU VCONN_Source pin as mentioned in Decoupling and bypass capacitors. VCONN FETs have an associated over current protection (OCP) circuit to protect the chip from VCONN OCP fault. PMG1-S0 MCU does not support VCONN functionality.

4.7.3 Gate driver or load switch control signals

The PMG1 MCUs have an integrated N-Channel FET, P-Channel FET (PFET), or both Gate drivers to drive FET-based load switches on the provider and consumer path.

PMG1-S0 has two P-channel FET gate drivers to drive two external PFETs on the VBUS consumer path. VBUS_FET_CTRL_0 gate driver has an active pull-up, and thus can drive HIGH, LOW, or High-Z. But VBUS_FET_CTRL_1 gate driver can drive only LOW or High-Z thus requires external pull-up. The gate driver signals are VBUS voltage-tolerant.

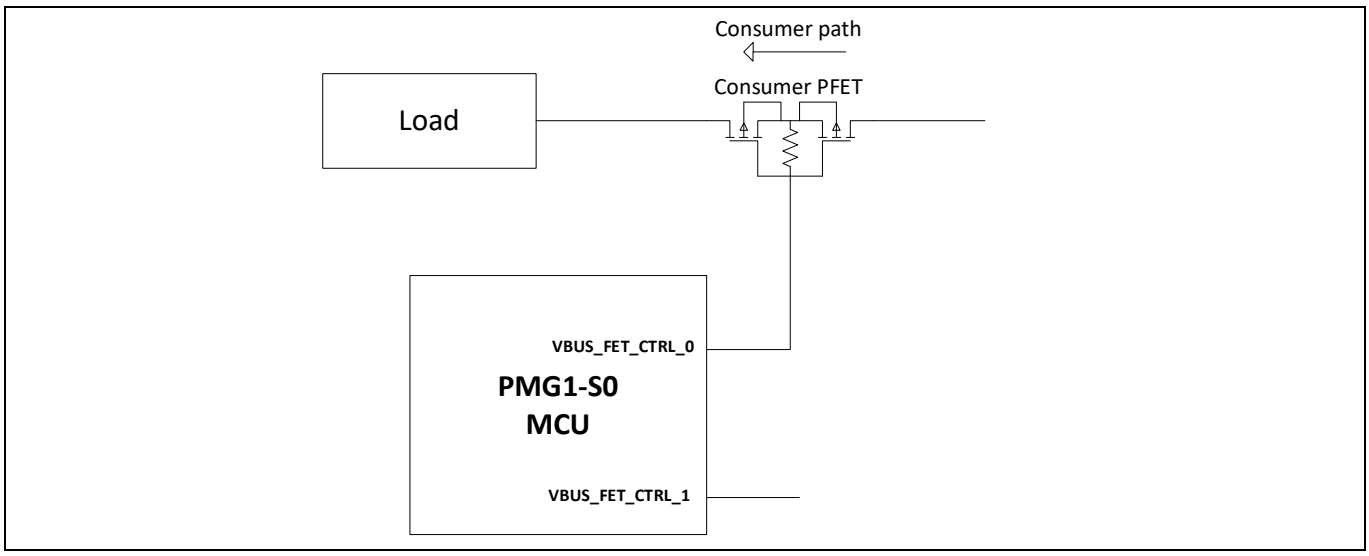

Figure 10 PMG1-S0 external FET control

PMG1-S1 has an integrated load switch controller with PFET driver to drive external PFETs on the consumer path in DRP and sink only designs. The gate diver requires an external pull-up. The load switch controller also has slew rate-controlled gate driver to drive external PFETs on provider path. The integrated load switch controller has more features compared to normal gate driver. See the PMG1-S1 datasheet [4] for details on the load switch controller.

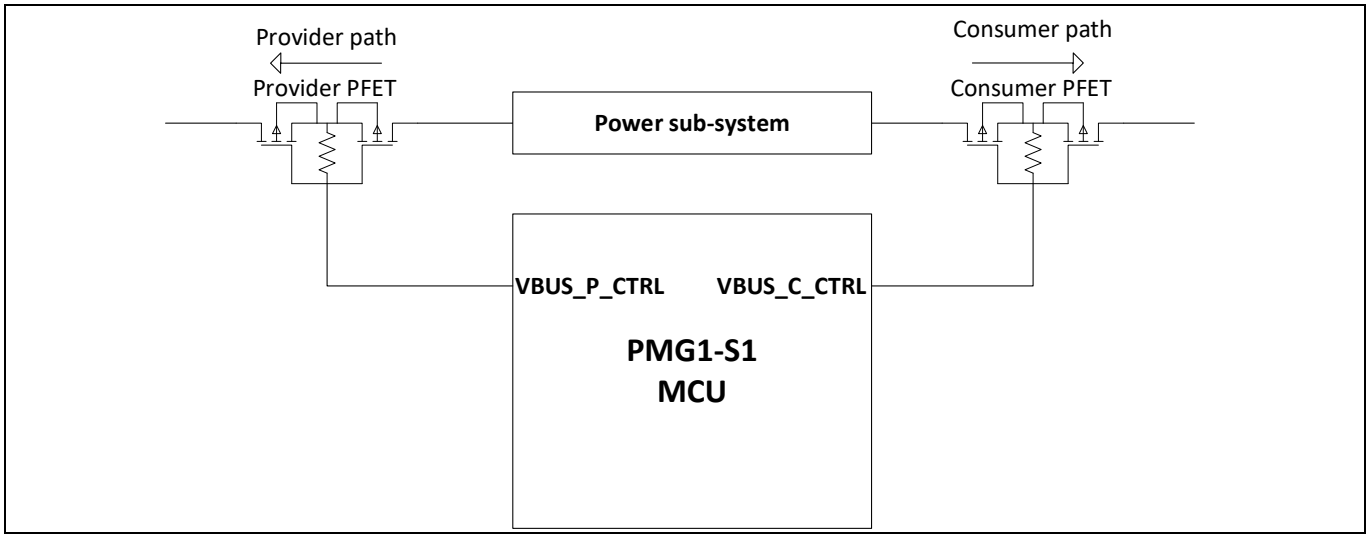

Figure 11 PMG1-S1 external FET control

Schematic design requirements

In the PMG1-S2 device, N-Channel FET (NFET) and PFET gate drivers are integrated with the MCU. The type of gate driver can be configured in hardware using the P1.0 GPIO pin, to support P and N type external FETs. Floating P1.0 indicates NFET driver and to configure as PFET driver, the pin should be connected to ground. PMG1-S2 has two pins, VBUS_P_CTRL0 and VBUS_P_CTRL1, for driving provider path FET and two pins (VBUS_C_CTRL0 and VBUS_C_CTRL1) for driving consumer path FET.

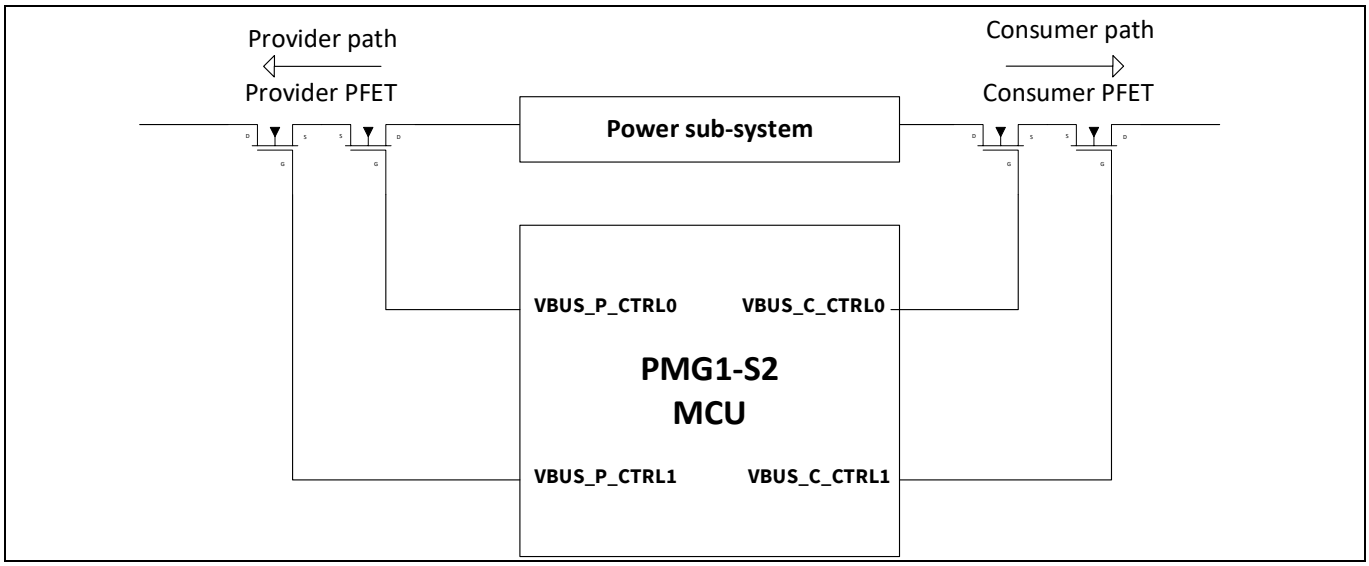

Figure 12 PMG1-S2 external FET control

Table 11 lists the PMG1 MCU pins assigned to the gate driver/load switch control.

Table 11 Load switch/gate driver signals

Load switch control signal	MCU Pin #	Description
PMG1-S0		
VBUS_FET_CTRL_0	3	External PMOS FET (PFET) control (30-V Tolerant) with internal pull-up 0: Path ON 1: Path OFF
VBUS_FET_CTRL_1	4	External PFET Control (30-V Tolerant) 0: Path ON High-Z: Path OFF To use this pin, provide external pull-up
PMG1-S1		
VBUS_P_CTRL	11	Slew Rate controlled I/O for enabling/disabling Provider side PFET 0: Path ON High Z: Path OFF
VBUS_C_CTRL	12	Pin for enabling/disabling Consumer side PFET 0: Path ON High Z: Path OFF
PMG1-S2		
VBUS_P_CTRL1	1	VBUS Gate Driver Control 1 for Provider Switch
VBUS_P_CTRL0	2	VBUS Gate Driver Control 0 for Provider Switch
VBUS_C_CTRL1	29	VBUS Gate Driver Control 1 for Consumer Switch
VBUS_C_CTRL0	30	VBUS Gate Driver Control 0 for Consumer Switch

4.8 Charger detection

The PMG1 MCU family integrates battery charger emulation and detection for USB BC 1.2 and Apple charge terminations. The DP and DM pins of the MCU connected to charger detect block. In PMG1-S1 device, charger detection is part of the internal HS Mux.

Following are the hardware design considerations for connecting DP and DM signals:

- In PMG1-S0 and PMG1-S2, short the A6 and B6 (DP) of the Type-C connector and route to the USBDP pin of the MCU. Short A7 and B7 (DM) and route to the USBDM pin of the MCU (**Figure 13**).
- In PMG1-S1, do not short the pins. Route the Type-C connector pins directly to the High-Speed (HS) pins of the MCU (**Figure 14**).
- Follow the USB HS signal routing consideration explained in Power domain for optimum performance.

Table 12 lists the pin number for USB HS/Charger detection signals on PMG1 MCUs.

Table 12 USB HS/Charger detection signals

HS Signal	MCU Pin#		
	PMG1-S0	PMG1-S1	PMG1-S2
USBDP	17	N/A	21
USBDM	16	N/A	22
USBDP_TOP	N/A	28	N/A
USBDP_BOT	N/A	26	N/A
USBDM_TOP	N/A	27	N/A
USBDM_BOT	N/A	25	N/A

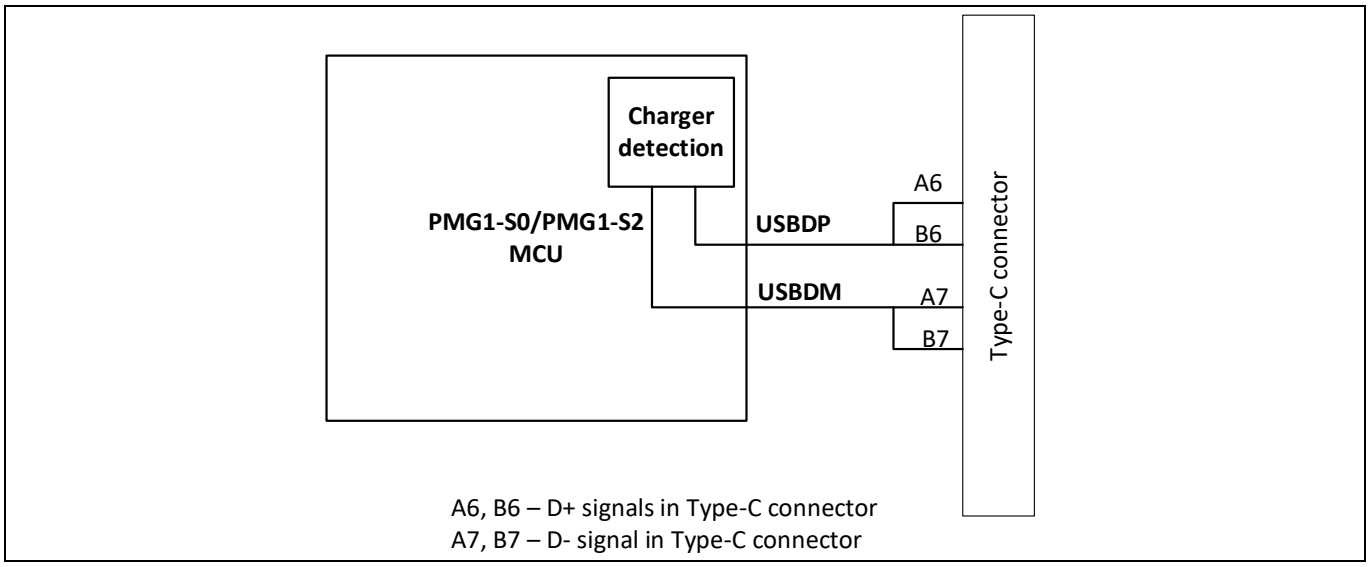

Figure 13 Charger detection in PMG1-S0 and PMG1-S2

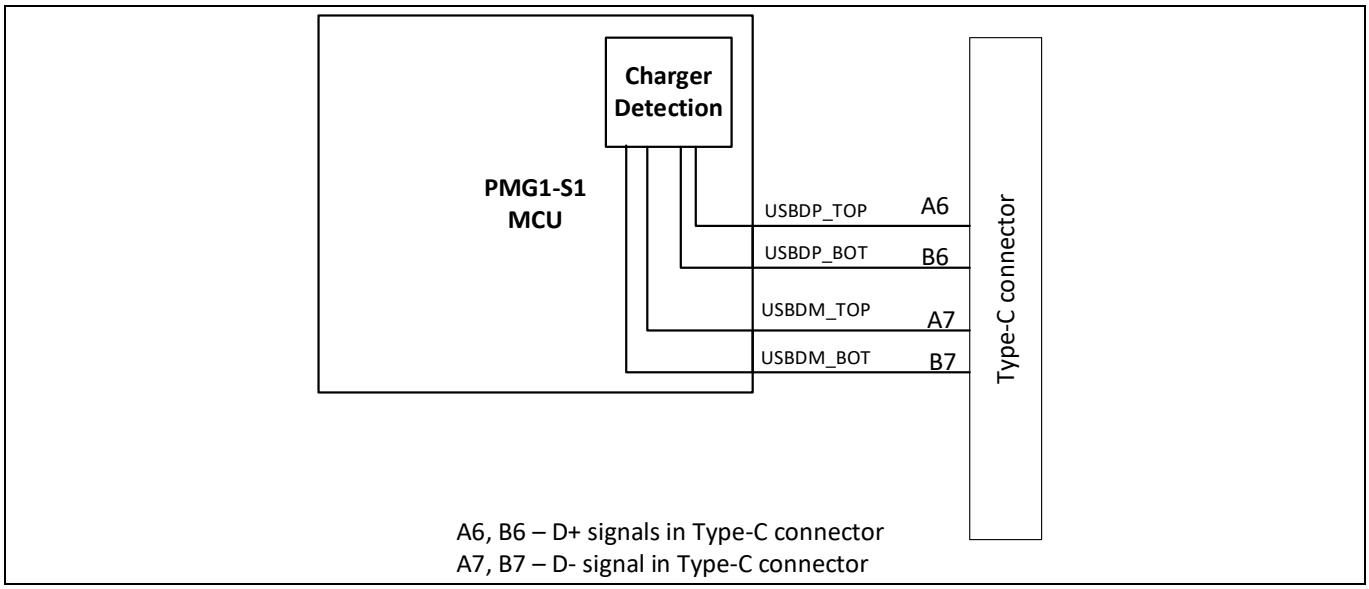

Figure 14 Charger detection in PMG1-S1

5 Electrical design consideration

5.1 ESD and EMI/EMC protection

PMG1 MCUs have built-in ESD protection on VBUS, OVT pin, and USB/USB PD lines. **Table 13** summarizes the built-in ESD protection of MCUs.

Table 13 Built-in ESD protection for PMG1 MCU

MCU	PMG1-S0	PMG1-S1	PMG1-S2
Contact Discharge	±8 kV on CC1, CC2, VBUS, P2.2, and P2.3 pins	No	±8 kV on CC1, CC2, VBUS, USBDP, USBDM, SBU1, and SBU2 pins
Air Discharge	±15 kV on CC1, CC2, VBUS, P2.2, and P2.3 pins	No	±15 kV on CC1, CC2, VBUS, USBDP, USBDM, SBU1, and SBU2 pins
HBM	± 2.2 kV	±2.2 kV	± 2.2 kV
CDM	± 500 V	± 500 V	± 500 V

The guidelines recommend adding ESD diodes on USB signals and CC lines for extended protection beyond the rated limits. The ESD diodes meet the requirements of IEC61000-4-2, and low input capacitance. Ferrite beads are not mandatory for all Type-C applications using PMG1, but it is recommended to connect the beads between the Type-C connector's shield and the system GND pin.

5.2 General PCB layout tips

There are many classic techniques for designing PCBs for low noise and EMC. This section explains some of these general techniques. These techniques can be used to improve the overall design of the system, EMI/EMC performance, noise handling, and so on:

- **Multiple layers:** Although they are more expensive, it is best to use a multi-layer PCB with separate layers dedicated to the VSS and VDD supplies. This provides good decoupling and shielding effects. Separate fills on these layers should be provided for GND, VDDIO, VSYS, VBUS, and VDDD.

  To reduce cost, a two-layer or even a single-layer PCB can be used. In that case, you must have a good layout for all and power and ground trace. But for designing USB PD systems, two-layer PCBs are not recommended, since the system has to handle a maximum power of 100 W.
- **Ground and power supply:** There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.

  The power supply should be close to the ground line to minimize the area of the supply loop. The supply loop can act as an antenna and can be a major emitter or receiver of EMI.
- **Decoupling:** The standard decoupling circuit for external power is a 100-µF capacitor. Supplementary 0.1-µF capacitors should be placed as close as possible to the VSS and VDD pins of the device to reduce high-frequency power supply ripple.

  Generally, you should decouple all sensitive or noisy signals to improve the EMC performance. Decoupling can be both capacitive and inductive.
- **Component position:** Separate the circuits on the PCB according to their EMI contribution. This will help reduce cross-coupling on the PCB. For example, separate noisy high-current circuits, low-voltage circuits, and digital components. The decoupling capacitors and the inductor (Buck Inductor) should be placed as close as possible to the device pins with minimum trace resistance.

- **Signal routing**: When designing an application, the following areas should be closely studied to improve the EMC performance:
  - Noisy signals, for example, signals with fast edge times
  - Sensitive and high-impedance signals
  - Signals that capture events, such as interrupts and strobe signals

  To improve the EMC performance, keep the trace lengths as short as possible and isolate the traces with VSS traces. To avoid crosstalk, do not route them near to or parallel to other noisy and sensitive traces.

5.3 PCB Selection and basic routing considerations

The PCB copper thickness should be 2oz minimum to handle a maximum current of 5 A.

5.3.1 Reference PCB stack up for PMG1 designs

5.3.1.1 1.2 mm, four-layer PCB stack up

Figure 15 shows the recommended stack up for a 1.2-mm thick PCB. The values of width (W) and spacing (S) are based on CY7110 EZ-PD PMG1-S0 Prototyping Kit.

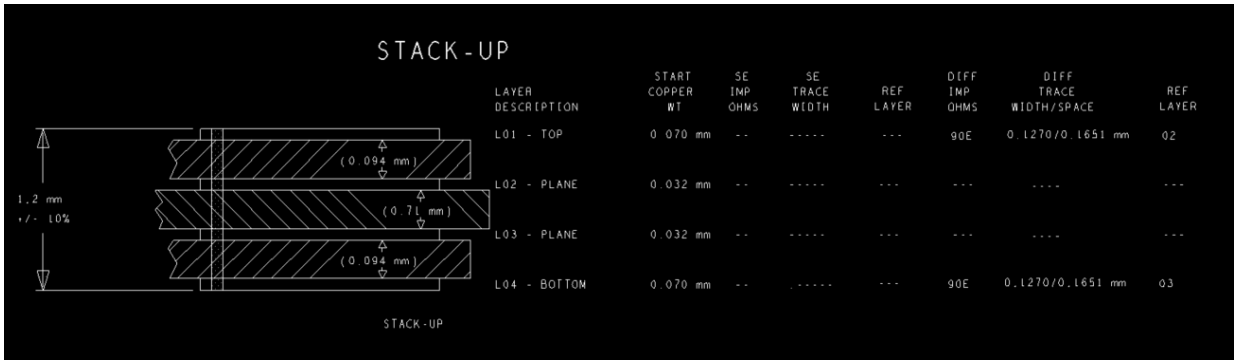

Figure 15 4-layer PCB stack up

5.3.1.2 1.2 mm, six-layer PCB Stack up

Figure 16 shows the recommended stack up for a 1.2-mm thick PCB. The values of width (W) and spacing (S) are based on CY7110 EZ-PD PMG1-S0 Prototyping Kit.

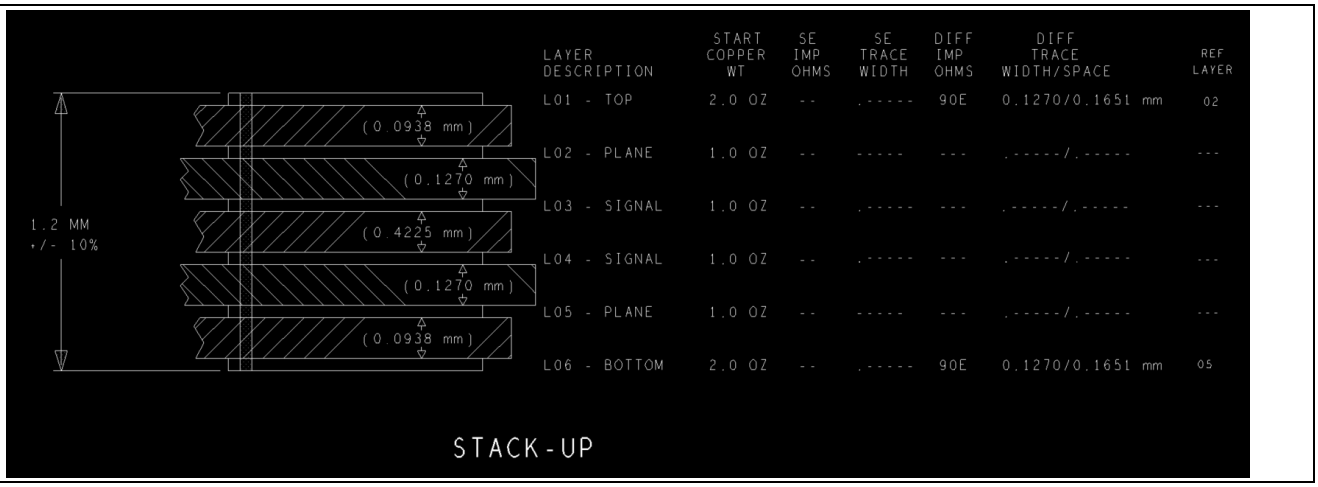

Figure 16 6-layer PCB stack up

5.4 Power domain

5.4.1 Placement of bulk and decoupling capacitors

- Place decoupling capacitors close to the power pins of the respective PMG controller for high- and low-frequency noise filtering as shown in **Figure 17**.
- Place the bulk capacitor, which acts as a local power supply, close to the power supply input and output headers and voltage regulators. Filter power inputs and outputs near the power headers to reduce the electrical noise. Ceramic or tantalum capacitors are recommended; electrolytic capacitors are not suitable for bulk capacitance.

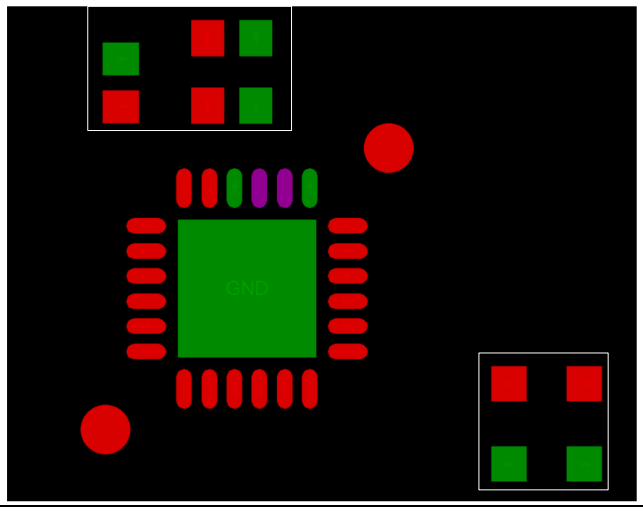

Figure 17 Placement of bulk and decoupling capacitors

5.4.2 Placement of power and ground planes

- There should be a single point for gathering all ground returns. Avoid ground loops, or minimize their surface area. All component-free surfaces of the PCB should be filled with additional grounding to create a shield, especially when using two-layer or single-layer PCBs.
- For design of system with USB PD functionality, use a high-performance substrate material for PCBs. According to the USB PD specification, the system may carry current up to 5 A. Thus, it is required to construct PCBs with 2-ounce (oz) copper thickness. Minimum recommended space between copper elements is 8 mil (0.203 mm).
- Use dedicated planes for power and ground. Use of dedicated planes reduces jitter on USB signals and helps minimize the susceptibility to EMI and RFI.
- Use cutouts on the power plane if more than one voltage is required on the board. **Figure 18** shows the cutouts on power plane, and various power domains are marked in different colors.

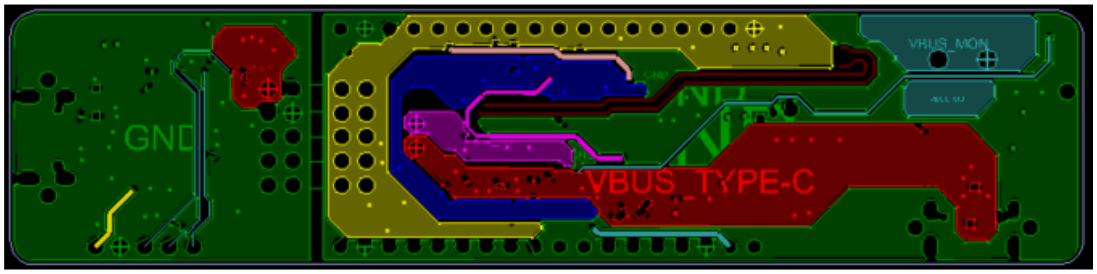

Figure 18 Power plane (Reference: PMG1-S1 kit)

- Place the power plane near the ground plane for good planar capacitance. Planar capacitance that exists between the planes acts as a distributed decoupling capacitor for high-frequency noise filtering, thereby reducing the electromagnetic radiation.

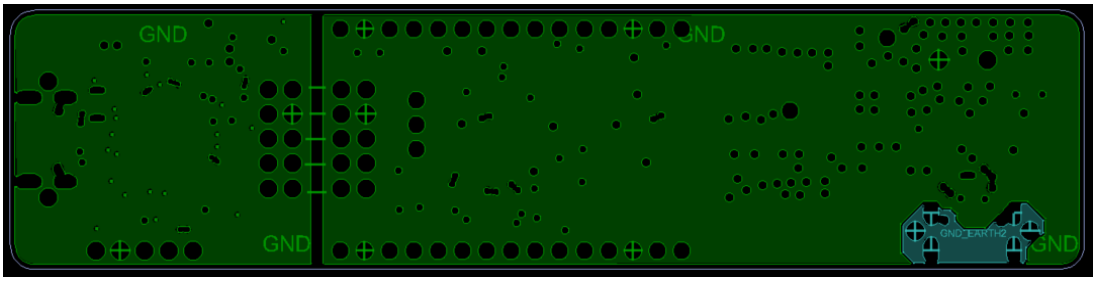

Figure 19 Ground plane (Reference: PMG1-S1 kit)

- Do not split or cut the ground plane. Splitting it increases the electrical noise and jitter on USB signals. Ground planes should be continuous. A discontinuous ground plane leads to larger inductance due to longer return current paths, which can increase EMI radiation. Also, multiple split grounds can cause increased crosstalk.

5.4.3 Power domain routing

- Route the power traces with a minimum of 40 mils trace width to reduce inductance.
- Keep the power traces short.
- Use larger vias (at least 30-mil pad, 15-mil hole) on power traces.
- Make the power trace width the same as that of the power pad. To connect power pins to the power plane, keep the vias very close to the power pads. This helps in minimizing the stray inductance and IR drop on the line.
- Solder the Exposed PAD (EPAN) of PMG1 MCUs onto an exposed ground pad provided in the PCB.
- If a switched-mode power supply is used, make sure that the power traces are far away from signal traces to avoid addition of power noise on signal or keep ground traces in between the signal traces.

5.4.4 Voltage regulation

Consider the following points while selecting voltage regulators/LDO to reduce electrical emissions and prevent regulation problems during USB suspend:

- Select voltage regulators that have minimum load current that is less than the board's load current during USB suspend. If the current drawn on the regulator is less than the regulator's minimum load current, then the output voltage may change.
- Place voltage regulators so that they straddle split VCC planes; this reduces emissions.

5.5 Routing of USB PD and USB-Data signals (Type-C)

5.5.1 Guidelines for routing Type-C (VBUS, GND, and CC) lines

- Group the VBUS pins together (all VBUS pins are brought out to the same plane using vias).
- Similarly, group the GND pins together (all GND pins are brought out to the same plane using vias).
- Place GND plane adjacent and below CC (CC1, CC2) lines. Traces from CC pins must be routed with a minimum of 20 mils trace width for VCONN operation.
- Route the signals as differential pair to the external Rsense resistor.

5.5.2 Guidelines for routing USB Data lines

- Match the High-Speed (DP and DM) signal trace lengths within 1.25 mm (50 mils) in PMG1 MCUs.
- In PMG1-S1, where USB High-Speed signals are routed through internal mux, ensure that the High-Speed signals are less than 3-inches (75 mm) between MCU and Type-C connector. Also, Htrace length, between the MCU and host connector, is less than three inches.
- Ensure that the differential pairs (USBDP, USBDM, USBDP_TOP, USBDP_BOT, USBDM_TOP, USBDM_BOT, USBDP_SYS and USBDM_SYS) have a minimum pair-to-pair separation of 0.5 mm.
- Minimize the use of vias.
- Select a grounded coplanar waveguide (CPWG) system as a transmission line method.
- Adjust the High-Speed signal trace lengths near the USB receptacle, if necessary.
- On USB signal lines, use as few bends as possible. Do not use a 90-degree bend. Use 45-degree or rounded (curved) bends if necessary (see **Figure 20**).

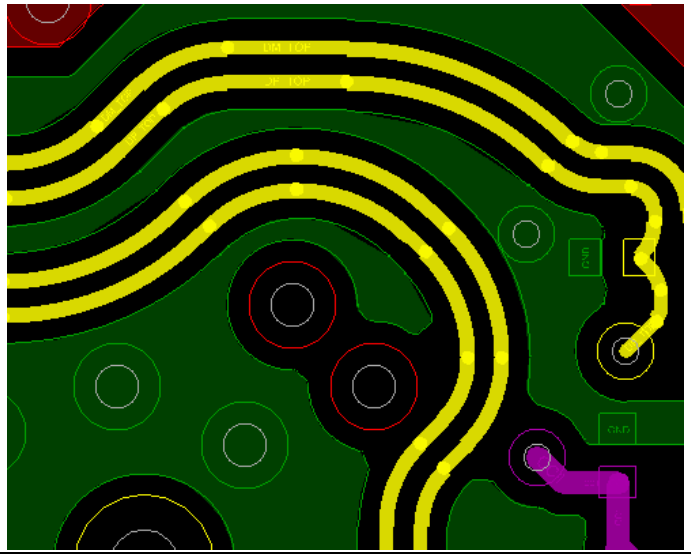

Figure 20 USB High-Speed signal routing - rounded bends

6 Schematics and layout review checklist

Table 14 Schematics and layout review checklist

No.	Schematic checklist	Answer (Yes/No/NA)
1	Are the decoupling capacitors and bulk capacitors connected on power supplies and CC pins as shown in **Figure 5** and **Figure 7**?	
2	Are the I²C lines provided with pull-up resistors (2.2 KΩ)? Is the GPIO for I2C interrupt pin the same in both bootloader and application firmware?	
3	Do the POR RC components meet the required reset times?	
4	Are the I²C lines provided with pull-up resistors to the 3.3-V domain?	
5	Is the recommended arrangement of FETs present on VBUS to control power provider and consumer path as shown in **Figure 11**, **Figure 12**, and **Figure 13**?	
6	Are all USB connector shields terminated properly?	
7	Is the VBUS discharge circuitry present in the design as shown in **Figure 13** for PMG1-S2?	
8	Are the VBUS discharge resistors rated for 2-W of power dissipation for PMG1-S2?	
Layout Checklist		
1	Are the decoupling capacitors and bulk capacitors placed close to the Type-C PD controller power pins?	
2	Is a 0.1-µF decoupling capacitor placed close to VCCD pin?	
3	Are the vias placed close to the Type-C PD controller power pins?	
4	Are the power traces routed away from the HS and Super-Speed (SS) data lines?	
5	Is the capacitor in the RC reset circuitry placed close to the reset pin of the Type-C PD controller?	
6	Has a dedicated and continuous GND plane been used?	
7	Are all VBUS pins on the Type-C connector brought on the same plane using vias?	
8	Are all GND pins on the Type-C connector brought on the same plane using vias?	
9	Is GND present adjacent to and below CC lines?	
10	Do the USB SS and HS signal lines match in length?	
11	Are the USB SS and HS signal lines provided with a solid ground plane underneath?	
12	Are the USB traces kept short?	
13	Do the USB traces have minimum bends and no 90-degree bends?	

Related documents

[1] Overview: **Infineon USB PD Controller Roadmap**

[2] Product Webpage:

- **EZ-PD PMG1 Webpage**

[3] Kit Webpages

- **CY7110**
- **CY7111**
- **CY7112**

[4] Datasheets

- **EZ-PD PMG1-S0 Datasheet**
- **EZ-PD PMG1-S1 Datasheet**
- **EZ-PD PMG1-S2 Datasheet**

[5] **AN232553 - Getting started with EZ-PD PMG1 on ModusToolbox**

Acronyms and abbreviations

Acronyms	Expansion
AC	Apple Charging
ADC	Analog-to-Digital Converter
Arm®	Advance RISC machine, a CPU architecture
BC	Battery Charging
CC	Configuration Channel
CDM	Charged Device Model
CPU	Central Processing Unit
CS	Current Sense
CSN	Current Sense Negative
CSP	Current Sense Positive
CYP	Cypress Programmer
DFP	Downstream Facing Port
DRP	Dual Role Port
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
FS	Full-Speed
GPIO	General Purpose Input/ Output
HBM	Human Body Model
HS	High-Speed
IC	Integrated Circuit
IDE	Integrated Development Environment
I^2C	Inter-Integrated Circuit, a communication protocol
I/O	Input/Output
LDO	Low Dropout Regulator
MCU	Microcontroller Unit
NC	No Connect
OCP	Over Current Protection
OVP	Over Voltage Protection
PCB	Printed Circuit Board
PD	Power Delivery
POR	Power-On-Reset
PWM	Pulse-Width Modulator
QFN	Quad-Flat No-lead, a type of IC packaging
RCP	Reverse Current Protection
R_D	Pull-down resistor on the USB Type-C CC wire used to indicate that the Port is a Sink

Acronyms and abbreviations

Acronyms	Expansion
R_{D-DB}	Pull-down resistor on the USB Type-C CC wire used to indicate that the Port is a dead battery sink
R_P	Pull-up resistor on the USB Type-C CC wire used to indicate that the Port is a Source
RX	Receiver
SAR	Successive Approximation Register
SCB	Serial Communication Block
SCL	I2C Serial Clock
SCP	Short Circuit Protection
SDA	I2C Serial Data
SPI	Serial Peripheral Interface, a communication protocol
SRAM	Static Random Access Memory
SWD	Serial Wire Debug
TCPWM	Timer/Counter Pulse-Width Modulator
TX	Transmit
Type-C	Latest USB connector and cable standard
UART	Universal Asynchronous Transmitter Receiver, a communication protocol
USB	Universal Serial Bus
USB-PD/ USB PD	USB Power Delivery
USB-FS	USB Full-Speed
UVP	Under Voltage Protection
XRES	External Reset I/O pin

Revision history

Document version	Date of release	Description of changes
**	2021-03-15	Initial release

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