

Converting STK25C48 to STK12C68

Introduction

This document provides guidance on converting a design that is currently using the STK25C48 to the Simtek recommended part STK12C68

Feature set and limitations of the STK 25C48

			/ = '
Function Category	STK25C48		STK12C68
Autostore	Yes, by specified slow VCC fall re		for immunity from ramp rate using a 68uf capacitor
Software store	Yes	Yes	
Software recall	Yes	Yes	

Package Comparison

The STK25C48 is only available in the 24 pin 600mil plastic dip package. The closest package is the 600 mil 28 pin PDIP and being larger may cause layout difficulty.

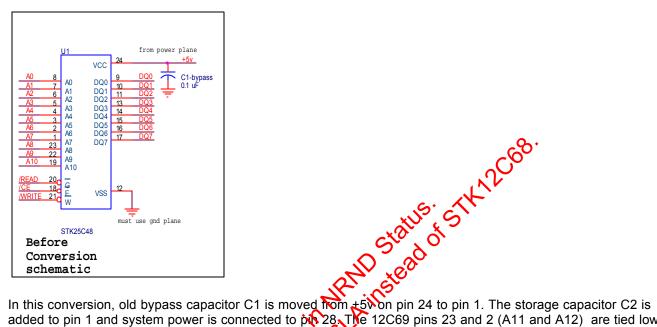
Package	PKCCode	STK25C48	STK12C68	Notes
350 mil SOIC – 28 pin	s S ing	Not available	Available	Surface mount – smallest PCB area
600 mil pdip 28 pin	W 3	Available	Available	Through hole
300 mil cdip 28 pin	CO	Not available	Available	Through hole
600 mil pdip 24pin	. W	Not available	Available	Through hole

Issues to consider during the conversion

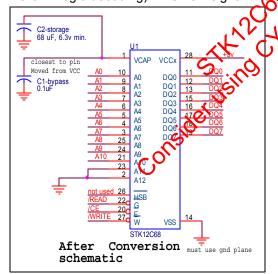
The key difference is that the STK25C48 has been internally configured to autostore but does not use a 68uf capacitor. This means there is no protection from power that falls too fast. This is no longer a recommended application and is no longer supported by Simtek. The STK12C68 will be wired using the 68uf power storage capacitor on the VCAP pin. The converted STK12C68 application will then be fully immune from the minimum ramp rate requirement. This application will process an autostore using power stored on a 68uf capacitor. Also, the new HSB signal is unused. All other pins have the same function.

Schematic changes for conversion:

This is a feature upgrade and conversion of the STK25C48 to the mainstream STK12C68. Applications requiring a minimum ramp rate are no longer supported or recommended. So, this conversion is to the full featured STK12C68 application with autostore being powered from a storage capacitor. This requires the addition of a 68uf capacitor and wired to VCAP pin 1. Also, the bypass capacitor moves to the VCAP pin. The choice of package is open with the "S" package being the most area efficient surface mount choice.



added to pin 1 and system power is connected to pix 28 The 12C69 pins 23 and 2 (A11 and A12) are tied low or you may utilize the additional memory space: of you want the space, be sure to expand the memory space in the /E logic decoding). The new signal /HSBs left open and unused.



On the next page, pin by pin comparisons of the two show all pins are the same except for the bypass capacitor moving to pin 1 and connected to system power, +5v.

Corresponding pin ConnectionsPin for pin comparison of the two parts is given in the table below:

STK25C48 NAME	Pin	STK12C68 NAME	Pin	Comments
none		VCAP	1	Must connect 0.1UF BYPASS and 68uf, 6.3v min.
none		A12	2	Tie to gnd
A7	1	A7	3	No change
A6	2	A6	4	ű.
A5	3	A5	5	ű.
A4	4	A4	6	66
A3	5	A3	7	66
A2	6	A2	8	66
A1	7	A1	9	
A0	8	A0	10	
DQ0	9	DQ0	11	
DQ1	10	DQ1	12	"
DQ2	11	DQ2	13	" " " " " " " " " " " " " " " " " " " "
VSS	12	VSS	14	
DQ3	13	DQ3	15	
DQ4	14	DQ4	16	" 20 200
DQ5	15	DQ5	17	
DQ6	16	DQ6	18	
DQ7	17	DQ7	19	
E#	18	E#	8 0	(h)
A10	19	A10	21	
G#	20	G#	22	"
none		A11 (23	Tie to gnd
A9	22	A9 5 0	24	No change
A8	23	A9 5 0	25	ii
none		I HQB 🔥 🗸	26	LEAVE OPEN UNUSED
W#	21	W#	27	No change
VCC	24	VC(\$X)	28	This pin now must continue to be connected to
		C _O ,		+5v, bypass of 0.1uF is ok but unneeded.