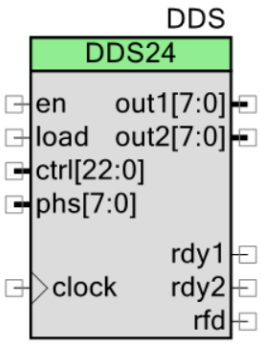
DDS24: Direct Digital Synthesis 24-bit generator

0.0

Features



- Implements 24-bit DDS arbitrary frequency generator.
- Dual outputs with arbitrary phase shift.
- Output bus with variable width.
- Digital input bus for hardware control.
- Hardware load (strobe) of control parameters.

General description

The DDS24 component implements arbitrary frequency generator based on Direct Digital Synthesis [1-4] and provides digital output in wide frequency range with 24-bit resolution. Component can provide frequency in the range between 2^{-24} and 2^{-1} of the input clock frequency with step resolution $F_{clock}/2^{-24}$. Component can synchronously generate two signals of the same frequency, which can be arbitrary phase shifted against each other with 8-bit resolution. The outputs can have variable bus width, allowing generation of harmonics (2x, 4x, ..., 128x) of the prime frequency. At runtime, frequency and phase can be controlled by either API functions or digital bus; else hardcoded values can be set at the design time.

When to use DDS24 component

Component was developed for high resolution frequency generation as a part of a lock-in detector project. Typical applications for this component are: test equipment with tunable frequency/phase generator, sweep frequency generator. Hardware control allows for generation of frequency modulated (FM) and phase-modulated (PM) outputs without CPU intervention. Output bus allows direct connection to DAC or a lookup table. Several demo projects are provided.

Input-output connections

en – clock enable input

This input is a level-sensitive enable, determining whether the DDS accumulator value will be incremented rising edges on the clock, active high. The pin is visible when either “Hardware only” or “Hardware & Software” options are selected. When “Auto enable” or “Software only” option are selected, the terminal is hidden. When visible, the pin must be connected to valid digital source.

load – input for strobed update of the DDS data

This pin is shown on the symbol when HardwareLoad option is selected. If selected, the data are strobed on each positive edge of the “load” signal. This pin is used for periodic sampling applications, such as sweep generator, when deterministic timing is important. When visible, the pin has to be connected to digital source.

Note: The pin has no effect when both ControlFreq and ContolPhase options are set to “Hardcoded” (see Functional Description section for details).

ctrl[22:0] – digital input of tuning word

This pin is for digital input of tuning word. Using this input the DDS frequency can be controlled entirely by hardware. Visibility of this pin is controlled by setting the ControlFreq option to the “Digital bus”. If visible, the pin must be connected to valid digital source.

phs[7:0] – digital input of phase

This pin is for digital input of “out2” phase. Using this input the out2_phase can be controlled entirely by hardware. Visibility of this pin is controlled by setting the ControlPhase option to the “Digital bus”. If visible, the pin must be connected to valid digital source.

clock – input clock

DDS accumulator value increments on rising edge of the clock. Valid clock source must be connected to the component. The frequency of the clock signal is limited to the range defined in the DC and AC Electrical Characteristics section.

out1[P-1: 0] – primary digital output

The output bus connected to top MSBs of the DDS accumulator. The bus width P is user-selectable, highest is 8. The bus MSB oscillates at DDS output frequency F_{out}, 50% nominal duty cycle. Consecutive bits oscillate at even harmonics { $2\times F_{out}$, $4\times F_{out}$, …, $128\times F_{out}$ } correspondingly. This pin is always visible. The pin doesn't have to be connected.

out2[Q-1: 0] – secondary digital output

The pin is similar to the "out1", except that its phase can be arbitrary shifted relative to "out1" using parameter out2_phase. Visibility of this pin controlled by option out2_enable. Outputs 1 and 2 can have individual bus width. Use "out2" for in-phase reference or quadrature signal.

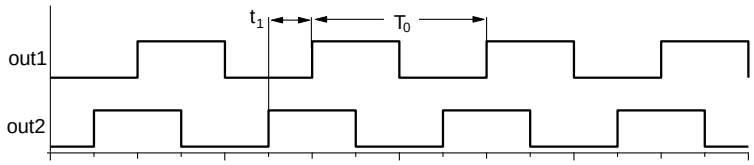


Figure 1. DDS24 example of quadrature outputs: out2 phase leads out1 by 90 deg.

rdy1 – data ready output

This pin provides sync pulse whenever the bus "out1" changes its state and is ready to be strobed for data. The pin is optionally shown on the symbol, when option rdy_enable is selected(*). The pin doesn't have to be connected.

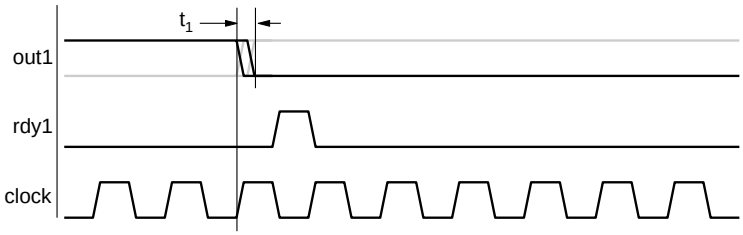


Figure 2. Data ready timing diagram. Typical jitter time t1 < 3ns.

rdy2 – data ready output

This pin provides sync pulse whenever the bus "out2" changes its state and is ready to be strobed for data. This pin is optionally shown on the symbol when option rdy_enable is selected and "out2" is visible. The pin doesn't have to be connected.

* Pins rdy1 and rdy2 are resources-hungry. Consider using clock or inverted clock for low-speed applications.

rfd – ready for data output

Ready for data output pin indicates that previous Frequency and Phase values has been applied to the Accumulator, and the component is ready to accept new data. If component is in enabled state, then pin goes into high state one full clock after data has been strobed by the "load" input. Pins "load" and "rfd" are activated as a group when the HardwareLoad option is selected. The pin is typically used to generate an interrupt signaling CPU to load next data into DDS registers. The pin doesn't have to be connected.

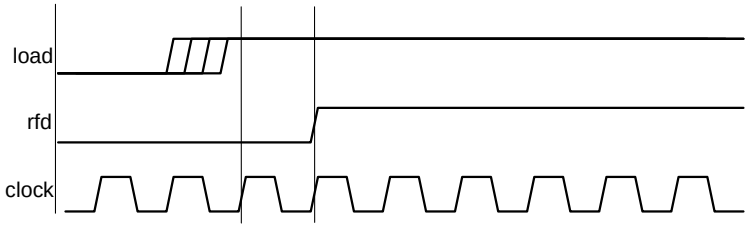
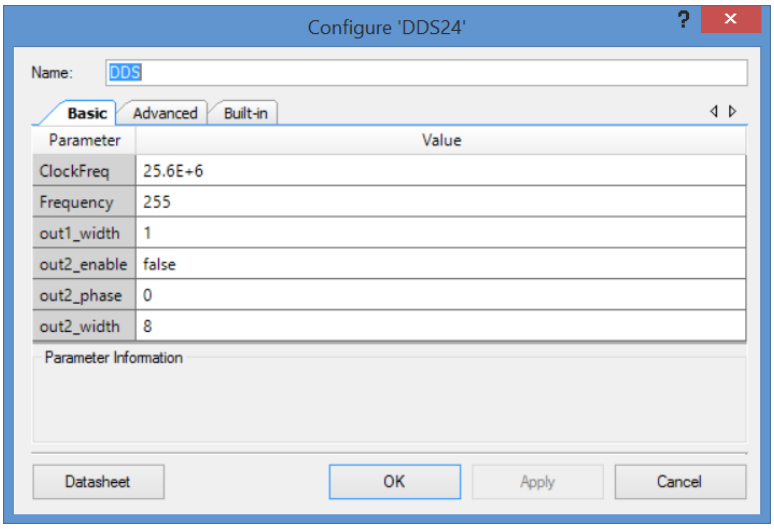


Figure 3. Timing diagram for "load" and "rfd" pins.

Parameters and Settings

Basic dialog provides following parameters:



ClockFreq (float)

The frequency of the input clock connected to the “clock” input, measured in Hz. This value should not exceed the maximum allowed frequency for the component, specified in the DC and AC Electrical Characteristics section. Parameter has effect only when ControlFreq option is set to either “API call” or “Hardcoded”.

Frequency (float)

Output set frequency. Valid range is from $F_{clock}/2^{25}$ to $F_{clock}/2 - F_{clock}/2^{25}$ (or roughly from ≈ 0 to $\approx F_{clock}/2$). Actual output frequency value will be rounded to the nearest frequency bin due to the finite (24-bit) resolution of the component. See Functional Description section for details. Parameter has effect only when ControlFreq option is set to either “API call” or “Hardcoded”.

out1_width [1…8]

Terminal “out1” bus width. Valid range is from 1 to 8. Set width to 1 for single wire output.

out2_enable (bool)

Enables secondary output terminal “out2”. If enabled, “out2” terminal appears on the symbol.

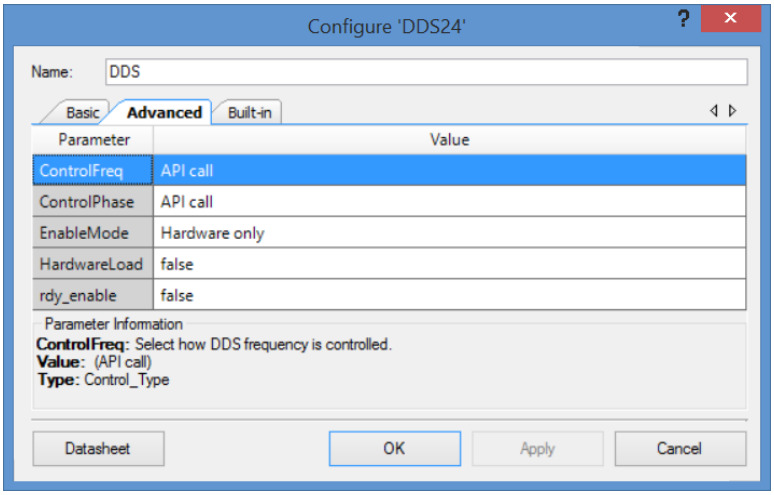
out2_phase (uint8)

Phase shift between “out2” and “out1”. Values from 0 to 255 correspond to 0 to 360° (“out2” leads “out1”). Values 0 to -255 correspond to 0 to -360° (“out2” is delayed against “out1”). Parameter has effect only when ControlPhase option is set to either “API call” or “Hardcoded”.

out2_width [1…8]

Terminal “out2” bus width. Valid range is from 1 to 8. Set width to 1 for single wire output.

Advanced dialog provides following parameters:



ControlFreq (API call | Hardcoded | Digital bus)

Select how output frequency is controlled. Valid options are “API call”, “Hardcoded” and “Digital bus”. See Functional Description section for details.

ControlPhase (API call | Hardcoded | Digital bus)

Select how “out2” phase is controlled. Valid options are “API call”, “Hardcoded” and “Digital bus”. See Functional Description section for details.

EnableMode (Auto enable | Software only | Hardware only | Hardware & Software)

Select how DDS enable state is controlled. When “Auto enable” option selected, the component always remains enabled. Select “Software only” option to enable/disable component by API functions. Select “Hardware only” for hardware control. Select “Hardware & Software” for both. Disabling component freezes all outputs in their current state.

HardwareLoad (bool)

Select this option for deterministic update of control parameters (frequency and phase) on the rising edge of the “load” signal.

rdy_enable (bool)

Sets visibility of the “rdy1” and “rdy2” pins on the component.

Application Programming Interface

Function	Description
`DDS24_Start()`	Initializes and enables component
`DDS24_Stop()`	Stops (disables) component
`DDS24_Init()`	Initializes component
`DDS24_Enable()`	Enables component
`DDS24_SetFrequency(double Freq)`	Sets desired output frequency
`DDS24_SetPhase(uint8 Phase)`	Set “out2” phase shift
`DDS24_GetOutFreq()`	Returns actual output frequency
`DDS24_GetFrequency()`	Returns set frequency
`DDS24_GetPhase()`	Returns phase shift

void DDS24_Start()

Description: Initializes and enables the component. This is default method to initialize component. Function has effect only when API calls are used to update internal control registers, that is when either ControlFreq or ControlPhase option is set to “API call” or when EnableMode parameter is set to “Software only” or “Hardware & Software”.

Parameters: none.
Return Value: none.

void DDS24_Stop()

Description: Stops (disables) the component. Calling this function inhibits the sample clock and freezes the output in the current state. Function has effect only if EnableMode parameter is set to “Software only” or “Hardware & Software”.

Parameters: none.
Return Value: none.

void DDS24_Init()

Description: Initializes the component, that is calculates and sets DDS tuning word and phase shift based on current parameters. Once initialized, the component can be enabled and disabled (stopped) multiple times without the need for re-initialization. Function has effect only when either ControlFreq or ControlPhase option is set to “API call”.

Parameters: none.
Return Value: none.

void DDS24_Enable(void)

Description: Enables DDS clock. It is not necessary to call DDS_Enable() because the DDS_Start() API calls this function, which is the preferred method to begin the component operation. Calling this function has effect only if EnableMode parameter is set to “Software only” or “Hardware & Software”.

Parameters: none.
Return Value: none.

uint8 DDS24_SetFrequency(double Freq)

Description: Sets DDS output frequency. Due to the finite resolution (24-bit), the actual output frequency is rounded to the nearest frequency bin within the resolution of the component. See Functional Description section for details. Has effect only if ControlFreq option selected is “API call”.

Parameters: Freq – desired DDS output frequency in Hz. Valid range depends on the input clock frequency: min. $F_{clock}/2^{25}$, max. $F_{clock}/2 - F_{clock}/2^{25}$**.**

Return Value: 1 – success, 0 – fail (resulting tuning word is outside valid range 1 … 8’388’607).

void DDS24_SetPhase(uint8 Phase)

Description: Sets “out2” phase shift. Has effect only if “out2” is enabled and ControlPhase option selected is “API call”.

Parameters: Phase - Value from 0 to 255 corresponds to 0 to 360° (“out2” leads “out1”). Value from 0 to -255 corresponds to 0 to -360° (“out2” is delayed vs. “out1”).

Return Value: none.

double DDS24_GetOutFreq()

Description: Returns actual DDS output frequency. Has effect only if ControlFreq option selected is “API call”. Note that output frequency may deviate from the set frequency due to the finite (24-bit) resolution of the component. See Functional Description section for details.

Parameters: none.

Return Value: Returns value of the calculated output frequency in Hz.

double DDS24_GetFrequency()

Description: Returns DDS set frequency. Has effect only if ControlFreq option selected is “API call”.

Parameters: none.

Return Value: current value of the set frequency in Hz.

uint8 DDS24_GetPhase()

Description: Returns current value of phase shift. Has effect only if ControlPhase option selected is “API call”.

Parameters: none.

Return Value: current phase. Value from 0 to 255 corresponds to 0 to 360°.

Functional Description

The principles of operation of DDS are available elsewhere [1-4]. A typical DDS relies on an accumulator to recursively sum the digital input tuning word at the rate of the sample clock (Figure 4). This produces a time series of digital words at the output of the accumulator that increases linearly until the accumulator rolls over [2].

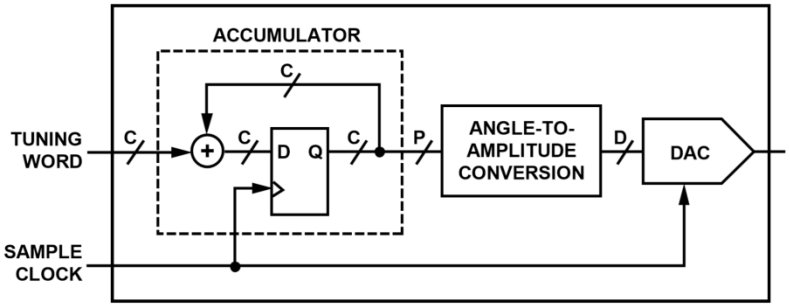


Figure 4. Typical Accumulator-based DDS architecture [2].

The DDS24 implementation is limited to basic form as *phase generator* (the Accumulator only). The DDS24 accumulator is 24-bit deep, but the output is truncated to top MSBs of user-selectable width *P* ($P \leq 8$). Neither Angle-to-Amplitude conversion module, nor DAC are included in current implementation of the component.

The output frequency of the DDS24 is governed by the equation

$$F_{out} = \frac{tuning\_word}{2^{24}} F_{clock} . \quad \text{(Eq. 1)}$$

For desired frequency F_{set}, the tuning word must be:

$$tuning\_word = round\left(\frac{F_{set}}{F_{clock}} 2^{24}\right). \quad \text{(Eq. 2)}$$

Therefore, instead of producing frequency F_{set}, actual DDS output falls into one of discrete bins: { $F_{clock}/2^{24}$, $2\times F_{clock}/2^{24}$, $3\times F_{clock}/2^{24}$, … , $(2^{23}-1)\times F_{clock}/2^{24}$ }, yielding frequency resolution:

$$\Delta F_{out} = F_{clock}/2^{24} \quad \text{(Eq. 3)}$$

For example, setting sample clock to 16’777’216 Hz (=2^{24}) gives DDS24 resolution of 1 Hz, with ability to produce any[*] of the frequencies: 1, 2, 3, … , 8’388’607 Hz. Any other set frequency will be rounded to closest bin, e.g. setting F_{set}=1.6 Hz will produce 2 Hz output. To get better frequency resolution select lower clock frequency. For example, using clock frequency of 1’677’721.6 Hz gives DDS24 resolution of 0.1 Hz, etc.

[*] F_{set}=0 and Fset=$F_{clock}/2$ yields no DDS output.

Note that output frequency deviation from the set point is never more than half bin away, so the absolute accuracy of DDS is twice better than its step resolution:

$$abs(F_{out} - F_{set}) \leq \Delta F_{out}/2 = F_{clock}/2^{25}. \quad \text{(Eq. 4)}$$

The maximum frequency the DDS can generate is given by the uniform sampling theorem (Nyquist): $F_{MAX} = (2^{23}\text{-}1)\times F_{clock}/2^{24} \approx F_{clock}/2$. The closer is F_{out} to $F_{clock}/2$, the more distorted and jittery the output wave, the harder the analog reconstruction using a low-pass filter. See section DC and AC Electrical Characteristics on practical limits on the clock frequency.

DDS24 control inputs

DDS24 can be controlled: (i) by using API functions, (ii) by setting hardcoded values at design time or (iii) by using a digital bus (Figure 5). These options are available for frequency and phase independently through parameters ControlFreq and ControlPhase in the Advanced Dialog.

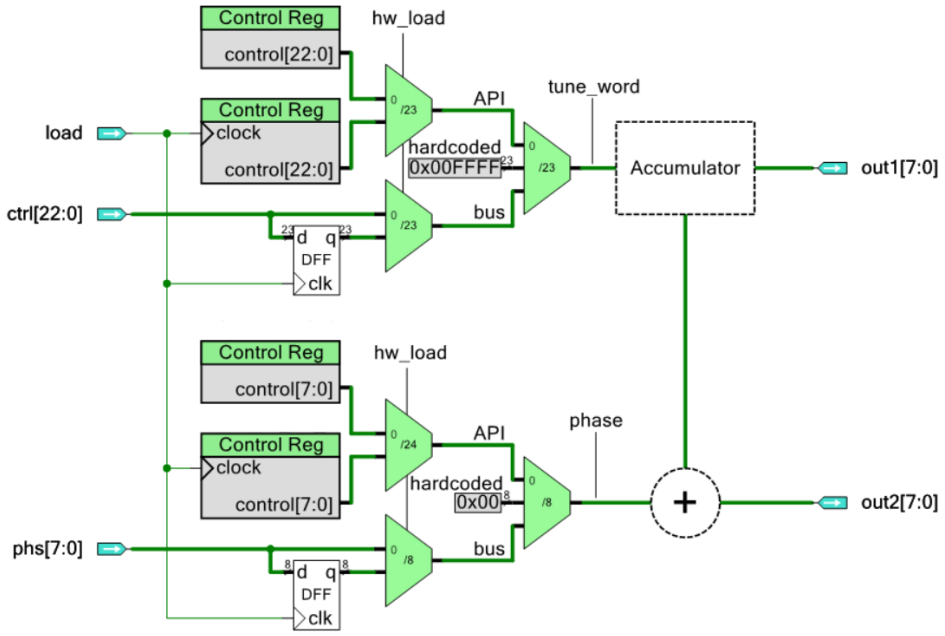


Figure 5. Block diagram of frequency and phase controls.

"API call" option allow updating DDS parameters at run-time, but consume extra resources. If HardwareLoad is enabled, the register value is strobed on the rising edge of the "load" signal. Hardware load allows for deterministic parameters update, while CPU is busy with other tasks.

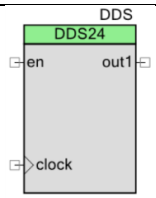
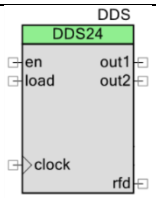
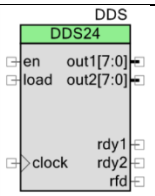
"Hardcoded" option forces DDS24 to use value specified in configuration dialog at design time. This saves UDB resources, but the value can't be changed at run-time. Such option may be useful, for example, when quadrature outputs are needed.

"Digital bus" option allows for direct hardware control of the tuning word and phase. API calls have no effect in this mode. Use Equation 2 to calculate tuning word for desired output frequency. If HardwareLoad is enabled, the bus is strobed on the rising edge of the "load" signal.

Resources

The DDS24 component is written in Verilog and does not utilize UDB Datapath resources. The component was tested using PSoC5LP (CY8C5868-LP035), summary is provided below. Component's use on PSoC4M is restricted to minimal configuration.

Table 1. PSoC5LP resource usage.

Options selected	Minimal configuration[1]		Medial configuration[2]		Maximal configuration[3]	
out2_enabled	☐		☑		☑	
ControlFreq	Hardcoded		API call		API call	
ControlPhase	—		API call		API call	
EnableMode	Hardware only		Hardware & Software		Hardware & Software	
HardwareLoad	☐		☑		☑	
rdy_enable	☐		☐		☑	
8-bit output	☐		☐		☑	
						
UDB Resource Type	Used	% Used	Used	% Used	Used	% Used
Macrocells	24	12.50%	33	17.19%	62	32.29%
Unique Pterms	24	6.25%	64	16.67%	121	31.51%
Datapath Cells	0	0.00%	0	0.00%	0	0.00%
Status Cells	0	0.00%	1	4.17%	1	4.17%
Control Cells	0	0.00%	5	20.83%	5	20.83%

1. Single output configuration, no run-time control. 2. Dual output configuration, API run-time control.
3. Dual bus output configuration, API run-time control.

DC and AC Electrical Characteristics

Table 2. Maximum clock frequency vs. operation temperature range.

Parameter	Description	-40 °C – 85 °C	0 °C – 85 °C
F_{CLOCK}, Max.	Maximum allowed sample clock	36.5 MHz	50.7 MHz

Clock Selection

Component requires a clock attached to it. DDS output accuracy as good as accuracy of the sample clock. For maximum accuracy use quartz oscillator (XO) as a reference source for PSoC PLL; using internal oscillator (IMO) diminishes accuracy of DDS24. Be aware that the actual frequency produced by the sample clock may deviate from the display value. Always measure and apply actual frequency of the clock in the settings Dialog. For example, it appeared that XO attached to the test board produced frequency of approx. 23.9978 MHz. Using that value in set Dialog instead of the nominal 24.0 MHz allowed for DDS accuracy of better than 0.0001%.

PSoC's clock PLL is capable of generating various frequencies from XO, but resulting frequency may deviate by few percent from the nominal value displayed on the clock symbol. For best accuracy, always measure and apply in the settings Dialog the actual clock frequency.

Sample Firmware Source Code

Basic DDS24 application example (Figure 6) requires updating only input clock and output frequency parameters in the Basic dialog.

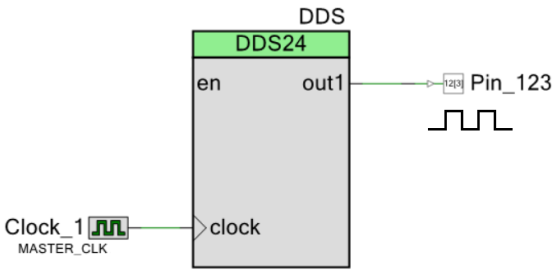


Figure 6. Basic application example.

Several demo projects are provided alongside the component: software and hardware controlled sweep frequency generator, dual output generator with variable phase shift. Advanced demos include[(*)] sine wave generator, a sensor with lock-in detector, AM- and FM-modulation examples, voltage controlled oscillator (VCO), arbitrary wave generator, etc.

[*] To be provided later

Performance

The component is written in Verilog and does not consume CPU resources. Only time CPU is involved when API calls are used to update DDS24 control registers.

Features not included in current release:

- Pipelined Accumulator
- Phase shift range options (-90° ÷ 90° | -180° ÷ 180°)
- Variable DDS resolution
- DMA control
- Reset input

Component Changes

Version	Description of changes	Reason for changes/impact
0.0	Version 0.0 is the first beta release of the DDS24 component	

References

1. L. Cordesses, DSP Tips&Tricks, Direct Digital Synthesis: A Tool for Periodic Wave Generation (Part 1) & (Part 2).
2. Analog Devices, AN-953. Direct Digital Synthesis (DDS) with a Programmable Modulus.
3. Analog Devices, MT-085. Fundamentals of Direct Digital Synthesis (DDS).
4. Analog Devices, A Technical Tutorial on Digital Signal Synthesis.