



Technical Reference Manual

**BCM20732S**

## **Bluetooth Low Energy SiP Module**

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## Revision History

| <b>Revision</b>    | <b>Date</b> | <b>Change Description</b>  |
|--------------------|-------------|--|
| MMP20732S-TRM106-R | 03/24/16    | <b>Updated:</b> <ul style="list-style-type: none"><li>• <a href="#">Table 5: "Current Consumption," on page 15.</a></li></ul>  |
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## About This Document

### Purpose and Audience

This document provides descriptions of the interfaces, pin assignments, and specifications of Broadcom® BCM20732S Bluetooth Low Energy (BLE) System-in-Package (SiP) module. It is intended for designers who are responsible for adding the BCM20732S module to wireless input devices including heart-rate monitors, blood pressure monitors, proximity sensors, temperature sensors, and battery monitors.

### Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: <http://www.broadcom.com/press/glossary.php>.

### Document Conventions

The following conventions may be used in this document:

| Convention  | Description   |
|-------------|---|
| <b>Bold</b> | User input and actions: for example, type <b>exit</b> , click <b>OK</b> , press <b>Alt+C</b>                            |
| Monospace   | Code: #include <iostream><br>HTML: <td rowspan = 3><br>Command line commands and parameters: w1 [-1] <command>          |
| < >         | Placeholders for <i>required</i> elements: enter your <username> or w1 <command>  |
| [ ]         | Indicates <i>optional</i> command-line parameters: w1 [-1]<br>Indicates bit and byte ranges (inclusive): [0:3] or [7:0] |

## Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, bills of material, PCB layout information, and software updates through its customer support portal. For a CSP account, contact your Broadcom Sales or Engineering support representative.

General WICED support is available to registered users within the Broadcom Support Community forums online: <http://community.broadcom.com/welcome>.

## Overview

The BCM20732S is a compact, highly-integrated Bluetooth low-energy (BLE) system-in-package (SiP) module. The BCM20732S SiP includes an embedded BLE antenna, 24 MHz clock, and 512 Kb EEPROM, so only a minimal set of external components is needed to create a standalone BLE device.

The BCM20732S is designed to accelerate time-to-market. The Bluetooth stack and several application profiles are built into the module, allowing customers to focus on their core applications. To further reduce application development time, the BCM20732S includes integrated software support, with one-click installation of the complete environment and a one-click compile/build/link/load cycle. All this, coupled with an ultra-small form factor and support for a wide voltage range, makes the BCM20732S well suited for virtually any Bluetooth Smart application.

## Features

- ARM Cortex-M3 microcontroller unit (MCU)
- Embedded 512 Kb EEPROM
- Broadcom Serial Control (BSC), SPI, and UART interfaces
- FCC and CE compliant
- RoHS compliant, certified lead- and halogen-free
- Moisture Sensitivity Level (MSL) 3 compliant
- 6.5 mm × 6.5 mm × 1.2 mm Land Grid Array (LGA) 48-pin package

## Application Profiles

The following profiles are supported in BCM20732S ROM:

- Battery status
- Blood pressure monitor
- Find me
- Heart rate monitor
- Proximity
- Thermometer
- Weight scale
- Time
- Blood glucose monitor

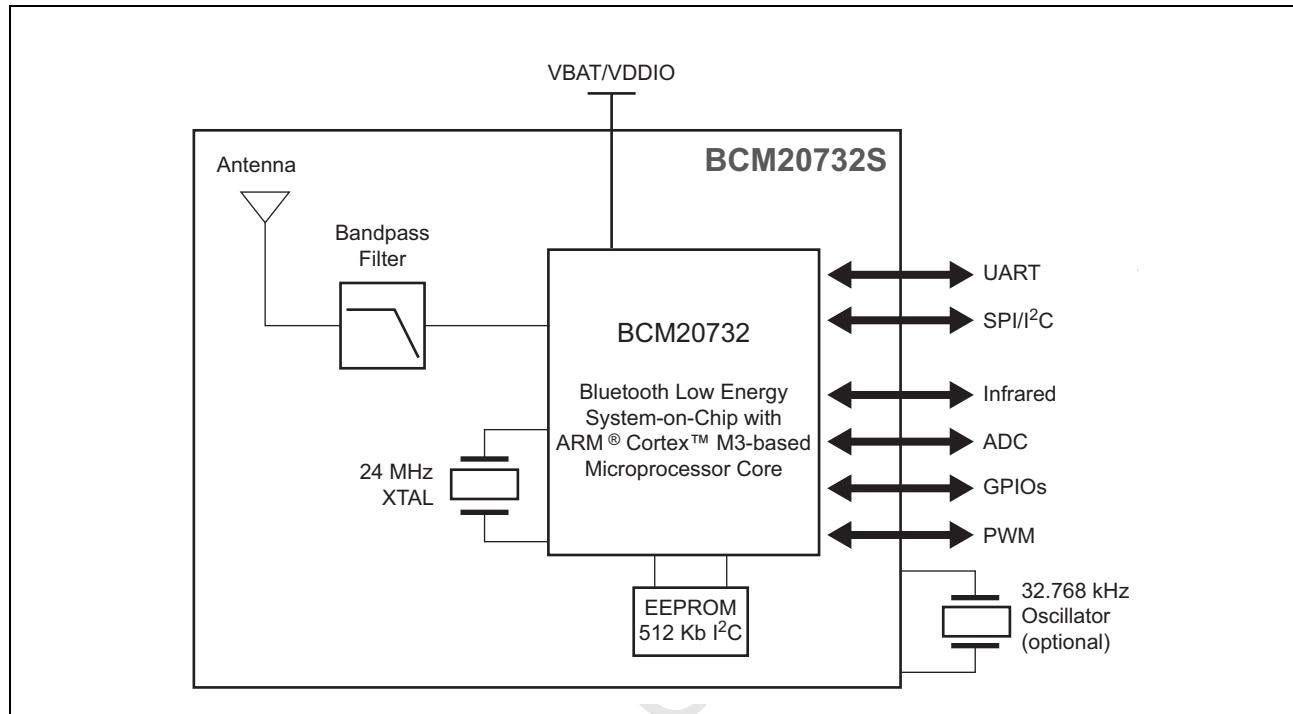
Additional profiles that can be supported in BCM20732S RAM include:

- Blood glucose monitor
- Temperature alarm
- Location
- Other custom profiles

## Block Diagram

A block diagram of the BCM20732S BLE SiP is shown in [Figure 1](#).

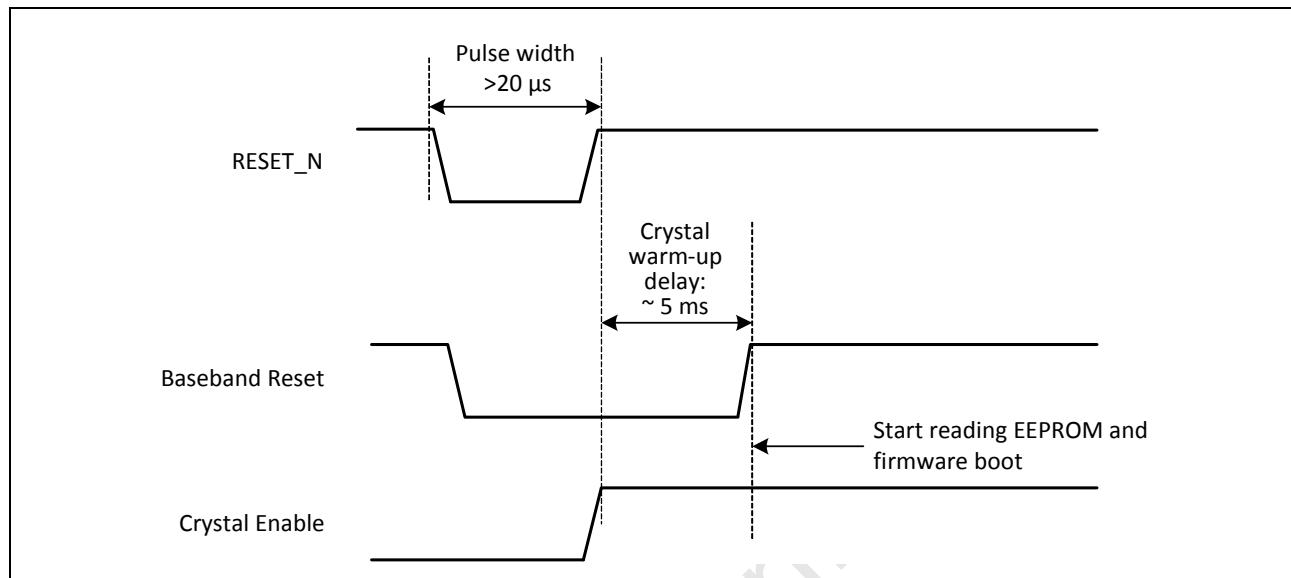
**Figure 1: BCM20732S BLE SiP Block Diagram**



## External Reset

External reset timing for the BCM20732S is illustrated in [Figure 2](#).

**Figure 2: External Reset Timing**



## 32.768 kHz Oscillator

The BCM20732S includes a standard Pierce oscillator. The oscillator circuit includes a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis eliminates chatter when the input is near the comparator threshold (~100 mV). The oscillator circuit can be designed for a 32 kHz or 32.768 kHz crystal oscillator, and can also be driven by an external clock input with a similar frequency. Characteristics for a 32 kHz oscillator are defined in [Table 1](#).

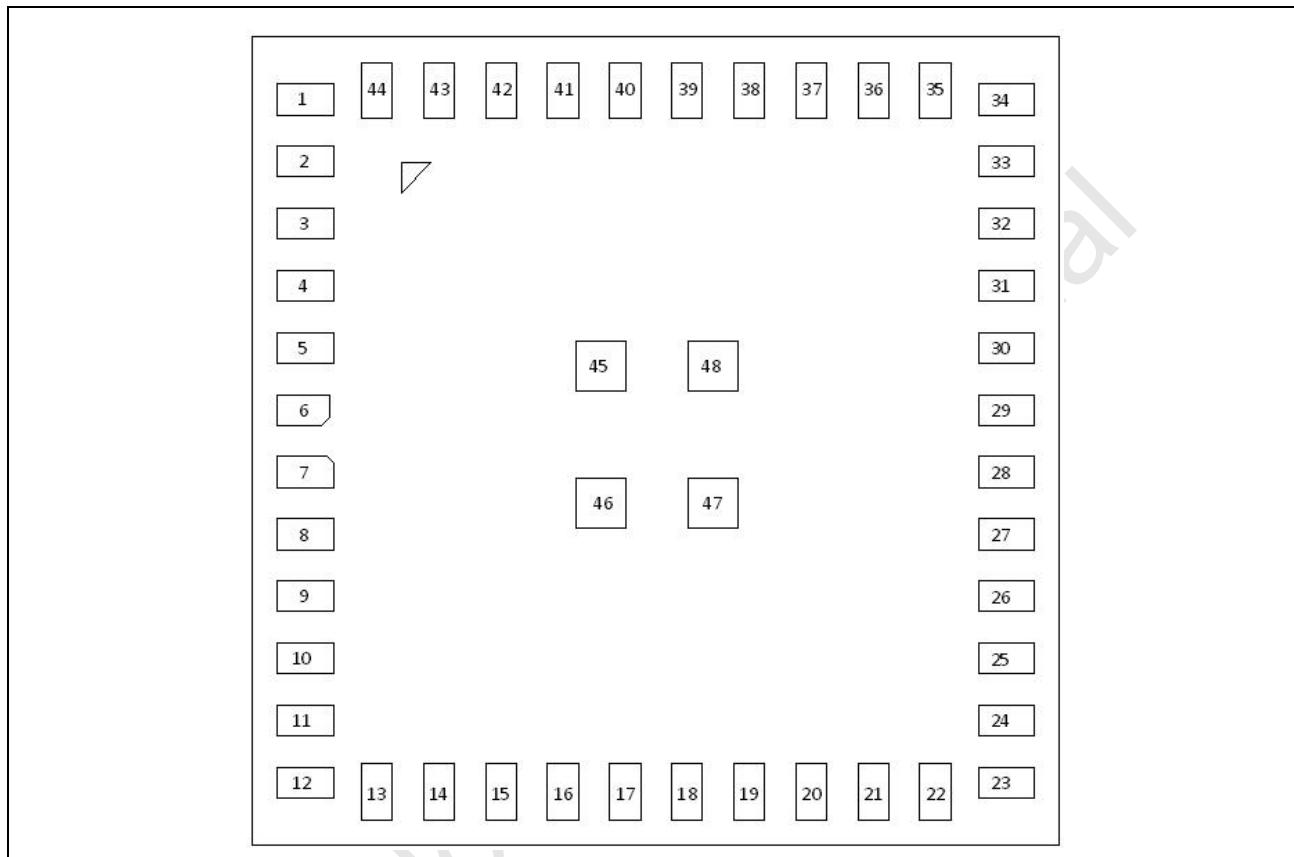
**Table 1: 32 kHz Crystal Oscillator Characteristics**

| Parameter                 | Symbol        | Conditions            | Min. | Typ.   | Max. | Unit      |
|---------------------------|---------------|-----------------------|------|--------|------|-----------|
| Output frequency          | $F_{oscout}$  | —                     | —    | 32.768 | —    | kHz       |
| Frequency tolerance       | $F_{tol}$     | Crystal-dependent     | —    | 100    | —    | ppm       |
| Start-up time             | $T_{startup}$ | —                     | —    | —      | 500  | $\mu s$   |
| Crystal drive level       | $P_{drv}$     | For crystal selection | 0.5  | —      | —    | $\mu W$   |
| Crystal series resistance | $R_{series}$  | For crystal selection | —    | —      | 70   | $k\Omega$ |
| Crystal shunt capacitance | $C_{shunt}$   | For crystal selection | —    | —      | 1.3  | pF        |

## Pin Map and Signal Descriptions

The BCM20732S pin map is shown in [Figure 3](#).

**Figure 3: BCM20732S (TOP View)**



The signal name, type, and description of each pin in the BCM20732S is listed in [Table 2](#). The symbols shown under I/O Type indicate pin directions (I/O = bidirectional, I = input, O = output) and the internal pull-up/pull-down characteristics (PU = weak internal pull-up resistor and PD = weak internal pull-down resistor), if any.

**Table 2: Pin Descriptions**

| <b>Pin</b> | <b>Name</b>       | <b>I/O Type</b> | <b>Description</b>   |
|------------|-------------------|-----------------|--|
| 1          | GPIO: P27<br>PWM1 | I               | Default direction: Input.<br>After POR state: Input floating.<br>Drain current: 16 mA<br>Alternate function: MOSI (master and slave) for SPI_2 |
| 2          | GND               | GND             | GND  |
| 3          | VBAT              | I               | Battery supply input.  |
| 4          | GND               | GND             | GND  |

**Table 2: Pin Descriptions (Cont.)**

| <b>Pin</b> | <b>Name</b> | <b>I/O Type</b> | <b>Description</b>  |
|------------|-------------|-----------------|---|
| 5          | GND         | GND             | GND   |
| 6          | GND         | GND             | GND   |
| 7          | GND         | GND             | GND   |
| 8          | GND         | GND             | GND   |
| 9          | GND         | GND             | GND   |
| 10         | Reserved    | –               | Leave floating  |
| 11         | GND         | GND             | GND   |
| 12         | GND         | GND             | GND   |
| 13         | GND         | GND             | GND   |
| 14         | GND         | GND             | GND   |
| 15         | GND         | GND             | GND   |
| 16         | GND         | GND             | GND   |
| 17         | GND         | GND             | GND   |
| 18         | UART_RX     | I               | UART_RX. This pin is pulled low through an internal 10 kΩ resistor.   |
| 19         | UART_TX     | O, PU           | UART_TX   |
| 20         | GND         | GND             | GND   |
| 21         | SCL         | I/O, PU         | SCL I/O, PU clock signal for an external I <sup>2</sup> C device  |
| 22         | SDA         | I/O, PU         | SDA I/O, PU data signal for an external I <sup>2</sup> C device   |
| 23         | GND         | GND             | GND   |
| 24         | GND         | GND             | GND   |
| 25         | GPIO: P1    | I               | Default direction: Input.<br>After POR state: Input floating.<br>This pin is tied to the WP pin of the embedded EEPROM.<br>Requires an external 10K pull-up   |
| 26         | TMC         | I               | Test mode control. Pull this pin high to invoke test mode; leave it floating if not used. This pin is connected to GND through an internal 10 kΩ resistor.  |
| 27         | RESET_N     | I/O PU          | Active-low system reset with open-drain output  |
| 28         | GPIO: P0    | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• Peripheral UART TX (PUART_TX)</li><li>• MOSI (master and slave) for SPI_2</li><li>• IR_RX</li><li>• 60Hz_main</li></ul> |
| 29         | GND         | GND             | GND   |

**Table 2: Pin Descriptions (Cont.)**

| <b>Pin</b> | <b>Name</b> | <b>I/O Type</b> | <b>Description</b>  |
|------------|-------------|-----------------|---|
| 30         | GPIO: P3    | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• Peripheral UART CTS (PUART_CTS)</li> <li>• SPI_CLK (master and slave) for SPI_2</li> </ul>  |
| 31         | GPIO: P2    | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• Peripheral UART RX (PUART_RX)</li> <li>• SPI_CS (slave only) for SPI_2</li> <li>• SPI_MOSI (master only) for SPI_2</li> </ul>                               |
| 32         | GPIO: P4    | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• Peripheral UART RX (PUART_RX)</li> <li>• MOSI (master and slave) for SPI_2.</li> <li>• IR_TX</li> </ul>   |
| 33         | GPIO: P8    | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions: A/D converter input</p>  |
| 34         | GPIO: P33   | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• A/D converter input</li> <li>• MOSI (slave only) for SPI_2</li> <li>• Auxiliary clock output (ACLK1)</li> <li>• Peripheral UART RX (PUART_RX)</li> </ul>    |
| 35         | GPIO: P32   | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• A/D converter input</li> <li>• SPI_CS (slave only) for SPI_2.</li> <li>• Auxiliary clock output (ACLK0)</li> <li>• Peripheral UART TX (PUART_TX)</li> </ul> |
| 36         | GPIO: P25   | I               | <p>Default direction: Input.</p> <p>After POR state: Input floating.</p> <p>Alternate functions:</p> <ul style="list-style-type: none"> <li>• MISO (master and slave) for SPI_2</li> <li>• Peripheral UART RX (PUART_RX)</li> </ul>   |

**Table 2: Pin Descriptions (Cont.)**

| <b>Pin</b> | <b>Name</b>       | <b>I/O Type</b> | <b>Description</b>  |
|------------|-------------------|-----------------|---|
| 37         | GPIO: P24         | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• SPI_CLK (master and slave) for SPI_2</li><li>• Peripheral UART TX (PUART_TX)</li></ul>    |
| 38         | N/C               | N/C             | N/C   |
| 39         | GPIO: P13<br>PWM3 | I               | Default Direction: Input<br>After POR State: Input Floating<br>Drain current: 16 mA<br>Alternate function: A/D converter input  |
|            | GPIO: P28<br>PWM2 | I               | Default direction: Input.<br>After POR state: Input floating.<br>Drain current: 16 mA<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• LED1</li><li>• IR_TX</li></ul>      |
| 40         | GPIO: P14<br>PWM2 | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate function: A/D converter input  |
|            | GPIO: P38         | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• MOSI (master and slave) for SPI_2</li><li>• IR_TX</li></ul> |
| 41         | GPIO: P15         | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• IR_RX</li><li>• 60 Hz_main</li></ul>                        |
| 42         | GPIO: P26<br>PWM0 | I               | Default direction: Input.<br>After POR state: Input floating.<br>Drain current: 16 mA<br>Alternate function: SPI_CS (slave only) for SPI_2  |

**Table 2: Pin Descriptions (Cont.)**

| <b>Pin</b>      | <b>Name</b> | <b>I/O Type</b> | <b>Description</b>   |
|-----------------|-------------|-----------------|--|
| 43 <sup>a</sup> | GPIO: P12   | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• XTALO32K</li></ul> |
|                 | XTALO32K    | O               | Low-power oscillator (LPO) output.<br>Alternate functions:<br>P12<br>P26   |
| 44 <sup>b</sup> | GPIO: P11   | I               | Default direction: Input.<br>After POR state: Input floating.<br>Alternate functions: <ul style="list-style-type: none"><li>• A/D converter input</li><li>• XTALI32K</li></ul> |
|                 | XTALI32K    | I               | Low-power oscillator (LPO) input.<br>Alternate functions: <ul style="list-style-type: none"><li>• P11</li><li>• P27</li></ul>  |
| 45              | GND         | GND             | GND  |
| 46              | GND         | GND             | GND  |
| 47              | GND         | GND             | GND  |
| 48              | GND         | GND             | GND  |

- a. When pin 43 (XTALO32K) is used, ADC/GPIO:P12 is unavailable. P26 may still be available.  
b. When pin 44 (XTALI32K) is used, ADC/GPIO:P11 is unavailable. P27 may still be available.

## Electrical Specifications

Absolute maximum ratings are defined in [Table 3](#).

**Table 3: Absolute Maximum Ratings**

| Parameter                                   | Min. | Max. | Unit |
|---|------|------|------|
| Supply power                                | NA   | 3.63 | V    |
| Storage temperature                         | -40  | 125  | °C   |
| Voltage ripple                              | 0    | ±2   | %    |
| Power supply (VBAT absolute maximum rating) | 1.62 | 3.63 | V    |

Power for the BCM20732S module is provided by the host through the power pins.

**Table 4: Voltage**

| Symbol | Parameter       | Min. | Typ. | Max. | Unit |
|--------|-----------------|------|------|------|------|
| VBAT   | Battery voltage | 1.62 | —    | 3.63 | V    |

**Table 5: Current Consumption**

| Operating Mode | Condition   | Nominal | Maximum | Unit |
|----------------|---|---------|---------|------|
| Receive        | Receiver and baseband are both operating, 100%    | 24.0    | 28.0    | mA   |
| Transmit       | Transmitter and baseband are both operating, 100% | 24.0    | 28.0    | mA   |
| Sleep          | Wake in < 5 ms                                    | 55.0    | 60.0    | µA   |
| Deep Sleep     | Wake on interrupt                                 | 2.0     | 2.5     | µA   |

**Note:** All measurements taken at 25°C

Based on the current measurements in [Table 5 on page 15](#), BCM20732S peak power values are:

- RX: 101.6 mW
- TX: 101.6 mW
- Sleep mode: 217.8 µW
- Deep Sleep mode: 9.1 µW

## RF Specifications

BCM20732S receiver specifications are defined in [Table 6](#).

**Table 6: Receiver Specifications**

| Parameter                    | Mode and Conditions  | Min. | Typ. | Max. | Unit |
|------------------------------|--|------|------|------|------|
| Frequency range              | –  | 2402 | –    | 2480 | MHz  |
| RX sensitivity<br>(standard) | Packets: 200<br>Payload: PRBS 9<br>Length: 37 Bytes<br>Dirty Transmitter: off.<br>PER: 30.8% | –    | -94  | –    | dBm  |
| Maximum input                | –  | -10  | –    | –    | dBm  |

**Note:** All measurements taken at 3.0V (default voltage)

RF transmitter specifications are defined in [Table 7](#).

**Table 7: Transmitter Specifications**

| Parameter  | Min. | Typ. | Max. | Unit      |
|--|------|------|------|-----------|
| <b>Transmitter</b>                                   |      |      |      |           |
| Frequency range <sup>a</sup>                         | 2402 | –    | 2480 | MHz       |
| Output power adjustment range                        | -20  | –    | 4    | dBm       |
| Output power   | –    | 2    | –    | dBm       |
| Output power variation                               | –    | 2.5  | –    | dB        |
| <b>LO Performance</b>                                |      |      |      |           |
| Initial carrier frequency tolerance                  | –    | –    | ±150 | kHz       |
| <b>Frequency Drift</b>                               |      |      |      |           |
| Frequency drift                                      | –    | –    | ±50  | kHz       |
| Drift rate   | –    | –    | 20   | kHz/50 µs |
| <b>Frequency Deviation</b>                           |      |      |      |           |
| Average deviation in payload<br>(sequence: 00001111) | 225  | –    | 275  | kHz       |
| Average deviation in payload<br>(sequence: 10101010) | 185  | –    | –    | kHz       |
| Channel spacing                                      | –    | 2    | –    | MHz       |

a. This parameter is taken from the Bluetooth 4.0 specification.

## ADC Specifications

BCM20732S ADC specifications are defined in [Table 8](#).

**Table 8: ADC Specifications**

| <b>Parameter</b>                   | <b>Symbol</b> | <b>Conditions</b>                   | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> | <b>Unit</b>      |
|------------------------------------|---------------|-------------------------------------|-------------|-------------|-------------|------------------|
| Number of input channels           | —             | —                                   | —           | 9           | —           | —                |
| Channel switching rate             | $f_{ch}$      | —                                   | —           | —           | 133.33      | Kch/s            |
| Input signal range                 | $V_{inp}$     | —                                   | 0           | —           | 3.63        | V                |
| Reference settling time            | —             | Charging refsel                     | 7.5         | —           | —           | $\mu$ s          |
| Input resistance                   | $R_{inp}$     | Effective, single-ended             | —           | 500         | —           | k $\Omega$       |
| Input capacitance                  | $C_{inp}$     | —                                   | —           | —           | 5           | pF               |
| Conversion rate                    | $F_c$         | —                                   | 5.859       | —           | 187         | kHz              |
| Conversion time                    | $T_c$         | —                                   | 5.35        | —           | 170.7       | $\mu$ s          |
| Resolution                         | R             | —                                   | —           | 16          | —           | Bits             |
| Absolute voltage measurement error | —             | Using on-chip ADC firmware driver   | —           | $\pm 2$     | —           | %                |
| Current                            | I             | $I_{avdd1p2} + I_{avdd3p3}$         | —           | —           | 1           | mA               |
| Power                              | P             | —                                   | —           | 1.5         | —           | mW               |
| Leakage Current                    | $I_{leakage}$ | $T = 25^{\circ}\text{C}$            | —           | —           | 100         | nA               |
| Power-up time                      | $T_{powerup}$ | —                                   | —           | —           | 200         | $\mu$ s          |
| Integral nonlinearity              | $I_{NL}$      | In the guaranteed performance range | —1          | —           | 1           | LSB <sup>a</sup> |
| Differential nonlinearity          | $D_{NL}$      | In the guaranteed performance range | —1          | —           | 1           | LSB <sup>a</sup> |

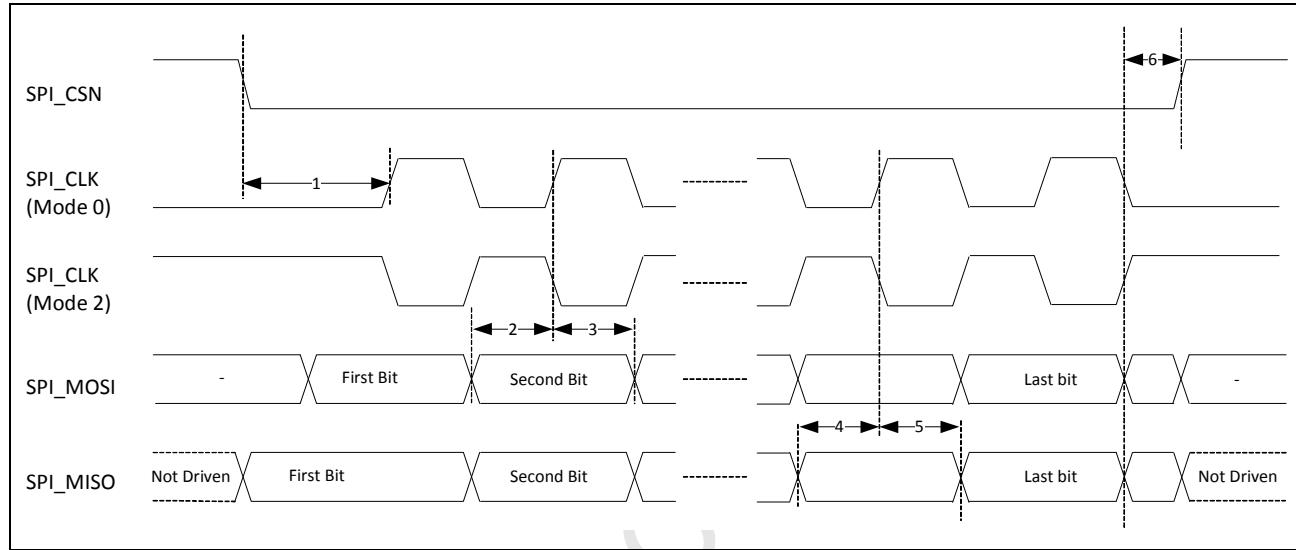
a. LSBs are expressed at the 10-bit level.

## Timing and AC Characteristics

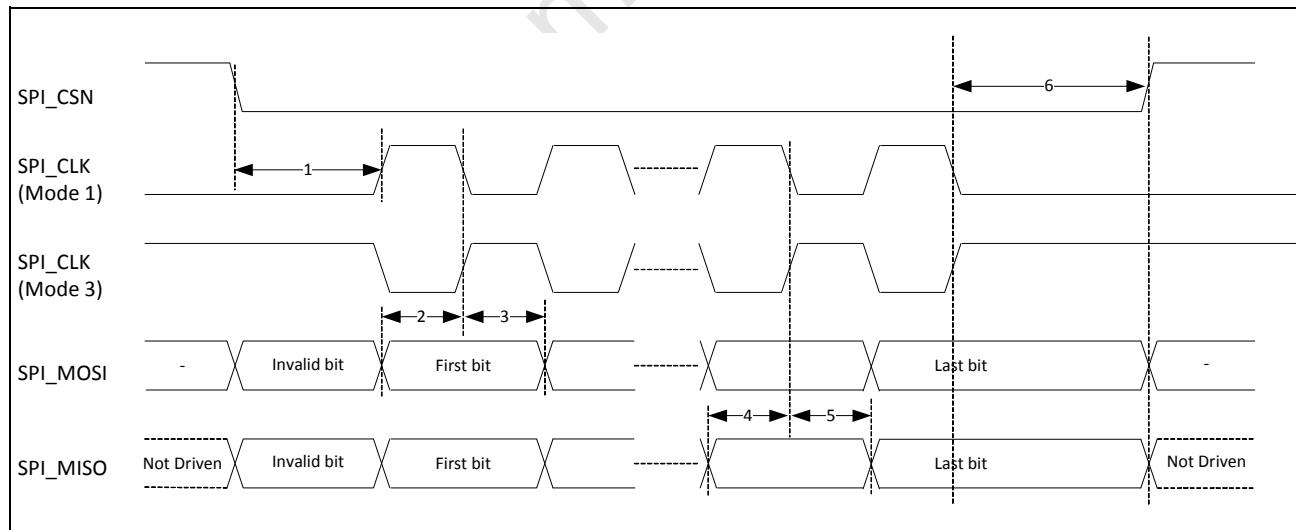
### SPI Timing

SPI interface timing is illustrated in [Figure 4](#) and [Figure 5](#) and are defined in [Table 9](#) on page 18.

**Figure 4: SPI Timing—Modes 0 and 2**



**Figure 5: SPI Timing—Modes 1 and 3**



**Table 9: SPI Interface Timing Specifications**

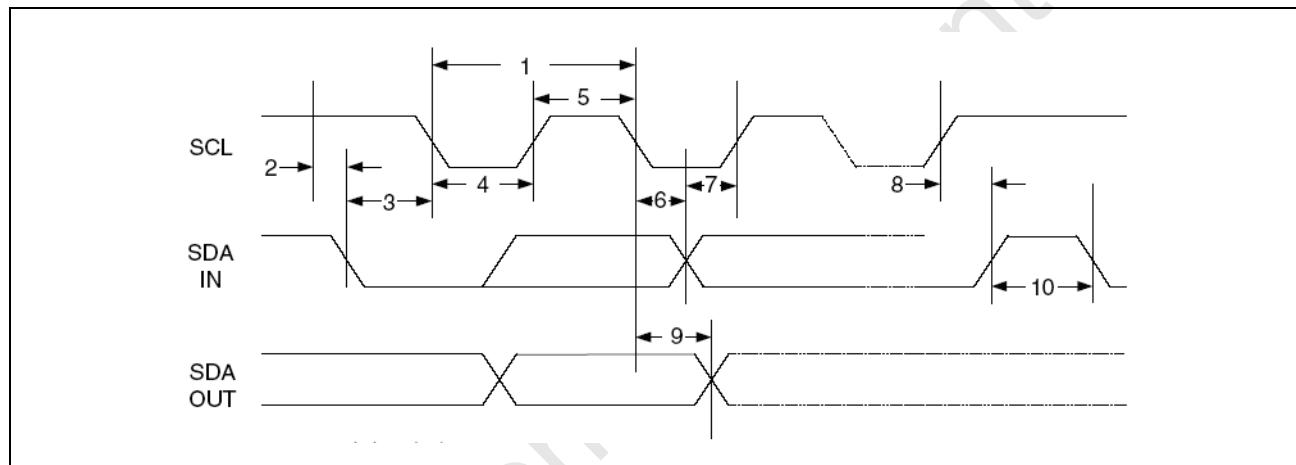
| Reference | Characteristics                            | Min.  | Typ. | Max.     |
|-----------|--|-------|------|----------|
| 1         | Time from CSN asserted to first clock edge | 1 SCK | 100  | $\infty$ |

**Table 9: SPI Interface Timing Specifications**

| <b>Reference</b> | <b>Characteristics</b>                      | <b>Min.</b> | <b>Typ.</b> | <b>Max.</b> |
|------------------|---|-------------|-------------|-------------|
| 2                | Master setup time                           | —           | 1/2SCK      | —           |
| 3                | Master hold time                            | 1/2SCK      | —           | —           |
| 4                | Slave setup time                            | —           | 1/2 SCK     | —           |
| 5                | Slave hold time                             | 1/2 SCK     | —           | —           |
| 6                | Time from last clock edge to CSN deasserted | SCK         | 10 SCK      | 100         |

## BSC Interface Timing

BSC interface timing is illustrated in [Figure 6](#) and is defined in [Table 10](#).

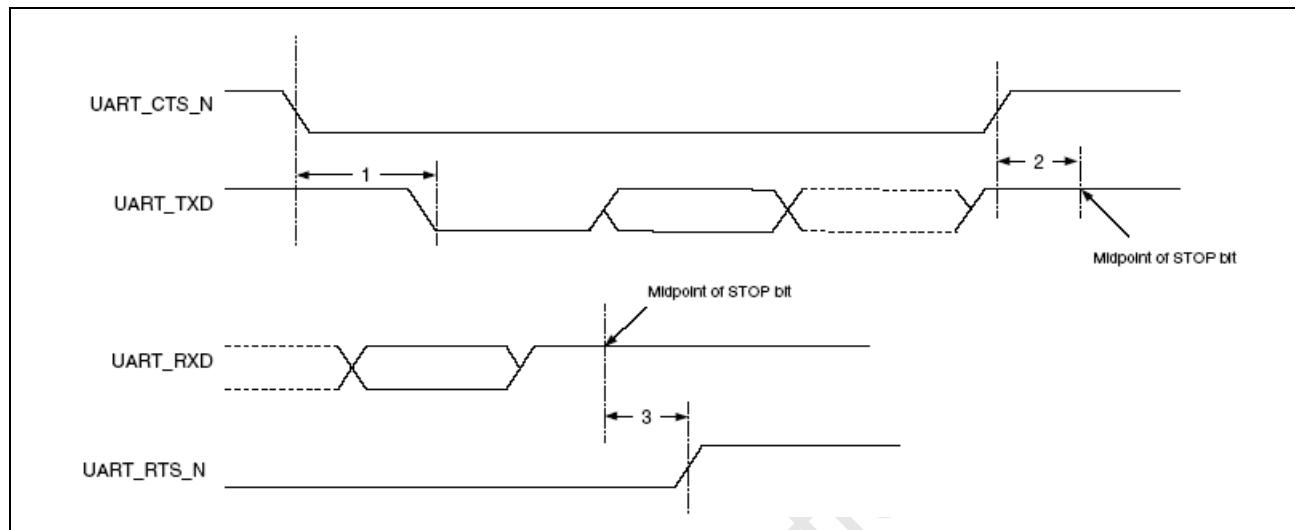
**Figure 6: BSC Interface Timing****Table 10: BSC Interface Timing Specifications**

| <b>Reference</b> | <b>Characteristics</b>     | <b>Min.</b> | <b>Max.</b>         | <b>Unit</b> |
|------------------|----------------------------|-------------|---------------------|-------------|
| 1                | Clock frequency            | —           | 100, 400, 800, 1000 | kHz         |
| 2                | START condition setup time | 650         | —                   | ns          |
| 3                | START condition hold time  | 280         | —                   | ns          |
| 4                | Clock low time             | 650         | —                   | ns          |
| 5                | Clock high time            | 280         | —                   | ns          |
| 6                | Data input hold time       | 0           | —                   | ns          |
| 7                | Data input setup time      | 100         | —                   | ns          |
| 8                | STOP condition setup time  | 280         | —                   | ns          |
| 9                | Output valid from clock    | —           | 400                 | ns          |
| 10               | Bus free time              | 650         | —                   | ns          |

## UART Timing

UART timing is illustrated in [Figure 7](#) and defined in [Table 11](#).

**Figure 7: UART Timing**



**Table 11: UART Timing Specifications**

| Reference | Characteristics  | Min. | Max. | Unit           |
|-----------|--|------|------|----------------|
| 1         | Delay time, <b>UART_CTS_N</b> low to <b>UART_TXD</b> valid     | –    | 24   | Baudout cycles |
| 2         | Setup time, <b>UART_CTS_N</b> high before midpoint of stop bit | –    | 10   | ns             |
| 3         | Delay time, midpoint of stop bit to <b>UART_RTS_N</b> high     | –    | 2    | Baudout cycles |

## PCB Design and Manufacturing Recommendations

### Pad and Solder Mask Opening Dimensions

BCM20732S pad and solder mask opening dimensions are defined in [Table 12](#).

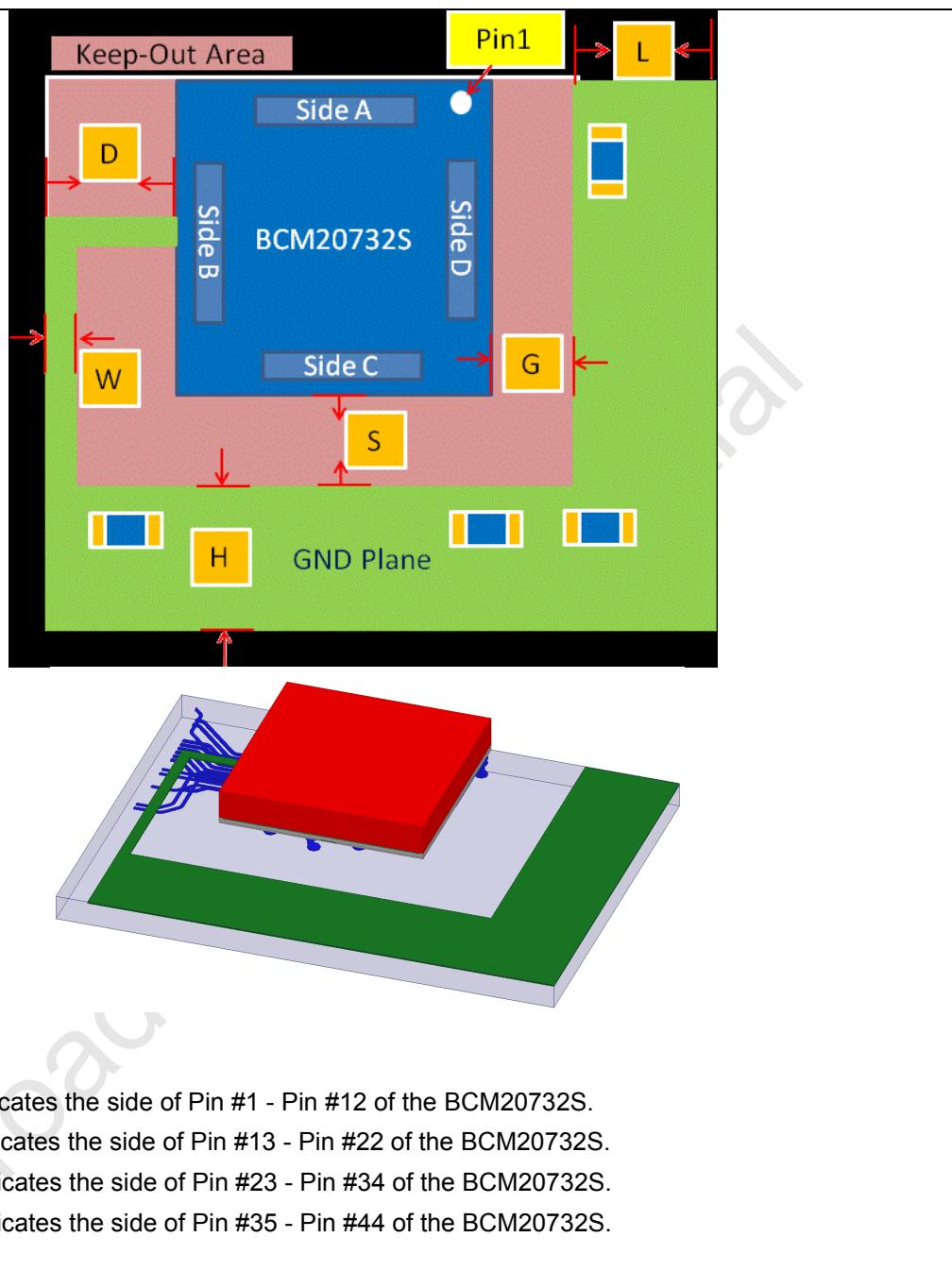
**Table 12: Pad and Solder Mask Dimensions**

| Pad Type | Pad Dimensions | Solder Mask Opening Dimensions | Unit |
|----------|----------------|--------------------------------|------|
| Type A   | 0.6 × 0.25     | 0.7 × 0.35                     | mm   |
| Type B   | 0.55 × 0.3     | 0.65 × 0.4                     |      |
| Type C   | 0.4 × 0.4      | 0.5 × 0.5                      |      |

### PCB Layout Recommendations for Configuration A

The following layout recommendations are referenced to [Figure 8 on page 22](#):

- Connect to system ground from side B of the module (pins 13–22).
- An L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout in [Figure 8 on page 22](#) and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)
- Route signal traces out of the module from side C (between pins 27 and 30) or side B (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or sideD.

**Figure 8: PCB Layout Example, Configuration A**

## Example of an L-Shaped Ground Plane

Figure 9 shows an L-shaped ground arrangement in the 2nd layer (purple color) and the top-side component placement and trace routing (blue color). We can see that some components and routings are placing in the L-shaped area on the top layer and the “L -shaped” ground is connected to system ground in the 2nd layer.

Figure 9 also indicates the clearance area (marked in yellow) and L-shaped GND area (marked in green).

**Figure 9: L-Shaped Ground Plane**

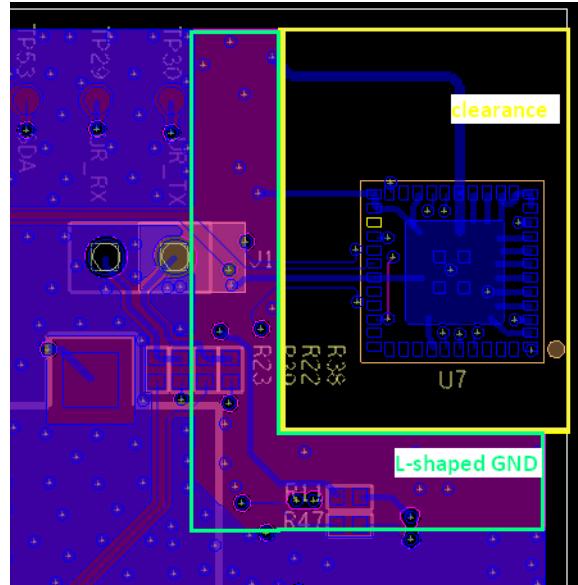
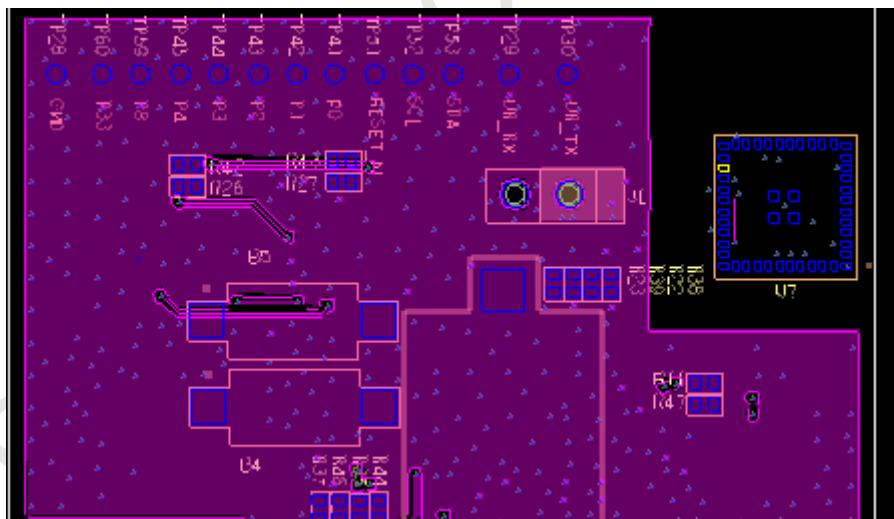


Figure 10 shows an L-shaped ground (arranged in the 2nd layer) only.

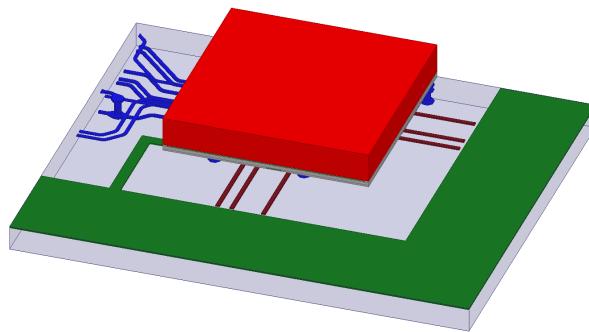
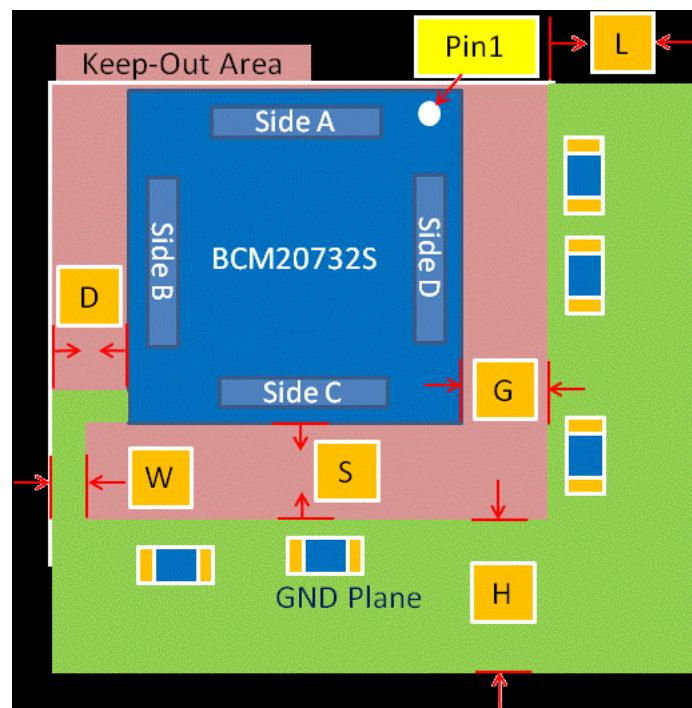
**Figure 10: L-Shaped Ground Plane, 2nd Layer**



## PCB Layout Recommendations for Configuration B

The following layout recommendations are referenced to [Figure 11 on page 25](#):

- Connect to system ground from side B of the module (pins 13–22).
- An L-shaped ground plane is required for the embedded BLE antenna. Keep the GND continuous. Do not cut off the GND shape to accommodate trace routes.
- If the L-shaped GND plane is located on the top layer of the PCB, do not place components on the ground plane. If this cannot be avoided, move the L-shaped ground plane to another layer.
- Antenna efficiency of 31–41% can be achieved based on the layout in [Figure 11 on page 25](#) and the dimensions listed below. Following these layout recommendations is expected to yield 50+ meters of usable range; deviating from these recommendations may reduce the range of the antenna.
  - D: 4.5 mm (typical)
  - G, H, S: 3 mm (typical)
  - L: 3 mm (minimum)
  - W: 0.4 mm (typical)
- Route signal traces out of the module from side C (between pins 27 and 30) or side B (between pins 16 and 19) of the module. Traces can be overlapped to avoid routing through the keep-out area.
- Do not route traces from side A or sideD.

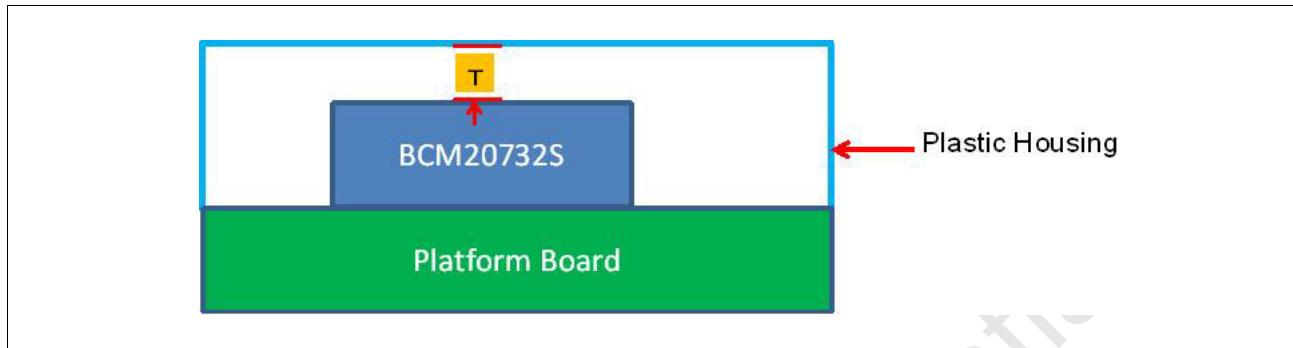
**Figure 11: PCB Layout Example, Configuration B****Notes:**

- Side A indicates the side of Pin #1 - Pin #12 of the **BCM20732S**.
- Side B indicates the side of Pin #13 - Pin #22 of the **BCM20732S**.
- Side C indicates the side of Pin #23 - Pin #34 of the **BCM20732S**.
- Side D indicates the side of Pin #35 - Pin #44 of the **BCM20732S**.

## Common Guidelines for BCM20732S

It is recommended to have a 0.4 mm gap between the chip's upper surface and the plastic housing (Figure 12).

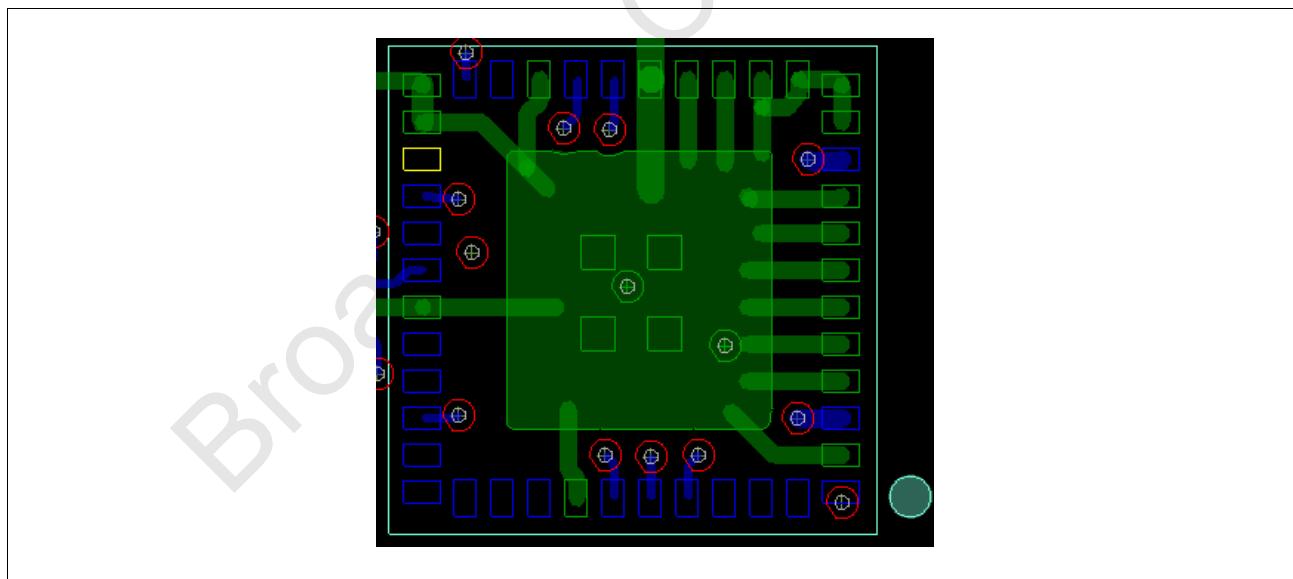
Figure 12: Gap Between Chip's Upper Surface and Plastic Housing



Refer to the following link for information about the plastic housing: PC - ABS, <http://www.stratasys.com/~media/Fortus/Files/PDFs/MS-PC-ABS-FORTUS.ashx>.

Arrange the GND plane under the module and connect the GND pins of the module to the GND plane as shown in Figure 14.

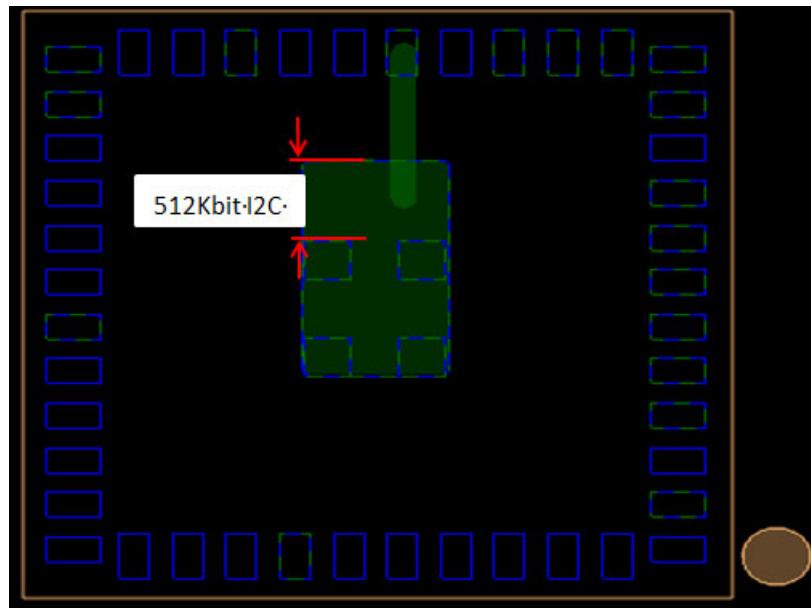
Figure 13: Example of Ground Plane Under the Module



**Note:** Do not route the GND plane under the RF pin.

If you are unable to reserve such a large GND plane, then use the minimal required area as shown in [Figure 14](#).

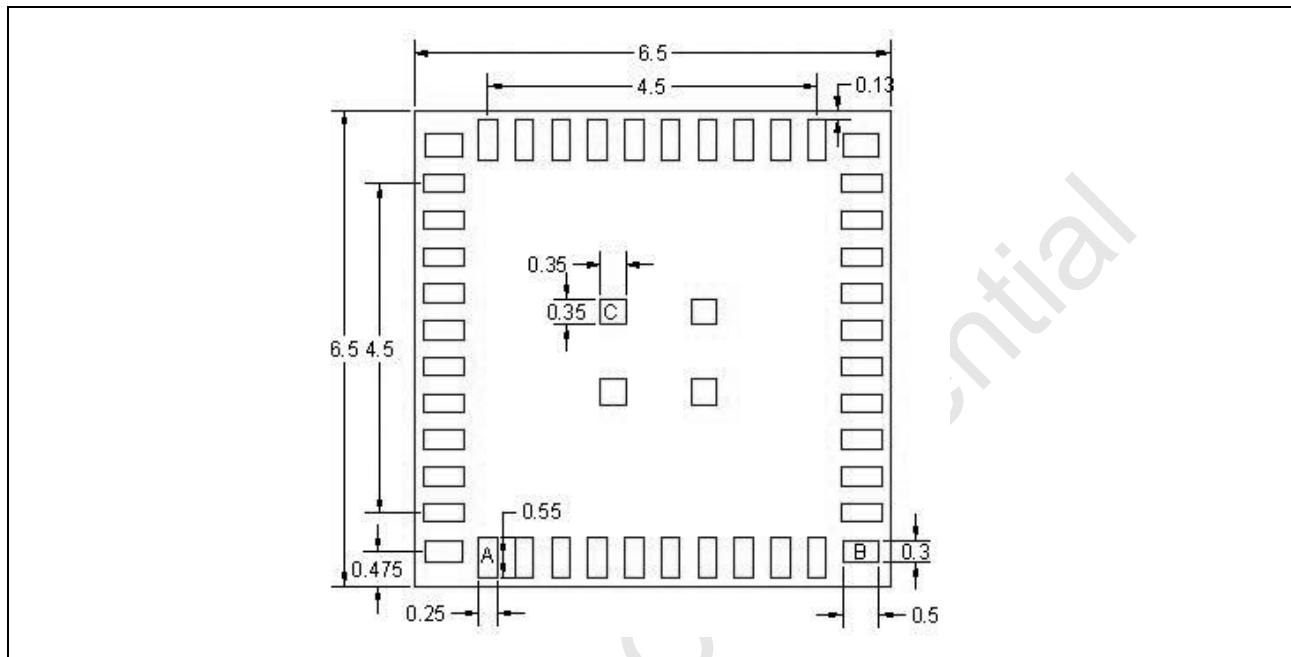
**Figure 14: Minimum Required Ground Plane**



# PCB Stencil

The recommended PCB stencil is shown in [Figure 15](#) (all measurements in mm). Use an unsolder mask to set the module footprint.

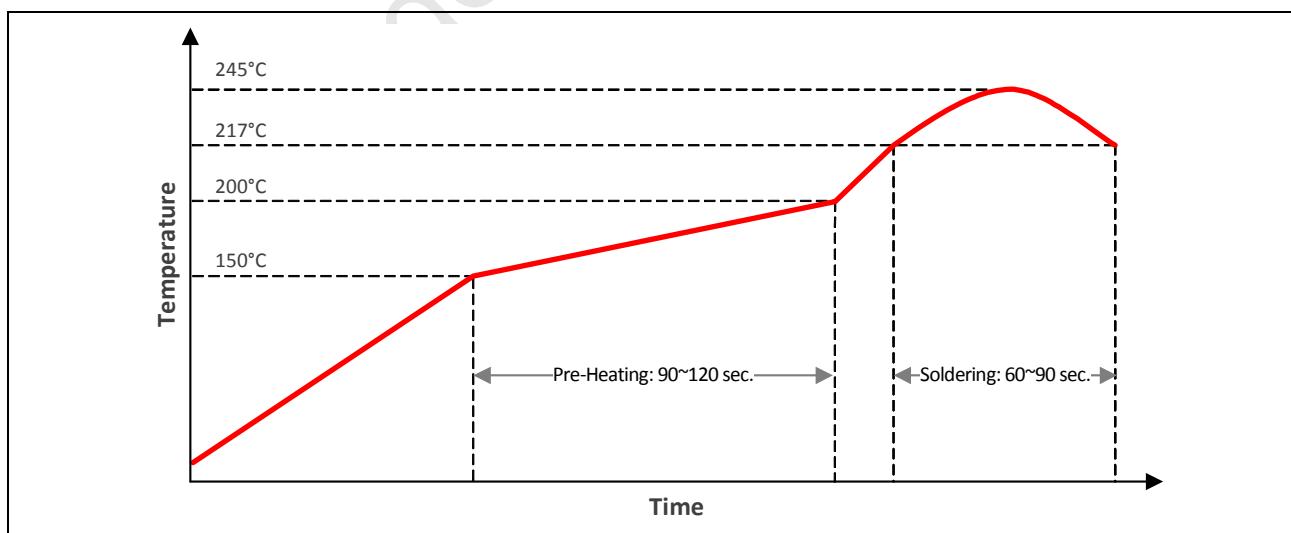
**Figure 15: BCM20732S Stencil (Bottom View)**



# Solder Reflow

The recommended solder reflow profile for the BCM20732S is defined in Figure 16.

**Figure 16: Solder Reflow Profile**



## Packaging and Storage Information

The BCM20732S is available in a tape and reel package and is shipped in an ESD-protected moisture-resistant (MSL-3) bag as shown in [Figure 17](#). The storage temperature range is -40°C to +125°C.

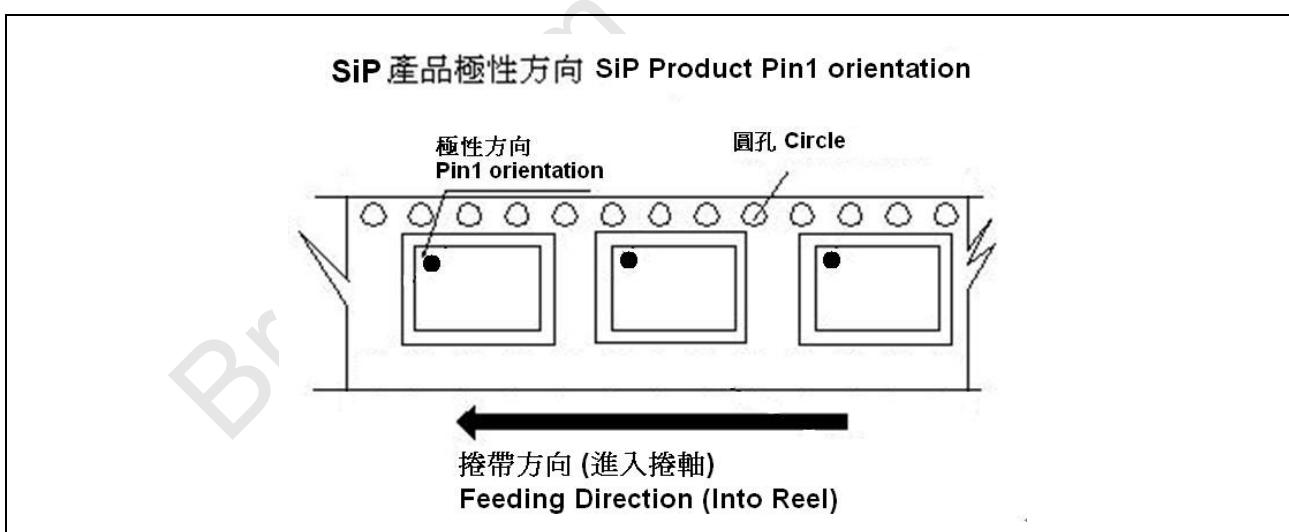
**Figure 17: BCM20732S ESD/Moisture Packaging**



The moisture sensitivity label on the BCM20732S shipping bag is shown in [Figure 18 on page 30](#).

**Figure 18: BCM20732S Moisture Sensitivity Label**

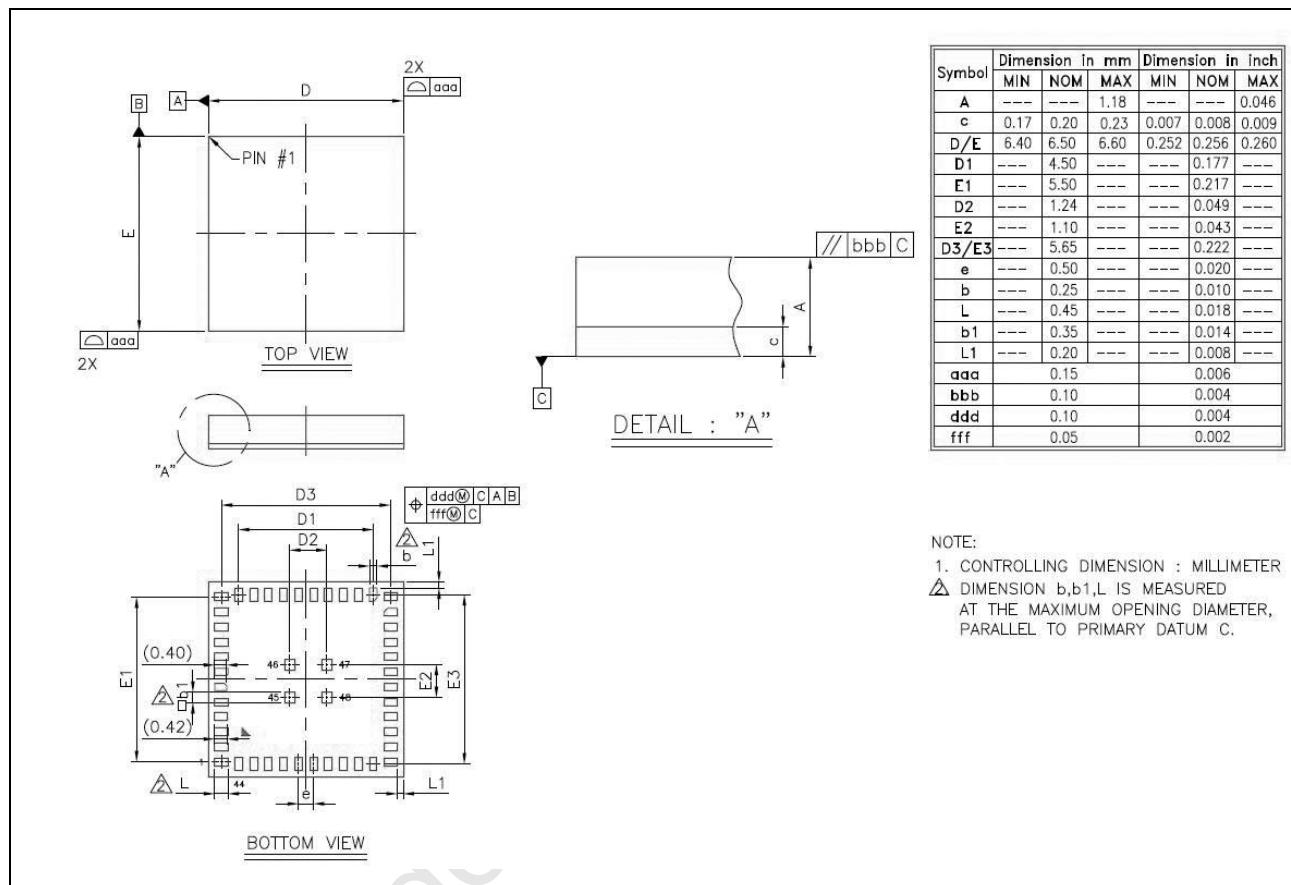
Figure 19 shows the location of pin 1 on the BCM20732S relative to its orientation on the tape packaging.

**Figure 19: BCM20732S Tape and Reel Pin 1 Location**

## Mechanical Information

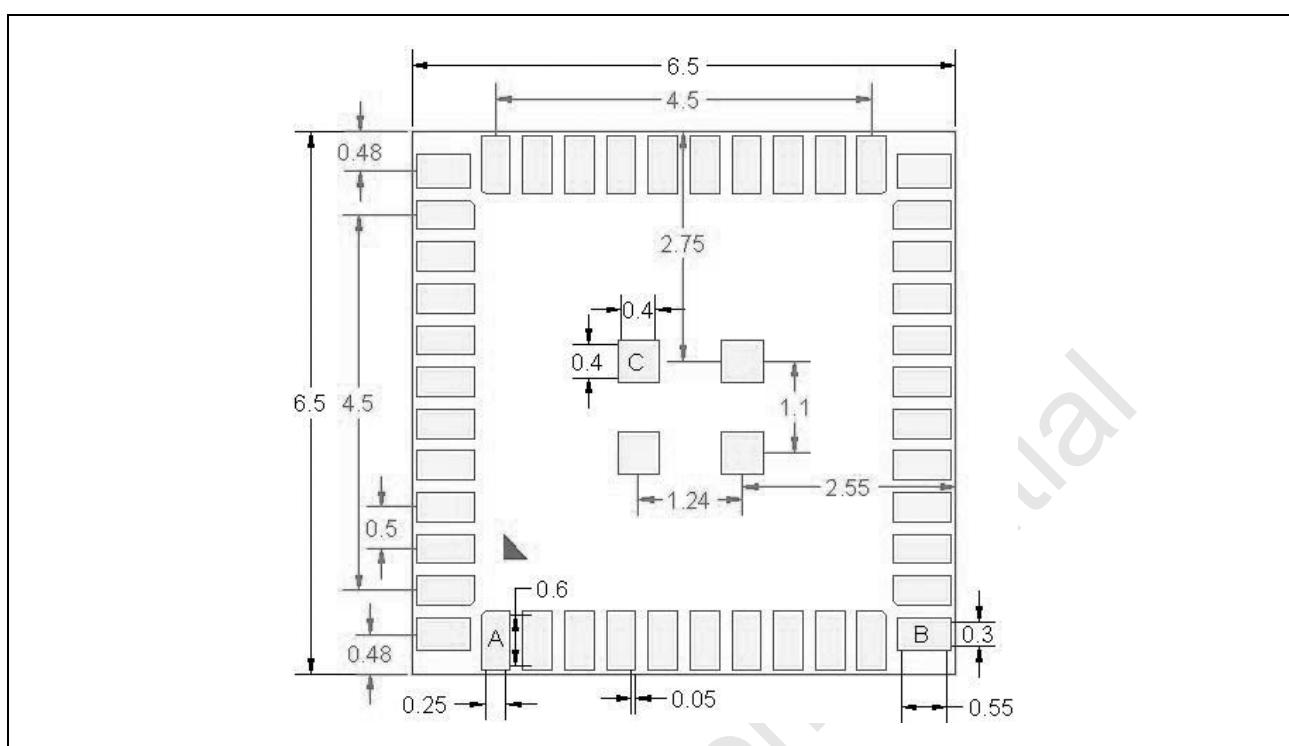
Package dimensions for the BCM20732S are shown in [Figure 20](#).

**Figure 20: BCM20732S Package Dimensions**



Additional BCM20732S package dimensions are shown in [Figure 21 on page 32](#).

**Figure 21: BCM20732S Pin Dimensions (Bottom View)**



## **Ordering Information**

**Table 13: Ordering Information**

| <b>Part Number</b> | <b>Package</b> | <b>Operating Temperature</b> | <b>Humidity</b>         |
|--------------------|----------------|------------------------------|-------------------------|
| BCM20732S          | 48-pin LGA     | –40°C to +85°C               | 95% max., noncondensing |

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